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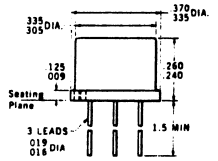
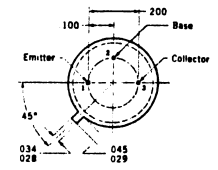
GENERAL DESCRIPTION — The 2N3467 and 2N3468 are low power, silicon PNP triode transistors designed primarily for high speed saturated switching and for core driving applications.

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-5) outline





NOTES: All dimensions in inches
Leads are gold-plated kovar
Collector internally connected to case
Package weight is 1.1 grams

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature		−65°C to +200°C
Operating Junction Temperature		+200°C
Lead Temperature (soldering, 10 second time limit)		+230°C
Maximum Power Dissipation (Notes 2 and 3)		
Total Dissipation at 25°C Ambient Temperature		1.0 Watt
at 25°C Case Temperature		5.0 Watts
Maximum Voltages and Current	2N3467	2N3468
V_{CBO} Collector to Base Voltage	−40 Volts	−50 Volts
V_{CEO} Collector to Emitter Voltage (Note 4)	−40 Volts	−50 Volts
V_{EBO} Emitter to Base Voltage	−5.0 Volts	−5.0 Volts
I_C Collector Current	1.0 Amp	1.0 Amp

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N3467 Min.	2N3467 Max.	2N3468 Min.	2N3468 Max.	UNITS	TEST CONDITIONS
t_d	Turn On Delay Time (Figure 1)		10		10	ns	$I_C = 500$ mA $I_{B1} = 50$mA
t_r	Rise Time (Figure 1)		30		30	ns	$I_C = 500$ mA $I_{B1} = 50$mA
t_s	Storage Time (Figure 2)		60		60	ns	$I_C = 500$ mA $I_{B1} = I_{B2} = 50$ mA
t_f	Fall Time (Figure 2)		30		30	ns	$I_C = 500$ mA $I_{B1} = I_{B2} = 50$ mA
C_{ob}	Output Capacitance (f = 100 kHz)		25		25	pF	$I_E = 0$ $V_{CB} = -10$ V
C_{ib}	Input Capacitance (f = 100 kHz)		100		100	pF	$I_C = 0$ $V_{OB} = -0.5$ V
h_{fe}	High Frequency Current Gain (f = 100 MHz)	1.75		1.5			$I_C = 50$ mA $V_{CE} = 10$ V
BV_{CBO}	Collector to Base Breakdown Voltage	−40		−50		Volts	$I_C = 10\ \mu$A $I_E = 0$
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0		−5.0		Volts	$I_E = 10\ \mu$A $I_C = 0$
BV_{CEO}	Collector to Emitter Breakdown Voltage (Note 5)	−40		−50		Volts	$I_C = 10$ mA $I_B = 0$
h_{FE}	DC Pulse Current Gain (Note 5)	40		25			$I_C = 150$ mA $V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	40	120	25	75		$I_C = 500$ mA $V_{CE} = -1.0$ V
h_{FE}	DC Pulse Current Gain (Note 5)	40		20			$I_C = 1.0$ A $V_{CE} = -5.0$ V
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)		−0.30		−0.35	Volt	$I_C = 150$ mA $I_B = 15$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)		−0.50		−0.60	Volt	$I_C = 500$ mA $I_B = 50$ mA
$V_{CE(sat)}$	Pulsed Collector Saturation Voltage (Note 5)		−1.0		−1.2	Volts	$I_C = 1.0$ A $I_B = 100$ mA

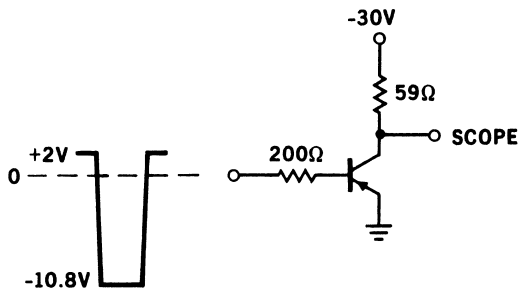
NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
(3) These ratings give a maximum junction temperature of 200°C and junction to case thermal resistance of 35°C/Watt (derating factor of 28.6 mW/°C); junction to ambient thermal resistance of 175°C/Watt (derating factor of 5.71 mW/°C).
(4) This rating refers to a high current point where collector to emitter voltage is lowest. For more information send for Fairchild Publicaion APP-4/2.
(5) Pulse Conditions: length = 300 μs; duty cycle = 1%.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N3467 Min.	2N3467 Max.	2N3468 Min.	2N3468 Max.	UNITS	TEST CONDITIONS
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 5)		−1.0		−1.0	Volt	$I_C = 150$ mA $I_B = 15$ mA
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 5)	−0.8	−1.2	−0.8	−1.2	Volts	$I_C = 500$ mA $I_B = 50$ mA
$V_{BE}(sat)$	Pulsed Base Saturation Voltage (Note 5)		−1.6		−1.6	Volts	$I_C = 1.0$ A $I_B = 100$ mA
I_{CBO}	Collector Cutoff Current		100		100	nA	$V_{CB} = -30$ V $I_E = 0$
$I_{CBO(100°C)}$	Collector Cutoff Current		15		15	μA	$V_{CB} = -30$ V $I_E = 0$
I_{CEX}	Collector Cutoff Current		100		100	nA	$V_{CB} = -30$ V $V_{OB} = -3.0$ V
I_{BL}	Base Cutoff Current		120		120	nA	$V_{CB} = -30$ V $V_{OB} = -3.0$ V
Q_T	Total Control Charge (Figure 3)		6.0		6.0	nC	$I_C = 500$ mA $I_B = 50$ mA

FIGURE 1

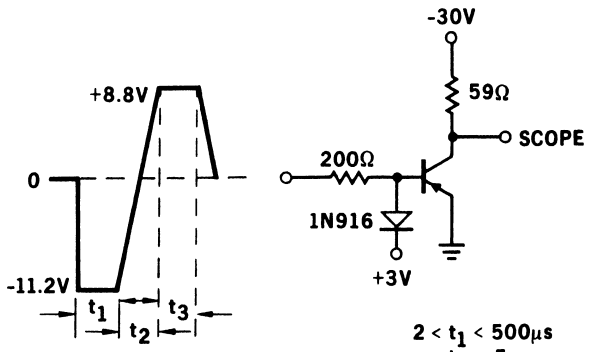
TURN-ON EQUIVALENT TEST CIRCUIT



PW = 200ns
RISE TIME ≤ 2ns
DUTY CYCLE = 2%

FIGURE 2

TURN-OFF EQUIVALENT TEST CIRCUIT



$2 < t_1 < 500\mu s$
$t_2 < 5$ns
$t_3 > 1\mu s$
DUTY CYCLE = 2%

FIGURE 3

Q_T TEST CIRCUIT