FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-13808-2E

16-bit Proprietary Microcontroller

CMOS

F²MC-16FX MB96310 Series

MB96F313/F315

■ DESCRIPTION

MB96310 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Note: F²MC is the abbreviation of Fujitsu Flexible Microcontroller

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

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■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

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Feature	Description
Real Time Clock	• Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every half second/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 48-pin plastic LQFP M26
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

■ PRODUCT LINEUP

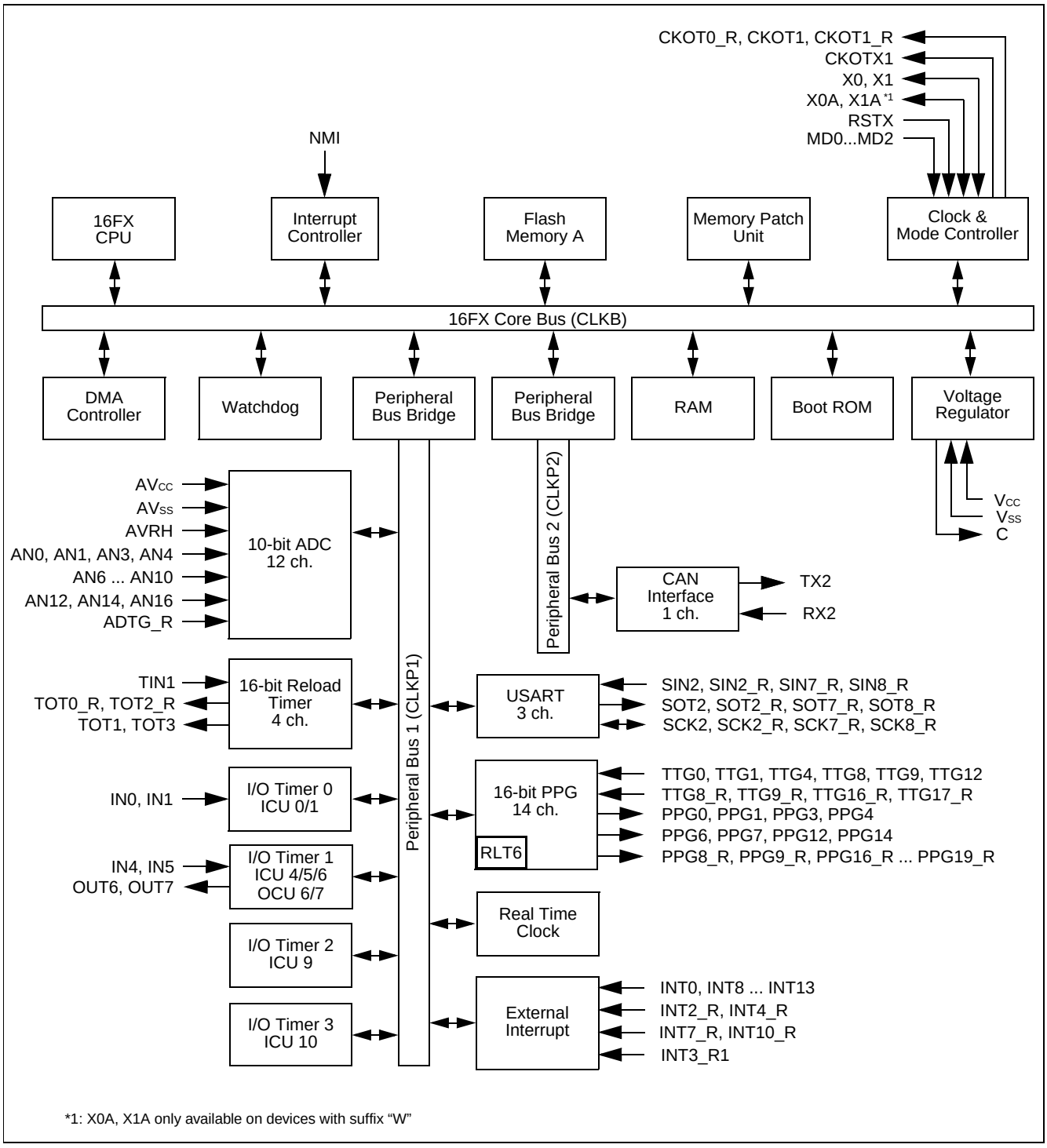
Features		MB96V300C	MB96(F)31x
Product type		Evaluation sample	Flash product: MB96F31x Mask ROM product: MB9631x
Product options			
YS		NA	Low voltage reset persistently on / Single clock devices
RS			Low voltage reset can be disabled / Single clock devices
YW			Low voltage reset persistently on / Dual clock devices
RW			Low voltage reset can be disabled / Dual clock devices
AS			No CAN / Low voltage reset can be disabled / Single clock devices
AW			No CAN / Low voltage reset can be disabled / Dual clock devices
Flash/ ROM	RAM		
96KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96F313Y, MB96F313R, MB96F313A
160KB	8KB		MB96F315Y, MB96F315R, MB96F315A
Package		BGA416	FPT-48P-M26
DMA		16 channels	4 channels
USART		10 channels	3 channels
A/D Converter		40 channels	12 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	4 channels (without external clock input pin)
16-bit Output Compare		12 channels	2 channels
16-bit Input Capture		12 channels	4 channels (plus 3 channels for LIN USART)
16-bit Programmable Pulse Generator		20 channels	14 channels
CAN Interface		5 channels	1 channel
External Interrupts		16 channels	11 channels
Non-Maskable Interrupt		1 channel	
Real Time Clock		1	
I/O Ports		136	34 for part number with suffix "W", 36 for part number with suffix "S"

000953H	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954H	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W

Features	MB96V300C	MB96(F)31x
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

■ BLOCK DIAGRAM

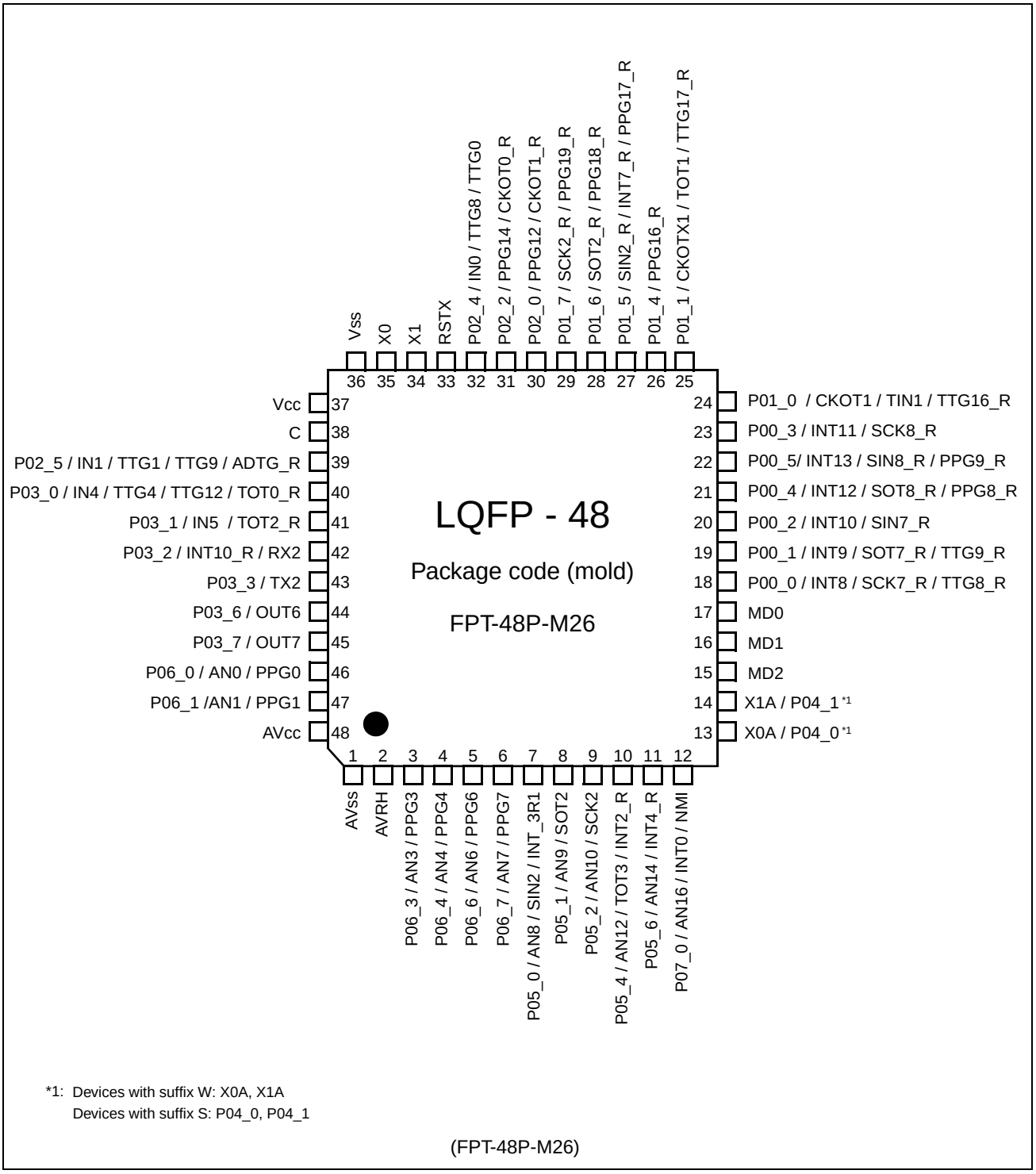
Block diagram of MB96(F)31x



*1: X0A, X1A only available on devices with suffix “W”

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)31x



*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

(FPT-48P-M26)

■ PIN FUNCTION DESCRIPTION

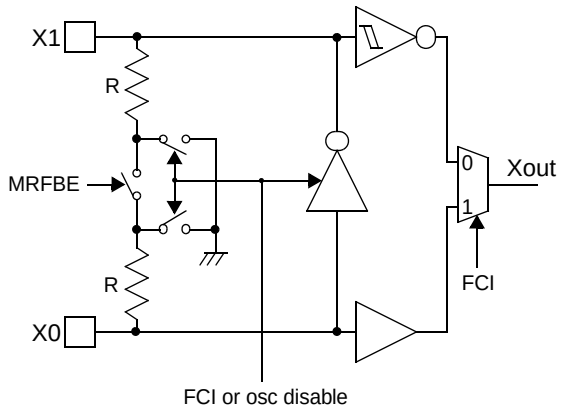
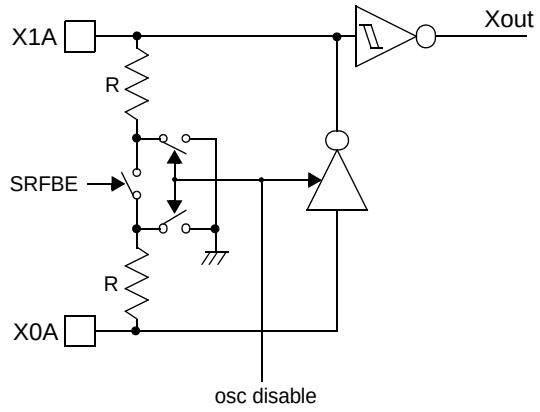
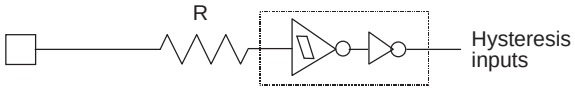
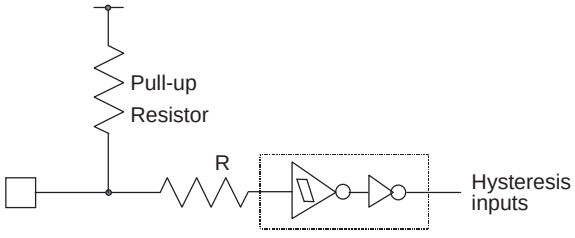
Pin Function description (1 of 2)

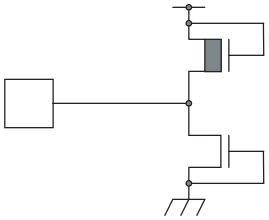
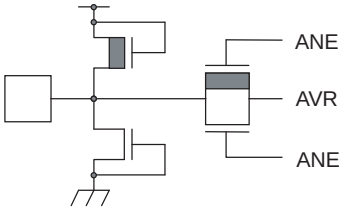
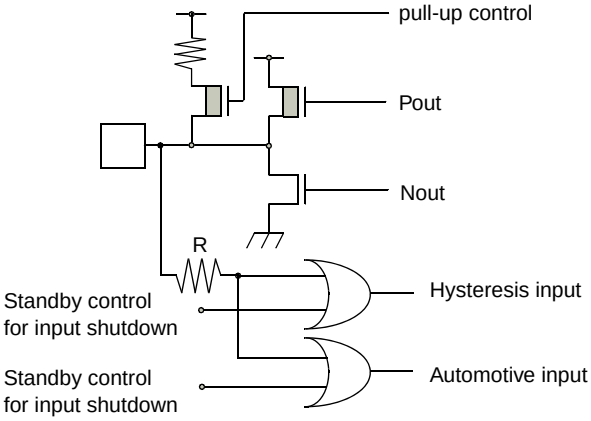
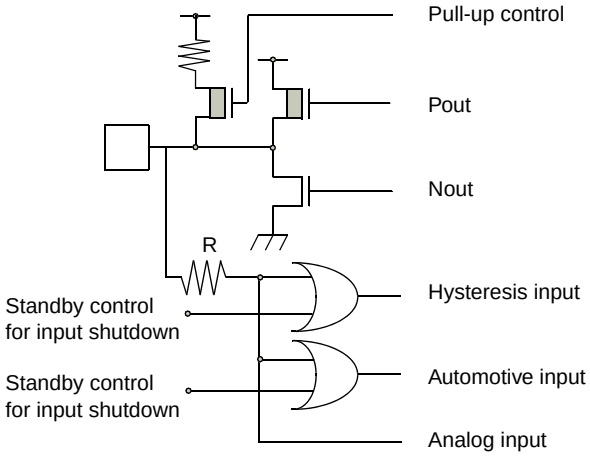
Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output

Pin Function description (2 of 2)

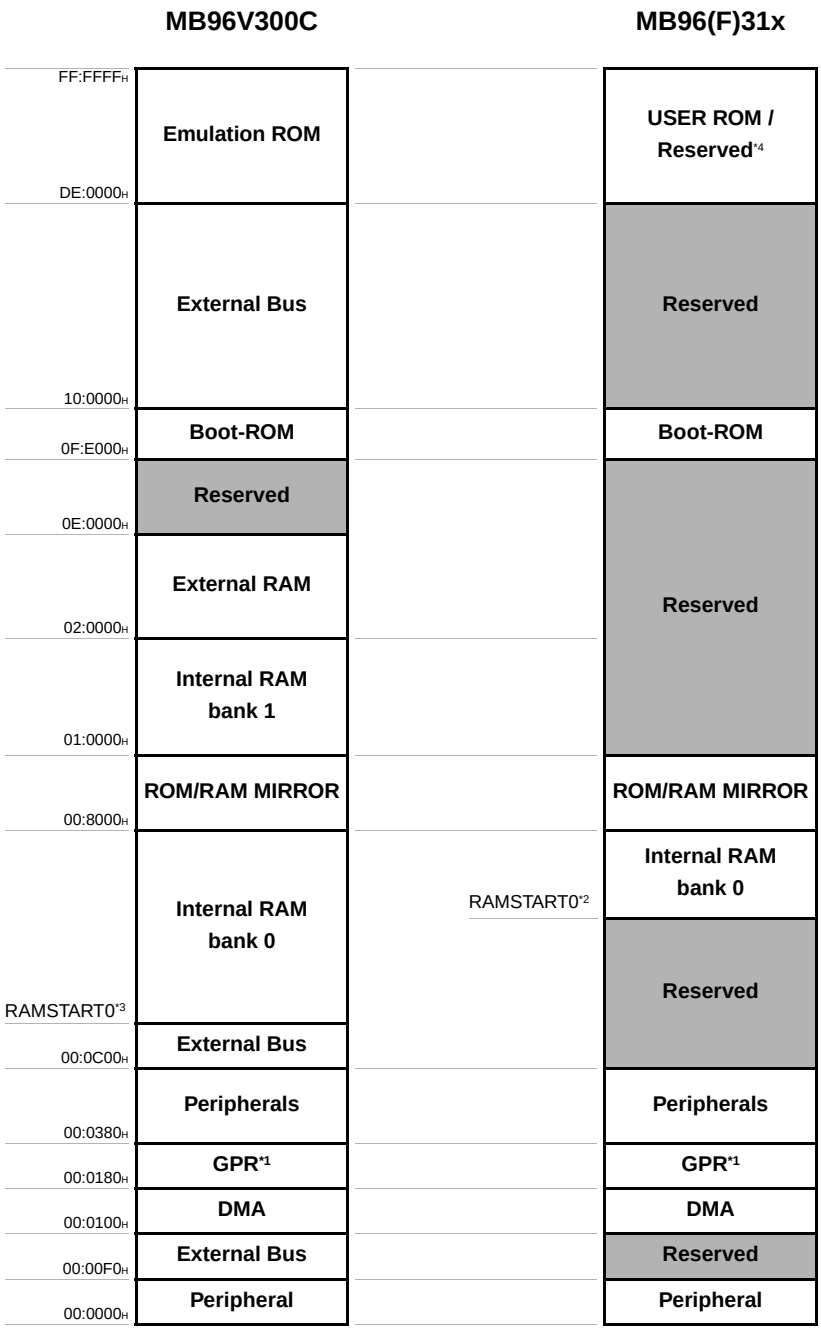
Pin name	Feature	Description
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx.
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • CMOS hysteresis input with input shutdown function • Automotive input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. • Analog input

■ MEMORY MAP



*1: Unused GPR banks can be used as RAM area

*2: For RAMSTART0 addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the ■ USER ROM MEMORY MAP FOR FLASH DEVICES on the following pages.

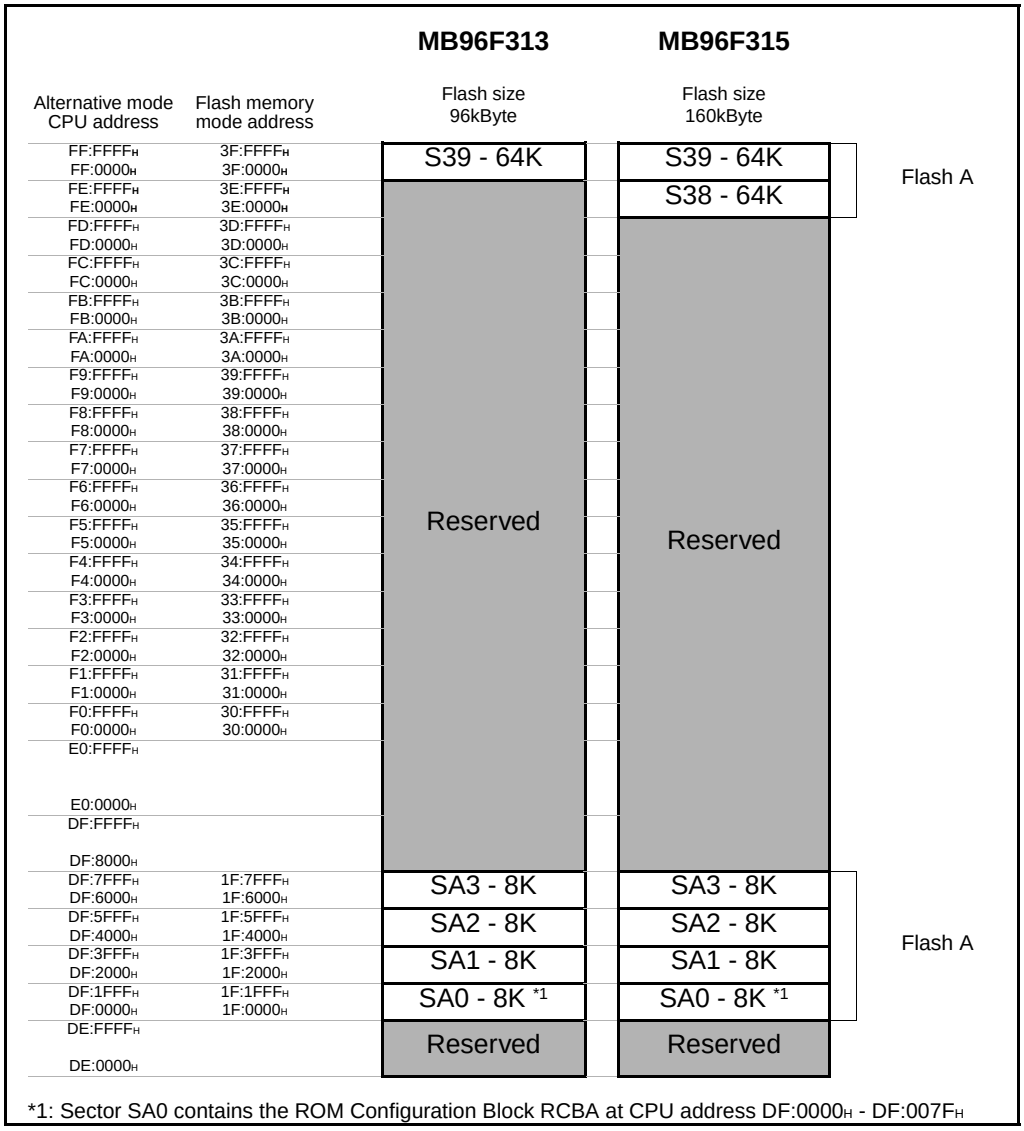
The DMA area is only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAMSTART ADDRESSES

Devices	RAM size	RAMSTART0
MB96F313/F315	8KByte	00:6240$_H$

■ USER ROM MEMORY MAP FOR FLASH DEVICES



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F31x		
Pin number	USART Number	Normal function
LQFP-48		
7	USART2	SIN2
8		SOT2
9		SCK2
20	USART7	SIN7_R
19		SOT7_R
18		SCK7_R
22	USART8	SIN8_R
21		SOT8_R
23		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Fujitsu suggests to the tool vendor to support at least port P00_1 on pin 19.
If handshaking is used by the tool but P00_1 is not available in customer's application, Fujitsu suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

I/O map MB96(F)315x (2 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000028H-000039H	Reserved			-
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H - 00004BH	Reserved			-
00004CH	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004DH	ICU4/ICU5 - Edge register	ICE45		R/W
00004EH	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004FH	ICU4 - Capture Register High	IPCPH4		R
000050H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051H	ICU5 - Capture Register High	IPCPH5		R
000052H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053H	ICU6/ICU7 - Edge register	ICE67		R/W
000054H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055H	ICU6 - Capture Register High	IPCPH6		R
000056H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057H	ICU7 - Capture Register High	IPCPH7		R
000058H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W

I/O map MB96(F)315x (3 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00005A$_H$	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B$_H$	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005C$_H$	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005D$_H$	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
00005E$_H$	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005F$_H$	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060$_H$	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061$_H$	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062$_H$	RLT0 - Reload Register - for writing		TMRLR0	W
000062$_H$	RLT0 - Reload Register - for reading		TMR0	R
000063$_H$	RLT0 - Reload Register - for writing			W
000063$_H$	RLT0 - Reload Register - for reading			R
000064$_H$	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065$_H$	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066$_H$	RLT1 - Reload Register - for writing		TMRLR1	W
000066$_H$	RLT1 - Reload Register - for reading		TMR1	R
000067$_H$	RLT1 - Reload Register - for writing			W
000067$_H$	RLT1 - Reload Register - for reading			R
000068$_H$	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069$_H$	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006A$_H$	RLT2 - Reload Register - for writing		TMRLR2	W
00006A$_H$	RLT2 - Reload Register - for reading		TMR2	R
00006B$_H$	RLT2 - Reload Register - for writing			W
00006B$_H$	RLT2 - Reload Register - for reading			R
00006C$_H$	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D$_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E$_H$	RLT3 - Reload Register - for writing		TMRLR3	W
00006E$_H$	RLT3 - Reload Register - for reading		TMR3	R
00006F$_H$	RLT3 - Reload Register - for writing			W

I/O map MB96(F)315x (4 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006F$_H$	RLT3 - Reload Register - for reading			R
000070$_H$	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071$_H$	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074$_H$	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075$_H$	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076$_H$	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077$_H$	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078$_H$	PPG0 - Timer register		PTMR0	R
000079$_H$	PPG0 - Timer register			R
00007A$_H$	PPG0 - Period setting register		PCSR0	W
00007B$_H$	PPG0 - Period setting register			W
00007C$_H$	PPG0 - Duty cycle register		PDUT0	W
00007D$_H$	PPG0 - Duty cycle register			W
00007E$_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F$_H$	PPG0 - Control status register High	PCNH0		R/W
000080$_H$	PPG1 - Timer register		PTMR1	R
000081$_H$	PPG1 - Timer register			R
000082$_H$	PPG1 - Period setting register		PCSR1	W
000083$_H$	PPG1 - Period setting register			W
000084$_H$	PPG1 - Duty cycle register		PDUT1	W
000085$_H$	PPG1 - Duty cycle register			W
000086$_H$	PPG1 - Control status register Low	PCNL1	PCN1	R/W

I/O map MB96(F)315x (5 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000087H	PPG1 - Control status register High	PCNH1		R/W
000088H-00008FH	Reserved			-
000090H	PPG3 - Timer register		PTMR3	R
000091H	PPG3 - Timer register			R
000092H	PPG3 - Period setting register		PCSR3	W
000093H	PPG3 - Period setting register			W
000094H	PPG3 - Duty cycle register		PDUT3	W
000095H	PPG3 - Duty cycle register			W
000096H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097H	PPG3 - Control status register High	PCNH3		R/W
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009CH	PPG4 - Timer register		PTMR4	R
00009DH	PPG4 - Timer register			R
00009EH	PPG4 - Period setting register		PCSR4	W
00009FH	PPG4 - Period setting register			W
0000A0H	PPG4 - Duty cycle register		PDUT4	W
0000A1H	PPG4 - Duty cycle register			W
0000A2H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3H	PPG4 - Control status register High	PCNH4		R/W
0000A4H-0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DDH-0000FFH	Reserved			-
000100H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103H	DMA0 - DMA control register	DMACS0		R/W
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107H	DMA0 - Data counter high byte	DCTH0		R/W
000108H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010AH	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010BH	DMA1 - DMA control register	DMACS1		R/W
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010DH	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010FH	DMA1 - Data counter high byte	DCTH1		R/W
000110H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113H	DMA2 - DMA control register	DMACS2		R/W
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117H	DMA2 - Data counter high byte	DCTH2		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000118H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011AH	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011BH	DMA3 - DMA control register	DMACS3		R/W
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011DH	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011FH	DMA3 - Data counter high byte	DCTH3		R/W
000120H-00017FH	Reserved			-
000180H-00037FH	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380H	DMA0 - Interrupt select	DISEL0		R/W
000381H	DMA1 - Interrupt select	DISEL1		R/W
000382H	DMA2 - Interrupt select	DISEL2		R/W
000383H	DMA3 - Interrupt select	DISEL3		R/W
000384H-00038FH	Reserved			-
000390H	DMA - Status register low byte	DSRL	DSR	R/W
000391H	DMA - Status register high byte	DSRH		R/W
000392H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393H	DMA - Stop status register high byte	DSSRH		R/W
000394H	DMA - Enable register low byte	DERL	DER	R/W
000395H	DMA - Enable register high byte	DERH		R/W
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	R/W
0003A1H	Interrupt index register	IDX		R/W
0003A2H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3H	Interrupt vector table base register High	TBRH		R/W
0003A4H	Delayed Interrupt register	DIRR		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003A5H	Non Maskable Interrupt register	NMI		R/W
0003A6H-0003ABH	Reserved			-
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003ADH	EDSU communication interrupt selection High	EDSU2H		R/W
0003AEH	ROM mirror control register	ROMM		R/W
0003AFH	EDSU configuration register	EDSU		R/W
0003B0H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1H	Memory patch control/status register ch 0/1			R/W
0003B2H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3H	Memory patch control/status register ch 2/3			R/W
0003B4H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5H	Memory patch control/status register ch 4/5			R/W
0003B6H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7H	Memory patch control/status register ch 6/7			R/W
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		R/W
0003BDH	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BEH	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0H	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1H	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2H	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3H	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4H	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5H	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6H	Memory Patch function - Patch address 4 high	PFAH4		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003C7H	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8H	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9H	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CAH	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CBH	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CCH	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CDH	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CEH	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CFH	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1H	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3H	Memory Patch function - Patch data 1 High	PFDH1		R/W
0003D4H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
0003D5H	Memory Patch function - Patch data 2 High	PFDH2		R/W
0003D6H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7H	Memory Patch function - Patch data 3 High	PFDH3		R/W
0003D8H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
0003D9H	Memory Patch function - Patch data 4 High	PFDH4		R/W
0003DAH	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
0003DBH	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DCH	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DDH	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DEH	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DFH	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0H-0003F0H	Reserved			-
0003F1H	Memory Control Status Register A	MCSRA		R/W
0003F2H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3H	Memory Timing Configuration Register A High	MTCRAH		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003F4H-0003F8H	Reserved			-
0003F9H	Flash Memory Write Control register 1	FMWC1		R/W
0003FAH	Flash Memory Write Control register 2	FMWC2		R/W
0003FBH	Flash Memory Write Control register 3	FMWC3		R/W
0003FCH	Flash Memory Write Control register 4	FMWC4		R/W
0003FDH	Flash Memory Write Control register 5	FMWC5		R/W
0003FEH-0003FFH	Reserved			-
000400H	Standby Mode control register	SMCR		R/W
000401H	Clock select register	CKSR		R/W
000402H	Clock Stabilization select register	CKSSR		R/W
000403H	Clock monitor register	CKMR		R
000404H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405H	Clock Frequency control register High	CKFCRH		R/W
000406H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407H	PLL Control register High	PLLCRH		R/W
000408H	RC clock timer control register	RCTCR		R/W
000409H	Main clock timer control register	MCTCR		R/W
00040AH	Sub clock timer control register	SCTCR		R/W
00040BH	Reset cause and clock status register with clear function	RCCSRC		R
00040CH	Reset configuration register	RCR		R/W
00040DH	Reset cause and clock status register	RCCSR		R
00040EH	Watch dog timer configuration register	WDTC		R/W
00040FH	Watch dog timer clear pattern register	WDTCP		W
000410H-000414H	Reserved			-
000415H	Clock output activation register	COAR		R/W
000416H	Clock output configuration register 0	COCR0		R/W
000417H	Clock output configuration register 1	COCR1		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000418H	Clock Modulator control register	CMCR		R/W
000419H	Reserved			-
00041AH	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041BH	Clock Modulator Parameter register High	CMPRH		R/W
00041CH-00042BH	Reserved			-
00042CH	Voltage Regulator Control register	VRCR		R/W
00042DH	Clock Input and LVD Control Register	CILCR		R/W
00042EH-00042FH	Reserved			-
000430H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434H	Reserved			-
000435H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438H-000443H	Reserved			-
000444H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448H	Reserved			-
000449H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044AH	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044BH	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044CH-000457H	Reserved			-
000458H	I/O Port P00 - Port Input Level Register	PILR00		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000459H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045AH	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045BH	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045CH	Reserved			-
00045DH	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045EH	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045FH	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460H-00046BH	Reserved			-
00046CH	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046DH	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046EH	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046FH	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470H	Reserved			-
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474H-00047FH	Reserved			-
000480H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484H	Reserved			-
000485H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488H-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004AA$_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004AB$_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004AC$_H$	Reserved			-
0004AD$_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AE$_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AF$_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0$_H$-0004BB$_H$	Reserved			-
0004BC$_H$	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD$_H$	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE$_H$	I/O Port P02 - External Pin State Register	EPSR02		R
0004BF$_H$	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0$_H$	Reserved			-
0004C1$_H$	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2$_H$	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3$_H$	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4$_H$-0004CF$_H$	Reserved			-
0004D0$_H$	ADC analog input enable register 0	ADER0		R/W
0004D1$_H$	ADC analog input enable register 1	ADER1		R/W
0004D2$_H$	ADC analog input enable register 2	ADER2		R/W
0004D3$_H$	ADC analog input enable register 3	ADER3		R/W
0004D4$_H$	ADC analog input enable register 4	ADER4		R/W
0004D5$_H$	Reserved			-
0004D6$_H$	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7$_H$	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8$_H$	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9$_H$	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA$_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB$_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC$_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004DD$_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE$_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF$_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0$_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1$_H$	RTC - Sub Second Register M	WTBRH0		R/W
0004E2$_H$	RTC - Sub-Second Register H	WTBR1		R/W
0004E3$_H$	RTC - Second Register	WTSR		R/W
0004E4$_H$	RTC - Minutes	WTMR		R/W
0004E5$_H$	RTC - Hour	WTHR		R/W
0004E6$_H$	RTC - Timer Control Extended Register	WTCER		R/W
0004E7$_H$	RTC - Clock select register	WTCKSR		R/W
0004E8$_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9$_H$	RTC - Timer Control Register High	WTCRH		R/W
0004EA$_H$	CAL - Calibration unit Control register	CUCR		R/W
0004EB$_H$	Reserved			-
0004EC$_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED$_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE$_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF$_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0$_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1$_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2$_H$-0004F9$_H$	Reserved			-
0004FA$_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB$_H$-0004FF$_H$	Reserved			-
000500$_H$	FRT2 - Data register of free-running timer		TCDT2	R/W
000501$_H$	FRT2 - Data register of free-running timer			R/W
000502$_H$	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000503H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505H	FRT3 - Data register of free-running timer			R/W
000506H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508H-000513H	Reserved			-
000514H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517H	ICU8 - Capture Register High	IPCPH8		R
000518H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519H	ICU9 - Capture Register High	IPCPH9		R
00051AH	ICU10/ICU11 - Control Status Register	ICS1011		R/W
00051BH	ICU10/ICU11 - Edge Register	ICE1011		R/W
00051CH	ICU10 - Capture Register Low	IPCPL10	IPCP10	R
00051DH	ICU10 - Capture Register High	IPCPH10		R
00051EH	ICU11 - Capture Register Low	IPCPL11	IPCP11	R
00051FH	ICU11 - Capture Register High	IPCPH11		R
000520H-00053DH	Reserved			-
00053EH	USART7 - Serial Mode Register	SMR7		R/W
00053FH	USART7 - Serial Control Register	SCR7		R/W
000540H	USART7 - Serial TX Register	TDR7		W
000540H	USART7 - Serial RX Register	RDR7		R
000541H	USART7 - Serial Status Register	SSR7		R/W
000542H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000545H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547H	Reserved			-
000548H	USART8 - Serial Mode Register	SMR8		R/W
000549H	USART8 - Serial Control Register	SCR8		R/W
00054AH	USART8 - Serial TX Register	TDR8		W
00054AH	USART8 - Serial RX Register	RDR8		R
00054BH	USART8 - Serial Status Register	SSR8		R/W
00054CH	USART8 - Ext. Control/Com. Register	ECCR8		R/W
00054DH	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054EH	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054FH	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551H-000563H	Reserved			-
000564H	PPG6 - Timer register		PTMR6	R
000565H	PPG6 - Timer register			R
000566H	PPG6 - Period setting register		PCSR6	W
000567H	PPG6 - Period setting register			W
000568H	PPG6 - Duty cycle register		PDUT6	W
000569H	PPG6 - Duty cycle register			W
00056AH	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056BH	PPG6 - Control status register High	PCNH6		R/W
00056CH	PPG7 - Timer register		PTMR7	R
00056DH	PPG7 - Timer register			R
00056EH	PPG7 - Period setting register		PCSR7	W
00056FH	PPG7 - Period setting register			W
000570H	PPG7 - Duty cycle register		PDUT7	W
000571H	PPG7 - Duty cycle register			W
000572H	PPG7 - Control status register Low	PCNL7	PCN7	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000573H	PPG7 - Control status register High	PCNH7		R/W
000574H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578H	PPG8 - Timer register		PTMR8	R
000579H	PPG8 - Timer register			R
00057AH	PPG8 - Period setting register		PCSR8	W
00057BH	PPG8 - Period setting register			W
00057CH	PPG8 - Duty cycle register		PDUT8	W
00057DH	PPG8 - Duty cycle register			W
00057EH	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057FH	PPG8 - Control status register High	PCNH8		R/W
000580H	PPG9 - Timer register		PTMR9	R
000581H	PPG9 - Timer register			R
000582H	PPG9 - Period setting register		PCSR9	W
000583H	PPG9 - Period setting register			W
000584H	PPG9 - Duty cycle register		PDUT9	W
000585H	PPG9 - Duty cycle register			W
000586H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587H	PPG9 - Control status register High	PCNH9		R/W
000588H-000597H	Reserved			-
000598H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059AH	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059BH	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059CH	PPG12 - Timer register		PTMR12	R
00059DH	PPG12 - Timer register			R
00059EH	PPG12 - Period setting register		PCSR12	W

I/O map MB96(F)315x (19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005CA$_H$	PPG17 - Period setting register		PCSR17	W
0005CB$_H$	PPG17 - Period setting register			W
0005CC$_H$	PPG17 - Duty cycle register		PDUT17	W
0005CD$_H$	PPG17 - Duty cycle register			W
0005CE$_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF$_H$	PPG17 - Control status register High	PCNH17		R/W
0005D0$_H$	PPG18 - Timer register		PTMR18	R
0005D1$_H$	PPG18 - Timer register			R
0005D2$_H$	PPG18 - Period setting register		PCSR18	W
0005D3$_H$	PPG18 - Period setting register			W
0005D4$_H$	PPG18 - Duty cycle register		PDUT18	W
0005D5$_H$	PPG18 - Duty cycle register			W
0005D6$_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7$_H$	PPG18 - Control status register High	PCNH18		R/W
0005D8$_H$	PPG19 - Timer register		PTMR19	R
0005D9$_H$	PPG19 - Timer register			R
0005DA$_H$	PPG19 - Period setting register		PCSR19	W
0005DB$_H$	PPG19 - Period setting register			W
0005DC$_H$	PPG19 - Duty cycle register		PDUT19	W
0005DD$_H$	PPG19 - Duty cycle register			W
0005DE$_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF$_H$	PPG19 - Control status register High	PCNH19		R/W
0005E0$_H$-00065F$_H$	Reserved			-
000660$_H$	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661$_H$	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662$_H$	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663$_H$	Peripheral Resource Relocation Register 13	PRRR13		W
000664$_H$-0008FF$_H$	Reserved			-
000900$_H$	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W

I/O map MB96(F)315x (20 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000901H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903H	CAN2 - Status register High (reserved)	STATRH2		R
000904H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R
000909H	CAN2 - Interrupt Register High	INTRH2		R
00090AH	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090BH	CAN2 - Test Register High (reserved)	TESTRH2		R
00090CH	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090DH	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090EH-00090FH	Reserved			-
000910H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W
000918H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
00091AH	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
00091BH	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
00091CH	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
00091DH	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
00091EH	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W

I/O map MB96(F)315x (21 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00091F$_H$	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920$_H$	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921$_H$	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922$_H$	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923$_H$	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924$_H$	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925$_H$	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W
000926$_H$-00093F$_H$	Reserved			-
000940$_H$	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	R/W
000941$_H$	CAN2 - IF2 Command request register High	IF2CREQH2		R/W
000942$_H$	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	R/W
000943$_H$	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944$_H$	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	R/W
000945$_H$	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		R/W
000946$_H$	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	R/W
000947$_H$	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		R/W
000948$_H$	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	R/W
000949$_H$	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		R/W
00094A$_H$	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	R/W
00094B$_H$	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		R/W
00094C$_H$	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	R/W
00094D$_H$	CAN2 - IF2 Message Control Register High	IF2MCTRH2		R/W
00094E$_H$	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	R/W
00094F$_H$	CAN2 - IF2 Data A1 High	IF2DTA1H2		R/W
000950$_H$	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	R/W
000951$_H$	CAN2 - IF2 Data A2 High	IF2DTA2H2		R/W
000952$_H$	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	R/W
000953$_H$	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954$_H$	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W

I/O map MB96(F)315x (4 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006F$_H$	RLT3 - Reload Register - for reading			R
000070$_H$	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071$_H$	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074$_H$	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075$_H$	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076$_H$	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077$_H$	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078$_H$	PPG0 - Timer register		PTMR0	R
000079$_H$	PPG0 - Timer register			R
00007A$_H$	PPG0 - Period setting register		PCSR0	W
00007B$_H$	PPG0 - Period setting register			W
00007C$_H$	PPG0 - Duty cycle register		PDUT0	W
00007D$_H$	PPG0 - Duty cycle register			W
00007E$_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F$_H$	PPG0 - Control status register High	PCNH0		R/W
000080$_H$	PPG1 - Timer register		PTMR1	R
000081$_H$	PPG1 - Timer register			R
000082$_H$	PPG1 - Period setting register		PCSR1	W
000083$_H$	PPG1 - Period setting register			W
000084$_H$	PPG1 - Duty cycle register		PDUT1	W
000085$_H$	PPG1 - Duty cycle register			W
000086$_H$	PPG1 - Control status register Low	PCNL1	PCN1	R/W

Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

■ INTERRUPT VECTOR TABLE

Interrupt vector table MB96(F)31x (1 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC$_H$	CALLV0	No	-	
1	3F8$_H$	CALLV1	No	-	
2	3F4$_H$	CALLV2	No	-	
3	3F0$_H$	CALLV3	No	-	
4	3EC$_H$	CALLV4	No	-	
5	3E8$_H$	CALLV5	No	-	
6	3E4$_H$	CALLV6	No	-	
7	3E0$_H$	CALLV7	No	-	
8	3DC$_H$	RESET	No	-	
9	3D8$_H$	INT9	No	-	
10	3D4$_H$	EXCEPTION	No	-	
11	3D0$_H$	NMI	No	-	Non-Maskable Interrupt
12	3CC$_H$	DLY	No	12	Delayed Interrupt
13	3C8$_H$	RC_TIMER	No	13	RC Timer
14	3C4$_H$	MC_TIMER	No	14	Main Clock Timer
15	3C0$_H$	SC_TIMER	No	15	Sub Clock Timer
16	3BC$_H$	PLL_UNLOCK	No	16	Reserved
17	3B8$_H$	EXTINT0	Yes	17	External Interrupt 0
18	3B4$_H$				Reserved
19	3B0$_H$	EXTINT2	Yes	19	External Interrupt 2
20	3AC$_H$	EXTINT3	Yes	20	External Interrupt 3
21	3A8$_H$	EXTINT4	Yes	21	External Interrupt 4
22	3A4$_H$				Reserved
23	3A0$_H$	EXTINT7	Yes	23	External Interrupt 7
24	39C$_H$	EXTINT8	Yes	24	External Interrupt 8
25	398$_H$	EXTINT9	Yes	25	External Interrupt 9
26	394$_H$	EXTINT10	Yes	26	External Interrupt 10
27	390$_H$	EXTINT11	Yes	27	External Interrupt 11
28	38C$_H$	EXTINT12	Yes	28	External Interrupt 12
29	388$_H$	EXTINT13	Yes	29	External Interrupt 13
30	384$_H$				Reserved

Interrupt vector table MB96(F)31x (2 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
31	380H				Reserved
32	37CH				Reserved
33	378H	CAN2	No	33	CAN Controller 2
34	374H	PPG0	Yes	34	Programmable Pulse Generator 0
35	370H	PPG1	Yes	35	Programmable Pulse Generator 1
36	36CH				Reserved
37	368H	PPG3	Yes	37	Programmable Pulse Generator 3
38	364H	PPG4	Yes	38	Programmable Pulse Generator 4
39	360				Reserved
40	35CH	PPG6	Yes	40	Programmable Pulse Generator 6
41	358H	PPG7	Yes	41	Programmable Pulse Generator 7
42	354H	PPG8	Yes	42	Programmable Pulse Generator 8
43	350H	PPG9	Yes	43	Programmable Pulse Generator 9
44	34CH				Reserved
45	348H				Reserved
46	344H	PPG12	Yes	46	Programmable Pulse Generator 12
47	340H				Reserved
48	33CH	PPG14	Yes	48	Programmable Pulse Generator 14
49	338H				Reserved
50	334H	PPG16	Yes	50	Programmable Pulse Generator 16
51	330H	PPG17	Yes	51	Programmable Pulse Generator 17
52	32CH	PPG18	Yes	52	Programmable Pulse Generator 18
53	328H	PPG19	Yes	53	Programmable Pulse Generator 19
54	324H	RLT0	Yes	54	Reload Timer 0
55	320H	RLT1	Yes	55	Reload Timer 1
56	31CH	RLT2	Yes	56	Reload Timer 2
57	318H	RLT3	Yes	57	Reload Timer 3
58	314H	PPGRLT	Yes	58	Reload Timer 6 - dedicated for PPG
59	310H	ICU0	Yes	59	Input Capture Unit 0
60	30CH	ICU1	Yes	60	Input Capture Unit 1
61	308H				Reserved
62	304H				Reserved
63	300H	ICU4	Yes	63	Input Capture Unit 4
64	2FCH	ICU5	Yes	64	Input Capture Unit 5
65	2F8H	ICU6	Yes	65	Input Capture Unit 6

Interrupt vector table MB96(F)31x (3 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
66	$2F4_H$				Reserved
67	$2F0_H$				Reserved
68	$2EC_H$	ICU9	Yes	68	Input Capture Unit 9
69	$2E8_H$	ICU10	Yes	69	Input Capture Unit 10
70	$2E4_H$				Reserved
71	$2E0_H$				Reserved
72	$2DC_H$				Reserved
73	$2D8_H$	OCU6	Yes	73	Output Compare Unit 6
74	$2D4_H$	OCU7	Yes	74	Output Compare Unit 7
75	$2D0_H$				Reserved
76	$2CC_H$				Reserved
77	$2C8_H$	FRT0	Yes	77	Free Running Timer 0
78	$2C4_H$	FRT1	Yes	78	Free Running Timer 1
79	$2C0_H$	FRT2	Yes	79	Free Running Timer 2
80	$2BC_H$	FRT3	Yes	80	Free Running Timer 3
81	$2B8_H$	RTC0	No	81	Real Timer Clock
82	$2B4_H$	CAL0	No	82	Clock Calibration Unit
83	$2B0_H$				Reserved
84	$2AC_H$	ADC0	Yes	84	A/D Converter
85	$2A8_H$	LINR2	Yes	85	LIN USART 2 RX
86	$2A4_H$	LINT2	Yes	86	LIN USART 2 TX
87	$2A0_H$				Reserved
88	$29C_H$				Reserved
89	298_H	LINR7	Yes	89	LIN USART 7 RX
90	294_H	LINT7	Yes	90	LIN USART 7 TX
91	290_H	LINR8	Yes	91	LIN USART 8 RX
92	$28C_H$	LINT8	Yes	92	LIN USART 8 TX
93	288_H	FLASH_A	No	93	Flash memory A (only Flash devices)

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

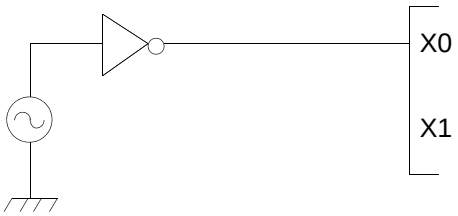
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

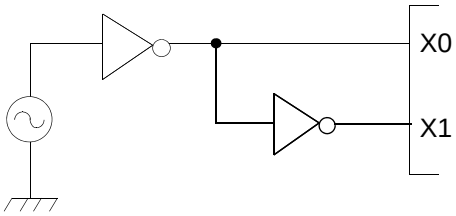
1. Single phase external clock

- When using a single phase external clock, X0 (X0A) pin must be driven and X1 (X1A) pin left open.



2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

12. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

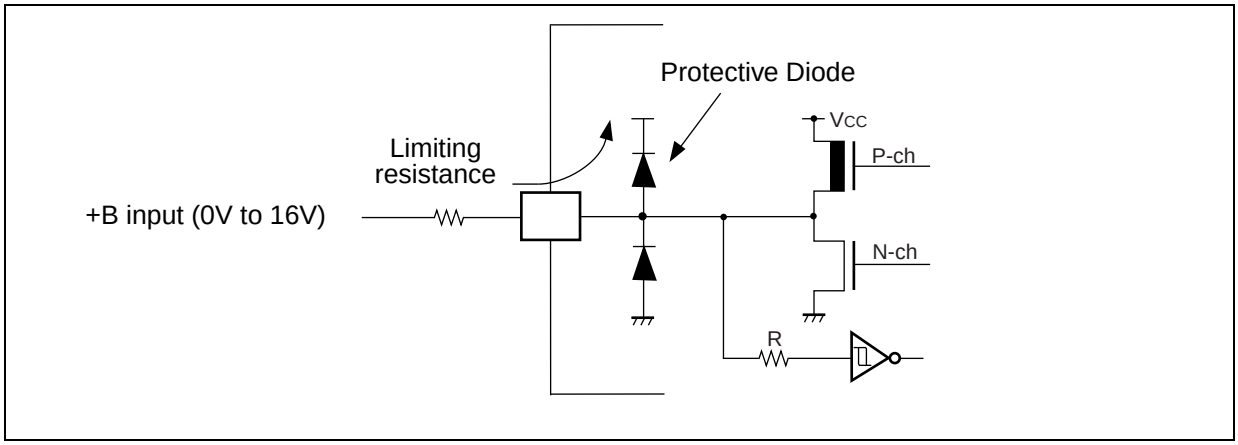
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *1
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V *2
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V *2
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purpose I/O pins *3
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices) *4	P_D	-	220*5	mW	T_A=105°C
		-	450*5	mW	T_A=85°C
		-	615*5	mW	T_A=70°C
		-	280*5	mW	T_A=125°C, no Flash program/ erase *6
		-	500*5	mW	T_A=105°C, no Flash program/ erase *6
Operating ambient temperature	T_A	0	+70	°C	MB96V300C
		-40	+105		
		-40	+125		*6
Storage temperature	T_{STG}	-55	+150	°C	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:
- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “3. DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7	15	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC characteristics

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -2mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA (PODR:OD=1)
	V_{OH5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -5mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA (PODR:OD=0)

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA (PODR:OD=1)
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA (PODR:OD=0)
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	µA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	V_{CC} = 3.3V ± 10%	40	100	160	kΩ	
			V_{CC} = 5.0V ± 10%	25	50	100	kΩ	

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 16MHz, CLKP2 = 8MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped)	+25°C	14.5	19.5	mA	
			+125°C	16	23		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1 = 32MHz, CLKP2 = 16MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25°C	23	29	mA	
			+125°C	25	33		
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz 0 Flash/ROM wait states (CLKRC and CLKSC stopped)	+25°C	26	38	mA	
			+125°C	28	42		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz 2 Flash/ROM wait states (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	40	51	mA	
			+125°C	42	55		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz 1 Flash/ROM wait state (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	43	56	mA	
			+125°C	45	60		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Run modes*	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz 1 Flash/ROM wait state (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4	5	mA	
			+125°C	4.7	8		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.5	3.5	mA	
			+125°C	3.2	6.5		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.18	0.3	mA	
			+125°C	0.73	3.1		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.15	0.25	mA	
			+125°C	0.7	3.05		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz 1 Flash/ROM wait state (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	
			+125°C	0.65	3		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = CLKP1 = 16MHz, CLKP2 = 8MHz (CLKRC and CLKSC stopped)	+25°C	4	6	mA	
			+125°C	4.7	9		
		PLL Sleep mode with CLKS1/2 = CLKP1 = 32MHz, CLKP2 = 16MHz (CLKRC and CLKSC stopped)	+25°C	7	9.5	mA	
			+125°C	8	12.5		
		PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped)	+25°C	7	9	mA	
			+125°C	8	12		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	11	14.5	mA	
			+125°C	12	17.5		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	12	15	mA	
			+125°C	13	18		
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1	1.3	mA	
			+125°C	1.6	4.1		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.55	1.1	mA	
			+125°C	1.15	3.9		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Sleep modes*	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.08	0.2	mA	
			+125°C	0.59	2.95		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.15	mA	
			+125°C	0.56	2.9		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	
			+125°C	0.54	2.9		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped)	+25°C	1.3	1.8	mA	
			+125°C	1.9	4.8		
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.11	0.2	mA	
			+125°C	0.63	3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.08	0.15	mA	
			+125°C	0.6	2.9		

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Power supply current in Timer modes*	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.1	0.2	mA	
			+125°C	0.63	3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.07	0.15	mA	
			+125°C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.06	0.15	mA	
			+125°C	0.56	2.95		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.03	0.1	mA	
			+125°C	0.53	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.035	0.1	mA	
			+125°C	0.53	2.85		
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	
			+125°C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	
			+125°C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	+25°C	5	10	µA	Must be added to all current above
			+125°C	7	20		
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value		Unit	Remarks
				Typ	Max		
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

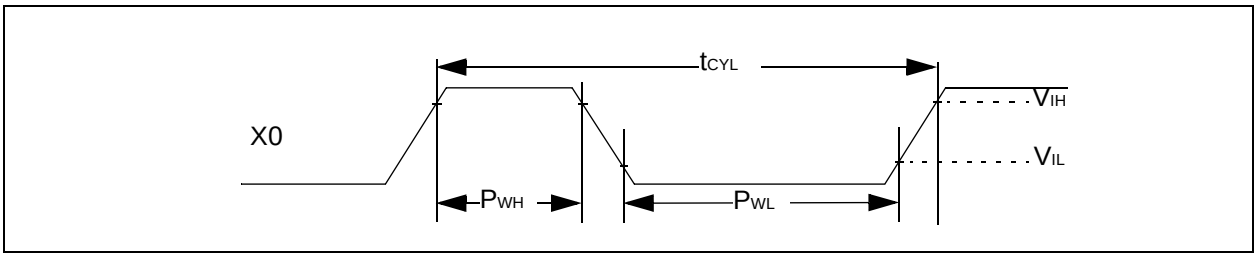
* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

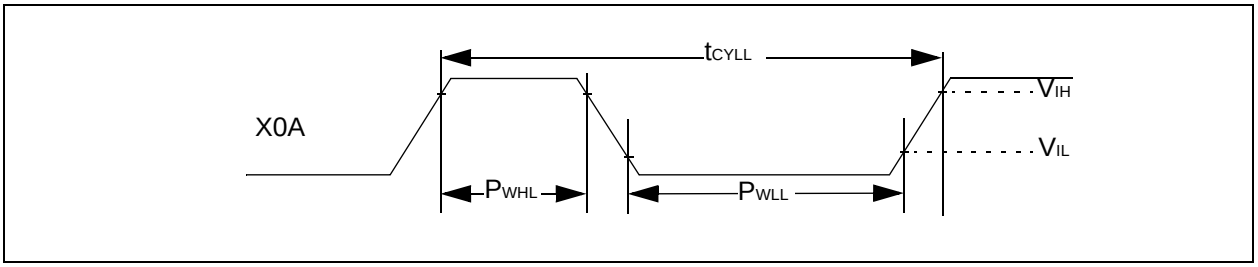
4. AC Characteristics

Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	-	256 RC clock cycles				Applied after any reset and when activating the RC oscillator.
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz, jitter coming from external oscillator, crystal or resonator is not covered
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	


tCYL
X0
VIH
VIL
PWH
PWL


tCYLL
X0A
VIH
VIL
PWHL
PWLL

Internal Clock timing

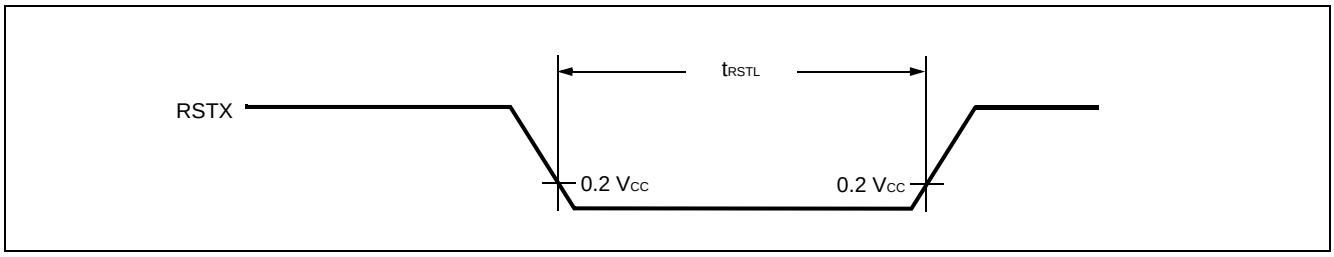
(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

External Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

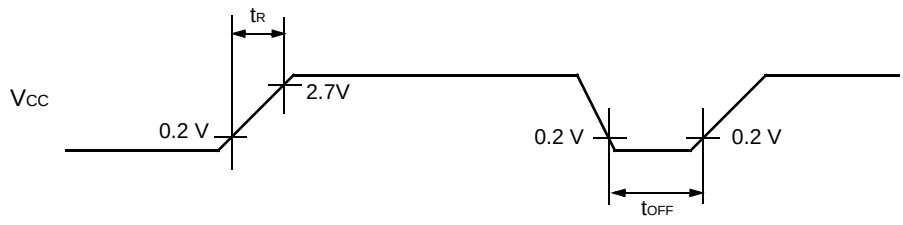
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



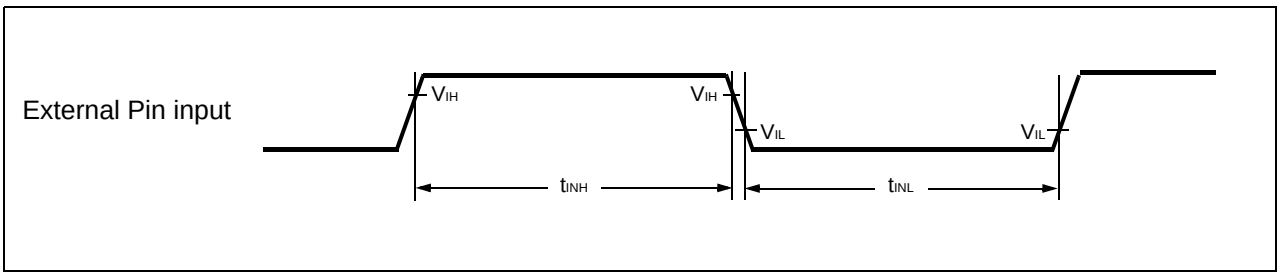
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

External Input timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 (t_{CLKP1}=1/ f_{CLKP1})	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG_R					AD Converter Trigger
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics



USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

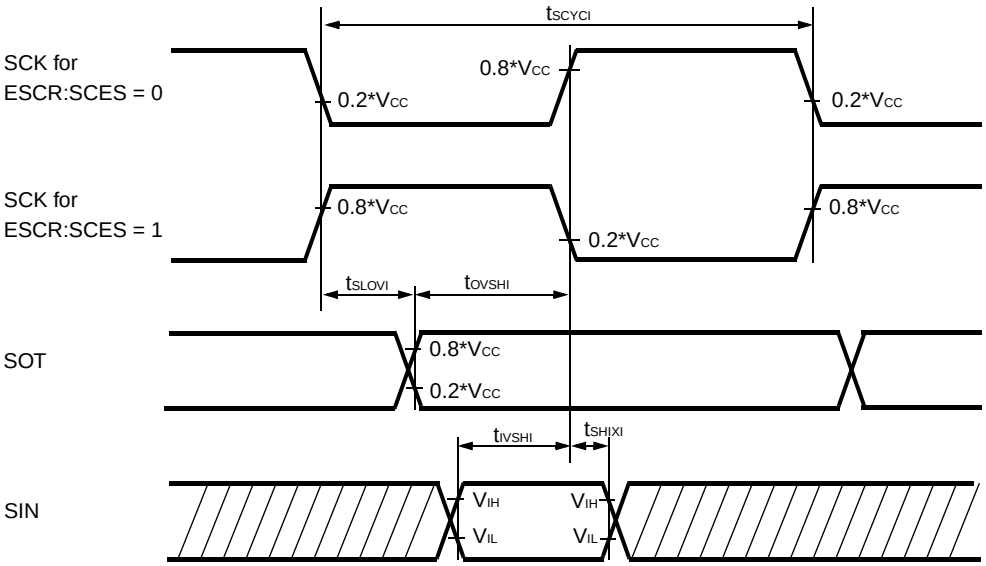
Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 *1	—	$N*t_{CLKP1}$ - 30 *1	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”.
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

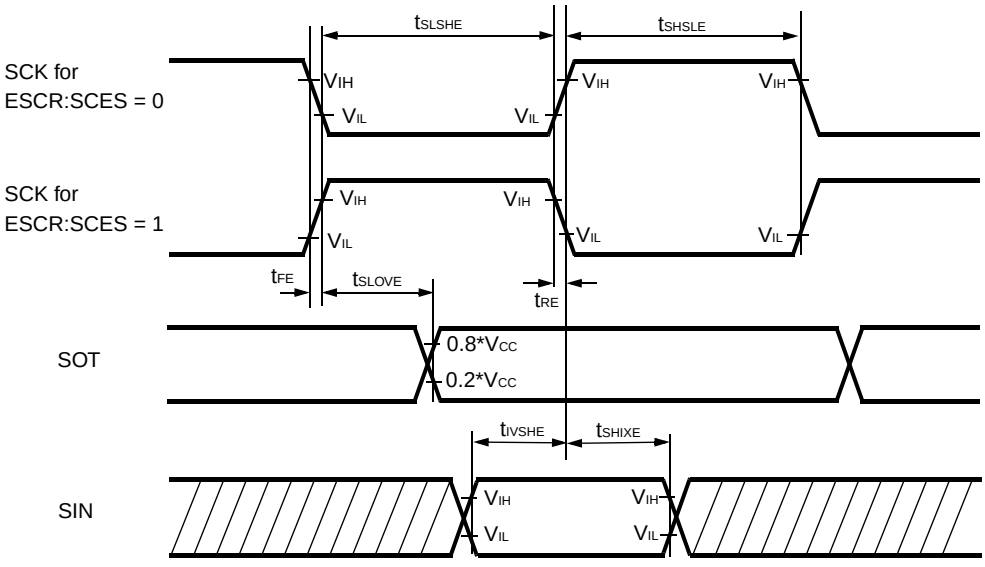
*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...



Internal Shift Clock Mode



External Shift Clock Mode

5. Analog Digital Converter

(T_A = -40 °C to +125 °C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-	-	± 3	LSB	
Nonlinearity error	-	-	-	-	± 2.5	LSB	
Differential nonlinearity error	-	-	-	-	± 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	AVRL - 1.5 LSB	AVRL+ 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale transition voltage	V_{FST}	ANn	AVRH - 3.5 LSB	AVRH - 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog input leakage current (during conversion)	I_{AIN}	ANn	-1	-	+1	µA	T_A ≤ 105 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-1.2	-	+1.2	µA	105 °C < T_A ≤ 125 °C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

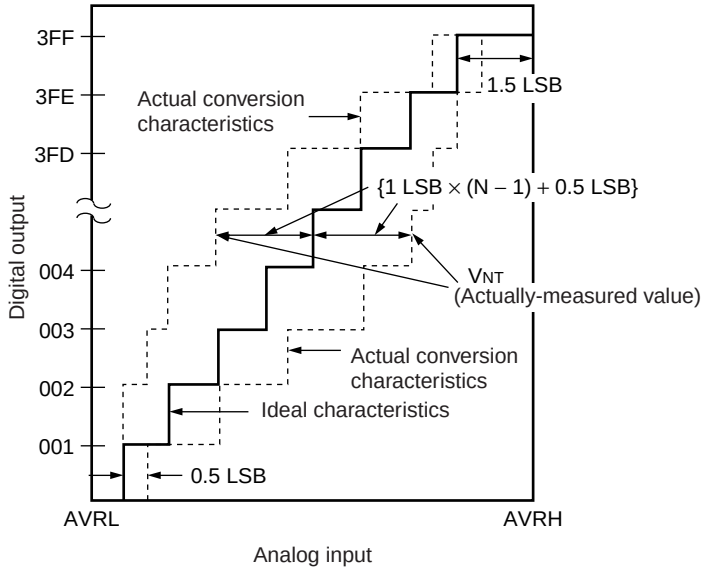
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

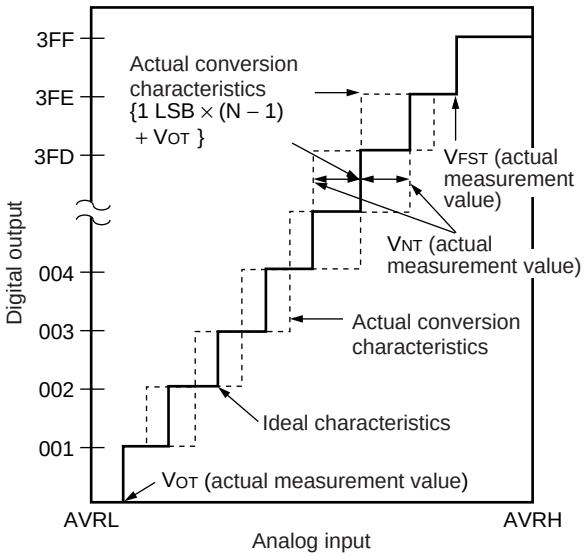
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

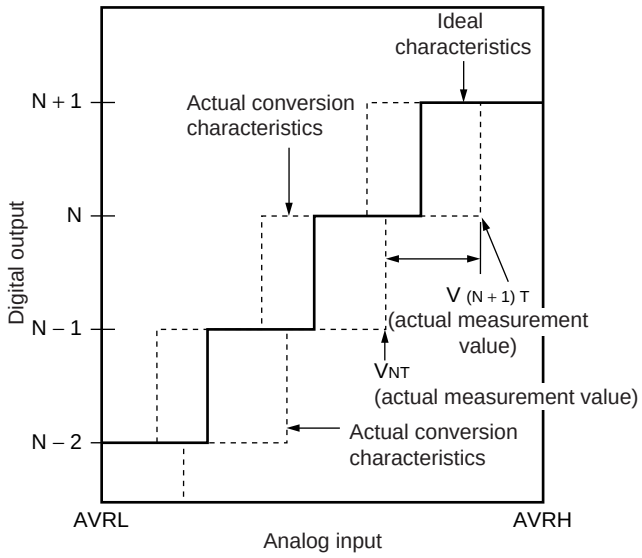
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

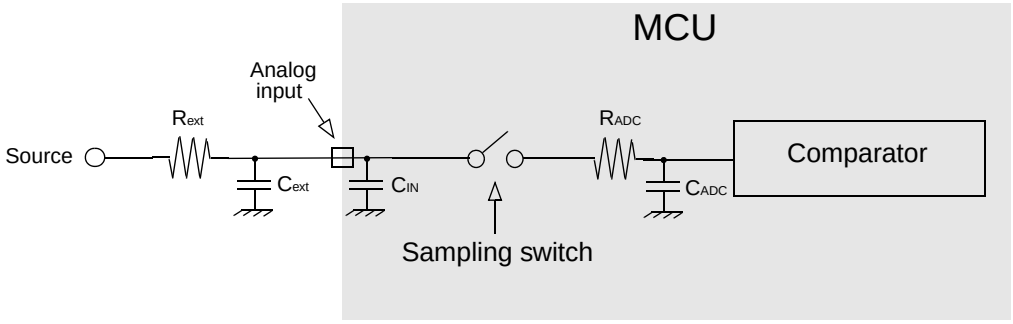
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

Accuracy and setting of the A/D Converter sampling time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{cc} voltage level. The following replacement model can be used for the calculation:



R_{ext}: external driving impedance
C_{ext}: capacitance of PCB at A/D converter input
C_{IN}: capacitance of MCU input pin: 15pF (max)
R_{ADC}: resistance within MCU: 2.6kΩ (max) for $4.5V \le AV_{cc} \le 5.5V$
12kΩ (max) for $3.0V \le AV_{cc} < 4.5V$
C_{ADC}: sampling capacitance within MCU: 10pF (max)

The sampling time should be set to minimum “7τ“. The following approximation formula for the replacement model above can be used:

$$T_{samp}\ [min] = 7 \times (R_{ext} \times (C_{ext} + C_{IN}) + (R_{ext} + R_{ADC}) \times C_{ADC})$$

- Do not select a sampling time below the absolute minimum permitted value (0.5µs for $4.5V \le AV_{cc} \le 5.5V$; 1.2 µs for $3.0V \le AV_{cc} < 4.5V$).
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin. In this case the internal sampling capacitance C_{ADC} will be charged out of this external capacitance.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current I_{IL} (static current before the sampling switch) or the analog input leakage current I_{AIN} (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current I_{IL} cannot be compensated by an external capacitor.
- The accuracy gets worse as |AVRH - AVRL| becomes smaller.

6. Low Voltage Detector characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.5	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.8	3.2	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3	3.4	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.35	3.8	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.5	3.95	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.6	4.1	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.7	4.2	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.8	4.3	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	3.9	4.4	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	3.95	4.5	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	2.6	3	V	CILCR:LVL[3:0]=”1100”
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

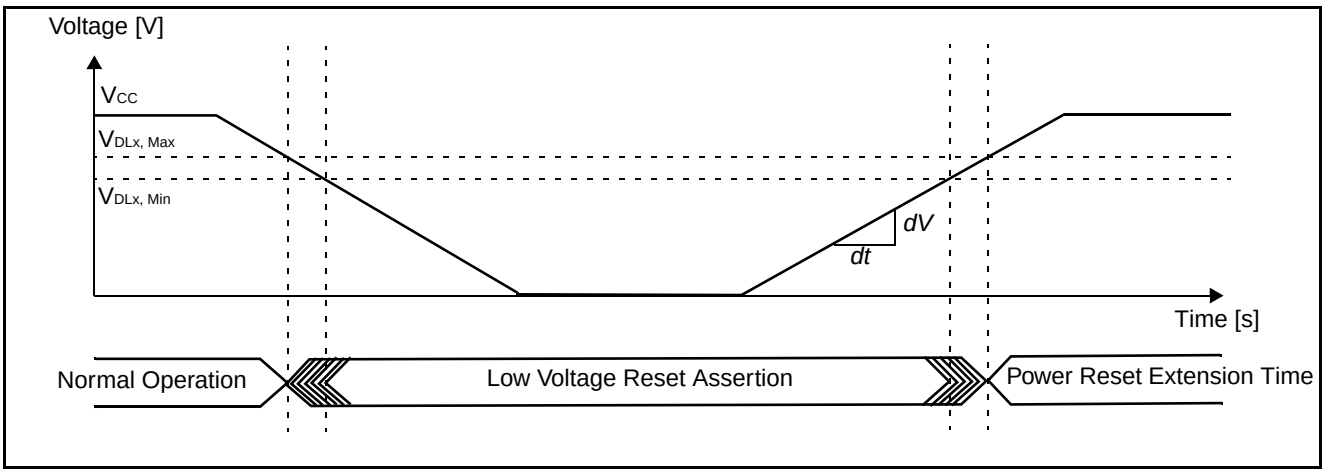
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004 \ \frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of “Level 0” (V_{DL0_MIN}). The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



7. FLASH memory program/erase characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

■ EXAMPLE CHARACTERISTICS

1. Temperature dependency of power supply currents

The following diagrams show the current consumption of samples with typical wafer process parameters in different operation modes.

Common condition for all operation modes:

- V_{CC} = AV_{CC} = 5.0V
- Main clock = 4MHz external clock
- Sub clock = 32kHz external clock

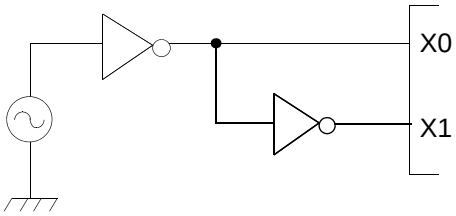
Operation mode details:

Mode name	Details
PLL Run 56	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 2 Flash/ROM wait states (MTCRA=$233A_H$) • RC oscillator and Sub oscillator stopped
PLL Run 48	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 96MHz • f_{CLKB} = f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • 1 Flash/ROM wait states (MTCRA=$6B09_H$) • RC oscillator and Sub oscillator stopped
PLL Run 24	PLL Run mode current I_{CCPLL} with the following settings: • f_{CLKS1} = f_{CLKS2} = 48MHz • f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 0 Flash/ROM wait states (MTCRA=2208_H) • RC oscillator and Sub oscillator stopped
Main Run	Main Run mode current I_{CCMAIN} with the following settings: • f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2} = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Sub oscillator stopped

Mode name	Details
RC Run 2M	RC Run mode current I_{CCRCH} with the following settings: • RC oscillator set to 2MHz (CKFCR:RCFS = 1) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 2MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
RC Run 100k	RC Run mode current I_{CCRCL} with the following settings: • RC oscillator set to 100kHz (CKFCR:RCFS = 0) • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 100kHz • Regulator in Low Power Mode A (SMCR:LPMS = 1) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, Main oscillator and Sub oscillator stopped
Sub Run	Sub Run mode current I_{CCSUB} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKB} = f_{CLKP1} = f_{CLKP2}$ = 32kHz • Regulator in Low Power Mode A (by hardware) • Core voltage at 1.8V (VRCR:LPMA[2:0] = 110_B) • 1 Flash/ROM wait states (MTCRA=0239_H) • PLL, RC oscillator and Main oscillator stopped
PLL Sleep 56	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1}$ = 56MHz • f_{CLKP2} = 28MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 48	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 96MHz • f_{CLKP1} = 48MHz • f_{CLKP2} = 24MHz • Regulator in High Power Mode • Core voltage at 1.9V (VRCR:HPM[1:0] = 11_B) • RC oscillator and Sub oscillator stopped
PLL Sleep 24	PLL Sleep mode current I_{CCSPLL} with the following settings: • $f_{CLKS1} = f_{CLKS2}$ = 48MHz • $f_{CLKP1} = f_{CLKP2}$ = 24MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • RC oscillator and Sub oscillator stopped
Main Sleep	Main Sleep mode current $I_{CCSMAIN}$ with the following settings: • $f_{CLKS1} = f_{CLKS2} = f_{CLKP1} = f_{CLKP2}$ = 4MHz • Regulator in High Power Mode • Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) • PLL, RC oscillator and Sub oscillator stopped

2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

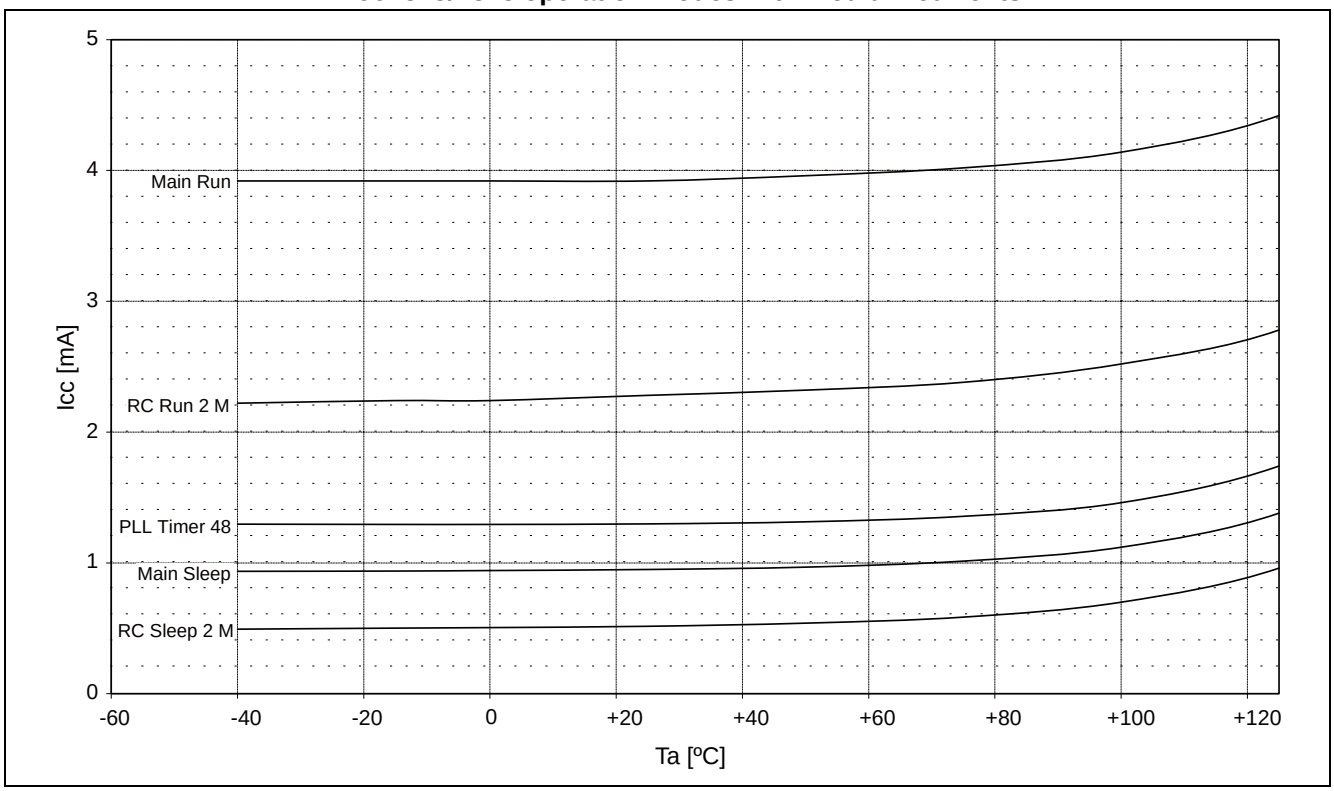
10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

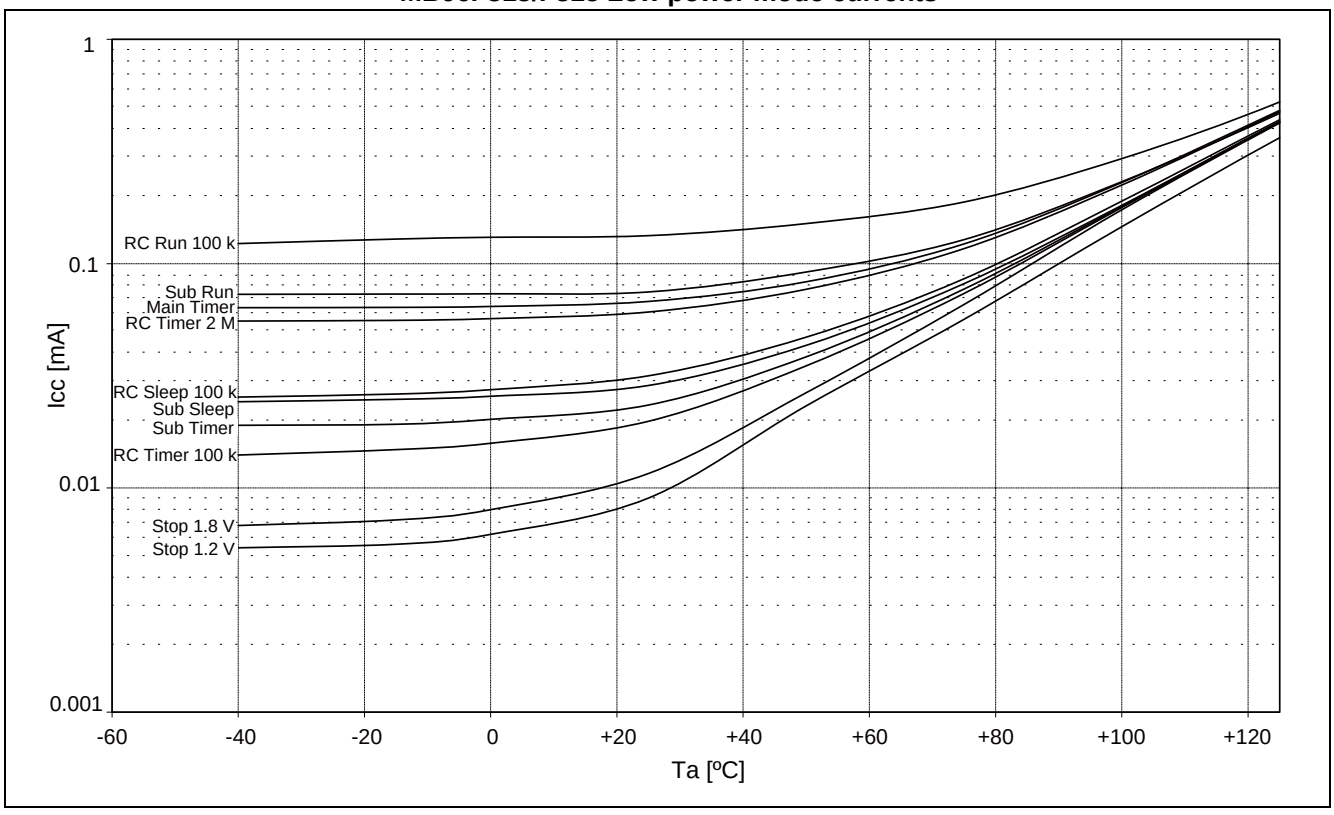
I/O map MB96(F)315x (19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005CA$_H$	PPG17 - Period setting register		PCSR17	W
0005CB$_H$	PPG17 - Period setting register			W
0005CC$_H$	PPG17 - Duty cycle register		PDUT17	W
0005CD$_H$	PPG17 - Duty cycle register			W
0005CE$_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF$_H$	PPG17 - Control status register High	PCNH17		R/W
0005D0$_H$	PPG18 - Timer register		PTMR18	R
0005D1$_H$	PPG18 - Timer register			R
0005D2$_H$	PPG18 - Period setting register		PCSR18	W
0005D3$_H$	PPG18 - Period setting register			W
0005D4$_H$	PPG18 - Duty cycle register		PDUT18	W
0005D5$_H$	PPG18 - Duty cycle register			W
0005D6$_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7$_H$	PPG18 - Control status register High	PCNH18		R/W
0005D8$_H$	PPG19 - Timer register		PTMR19	R
0005D9$_H$	PPG19 - Timer register			R
0005DA$_H$	PPG19 - Period setting register		PCSR19	W
0005DB$_H$	PPG19 - Period setting register			W
0005DC$_H$	PPG19 - Duty cycle register		PDUT19	W
0005DD$_H$	PPG19 - Duty cycle register			W
0005DE$_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF$_H$	PPG19 - Control status register High	PCNH19		R/W
0005E0$_H$-00065F$_H$	Reserved			-
000660$_H$	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661$_H$	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662$_H$	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663$_H$	Peripheral Resource Relocation Register 13	PRRR13		W
000664$_H$-0008FF$_H$	Reserved			-
000900$_H$	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W

MB96F313/F315 operation modes with medium currents



MB96F313/F315 Low power mode currents



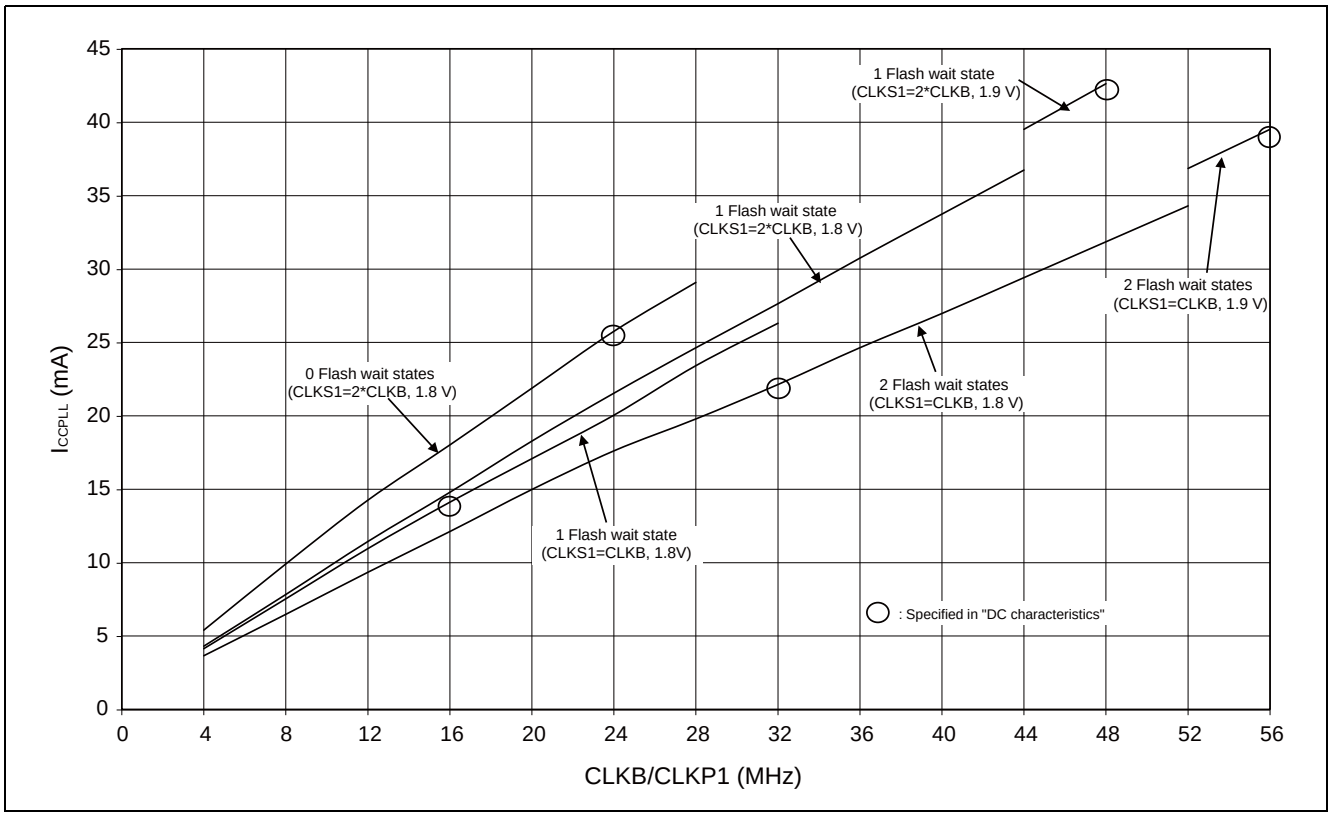
2. Frequency dependency of power supply currents in PLL Run mode

The following diagrams show the current consumption of samples with typical wafer process parameters in PLL Run mode at different frequencies and Flash timing settings.

Measurement conditions:

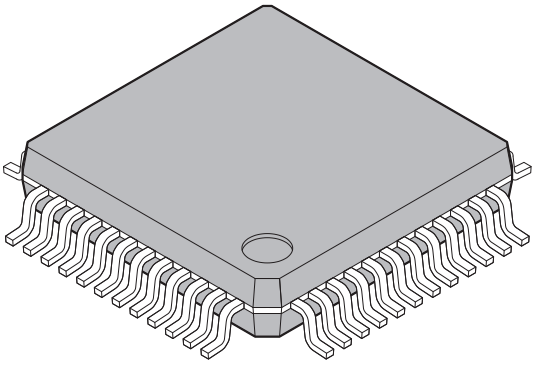
- V_{CC} = AV_{CC} = 5.0V
- Ta = 25°C
- f_{CLKS1} = f_{CLKB} or f_{CLKS1} = 2*f_{CLKB} as described in diagram
- f_{CLKS2} = f_{CLKS1}
- f_{CLKP1} = f_{CLKB}
- f_{CLKP2} = f_{CLKB}/2
- Core voltage at 1.8V (VRCR:HPM[1:0] = 10_B) or 1.9V (VRCR:HPM[1:0] = 11_B) as described in diagram
- Main clock = 4MHz external clock
- Flash memory timing settings:
  - MTCRA=2128_H/2208_H (0 Flash wait states, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=0239_H/2129_H (1 Flash wait state, f_{CLKS1} = f_{CLKB})
  - MTCRA=$4C09_H$/$6B09_H$ (1 Flash wait state, f_{CLKS1} = 2*f_{CLKB})
  - MTCRA=$233A_H$ (2 Flash wait states, f_{CLKS1} = f_{CLKB})
- Average Flash access rate (number of read accesses to the Flash per CLKB clock cycle, no buffer hit):
  - 0 Flash wait states: 0.5
  - 1 Flash wait states: 0.33
  - 2 Flash wait states: 0.25

MB96F313/F315 PLL Run mode currents



■ PACKAGE DIMENSION MB96(F)31x LQFP48

48-pin plastic LQFP

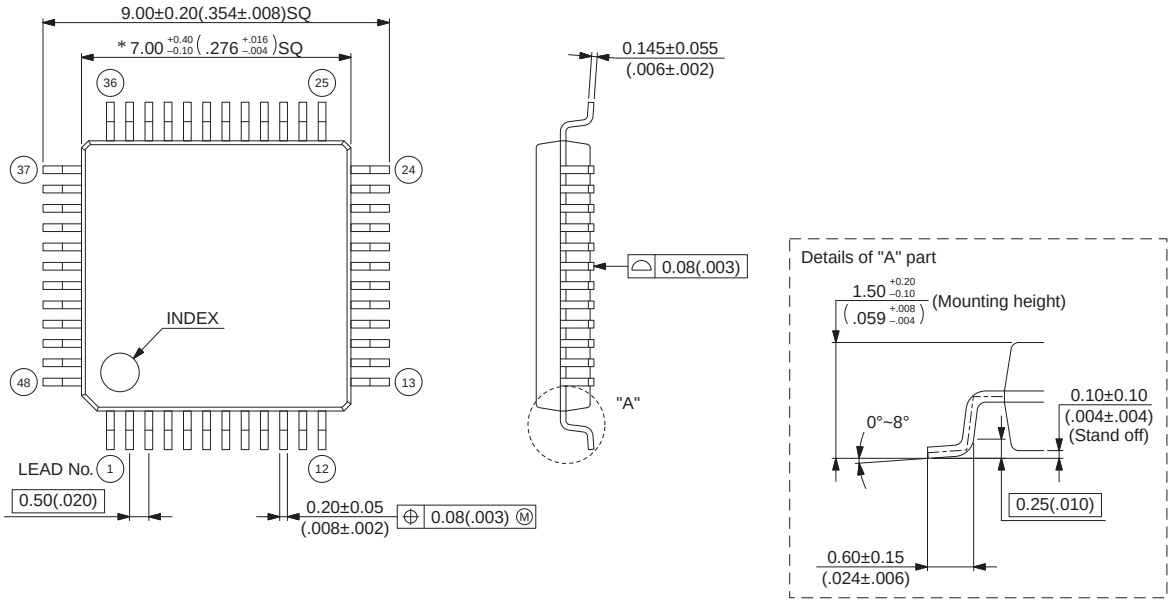


(FPT-48P-M26)

Lead pitch	0.50 mm
Package width × package length	7 mm × 7 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.17 g
Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

I/O map MB96(F)315x (19 of 22)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005CA$_H$	PPG17 - Period setting register		PCSR17	W
0005CB$_H$	PPG17 - Period setting register			W
0005CC$_H$	PPG17 - Duty cycle register		PDUT17	W
0005CD$_H$	PPG17 - Duty cycle register			W
0005CE$_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF$_H$	PPG17 - Control status register High	PCNH17		R/W
0005D0$_H$	PPG18 - Timer register		PTMR18	R
0005D1$_H$	PPG18 - Timer register			R
0005D2$_H$	PPG18 - Period setting register		PCSR18	W
0005D3$_H$	PPG18 - Period setting register			W
0005D4$_H$	PPG18 - Duty cycle register		PDUT18	W
0005D5$_H$	PPG18 - Duty cycle register			W
0005D6$_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7$_H$	PPG18 - Control status register High	PCNH18		R/W
0005D8$_H$	PPG19 - Timer register		PTMR19	R
0005D9$_H$	PPG19 - Timer register			R
0005DA$_H$	PPG19 - Period setting register		PCSR19	W
0005DB$_H$	PPG19 - Period setting register			W
0005DC$_H$	PPG19 - Duty cycle register		PDUT19	W
0005DD$_H$	PPG19 - Duty cycle register			W
0005DE$_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF$_H$	PPG19 - Control status register High	PCNH19		R/W
0005E0$_H$-00065F$_H$	Reserved			-
000660$_H$	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661$_H$	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662$_H$	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663$_H$	Peripheral Resource Relocation Register 13	PRRR13		W
000664$_H$-0008FF$_H$	Reserved			-
000900$_H$	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
3	■ FEATURES	Corrected the sentence “Reload timer overflow” to “Reload timer underflow” for Programmable Pulse Generator.
5, 6	■ PRODUCT LINEUP	Removed footnote. Changed name of evaluation sample.
8	■ PIN ASSIGNMENTS	Corrected pin number of X0. 34 → 35
14	■ MEMORY MAP	Changed name of evaluation sample.
17	■ SERIAL PROGRAMMING COMMUNICATION INTERFACE	Corrected device name, package name and pin numbers.
49-50	■ ELECTRICAL CHARACTERISTICS 3.DC characteristics	Note added in DC characteristics how to select driving strength of ports.
51-56	■ ELECTRICAL CHARACTERISTICS 3.DC characteristics	Updated Icc specs. Updated Power Supply current spec in Run/Sleep/Timer/ Stop modes (new spec items in PLL Run/Sleep mode, small adjustment of most other values).
57	■ ELECTRICAL CHARACTERISTICS 4.AC Characteristics	Note added that PLL phase jitter spec does not include jitter coming from Main clock. Added specification of RC clock stabilization time.
65	■ ELECTRICAL CHARACTERISTICS 5. Analog Digital Converter	Changed the item for “Zero reading voltage” and “Full scale reading voltage”. AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg.
68	■ ELECTRICAL CHARACTERISTICS 5. Analog Digital Converter	“Notes on A/D Converter Section” was rewrite and renamed to “Accuracy and setting of the A/D Converter sampling time”. Impact of input pin capacitance and external capacitance added to formula for calculation of the sampling time.
69	■ ELECTRICAL CHARACTERISTICS 6. Low Voltage Detector characteristics	Detection levels updated.
72-77	■ EXAMPLE CHARACTERISTICS	Added.
78	■ PACKAGE DIMENSION MB96(F)31x LQFP48	Updated package figure. Added the following sentence under the figure: “Please check the latest package dimension at the following URL. http://edevice.fujitsu.com/package/en-search/”.
79	■ ORDERING INFORMATION	Updated part number: MB96F313/F315**A → MB96F313/F315**B Removed footnote. Added Part Numbers “MB96F313RSB PMC-GSE1”, “MB96F315RSB PMC-GSE1”.

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FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan
Tel: +81-45-415-5858
http://jp.fujitsu.com/fsl/en/

For further information please contact:

North and South America
FUJITSU SEMICONDUCTOR AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://us.fujitsu.com/micro/

Europe
FUJITSU SEMICONDUCTOR EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/semiconductor/

Korea
FUJITSU SEMICONDUCTOR KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU SEMICONDUCTOR ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fujitsu.com/sg/services/micro/semiconductor/

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

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