4-Channel, Software Selectable True bipolar Input, 12-Bit Plus Sign ADC

Preliminary Technical Data

AD7324*

FEATURES

- **12-Bit plus Sign SAR ADC**
- **True Bipolar Input Ranges**
- **Software Selectable Input Ranges**
  ± 10V, ± 5V, ± 2.5V, 0 to 10V
- **1 MSPS Throughput Rate**
- **Four Analog Input Channels with Channel Sequencer**
- **Single Ended, True Differential and Pseudo Differential Analog Input Capability**
- **High Analog Input Impedance**
- **Low Power:- 26 mW max**
- **Full Power Signal Bandwidth: 7 MHz**
- **Internal 2.5 V Reference**
- **High Speed Serial Interface**
- **Power Down Modes**
- **16-Lead TSSOP package**
- ***i*CMOS™ Process Technology**
- **For eight and two channel equivalent devices see AD7328 and AD7322 respectively.**

GENERAL DESCRIPTION

The AD7324 is a 4-Channel, 12-Bit plus Sign Successive Approximation ADC. The ADC has a high speed serial interface that can operate at throughput rates up to 1 Msps.

The AD7324 can accept true bipolar Analog Input signals. The AD7324 has four software selectable inputs Ranges, ±10V, ±5V, ±2.5V and 0 to 10V. Each analog input channel can be independently programmed to one of the four input ranges.

The Analog input channels on the AD7324 can be programmed to be Single-Ended, true Differential or Pseudo Differential.

The AD7324 contains a 2.5V Internal reference. The AD7324 also allows for external Reference operation. If a 3V reference is applied the $REF_{IN/OUT}$ pin the AD7324 can accept a true Bipolar ±12V Analog Input. Minimum V_{DD} and V_{SS} supplies of ±12V are required for the ±12V Input Range.

* Protected by U.S. Patent No. 6,731,232

FUNCTIONAL BLOCK DIAGRAM

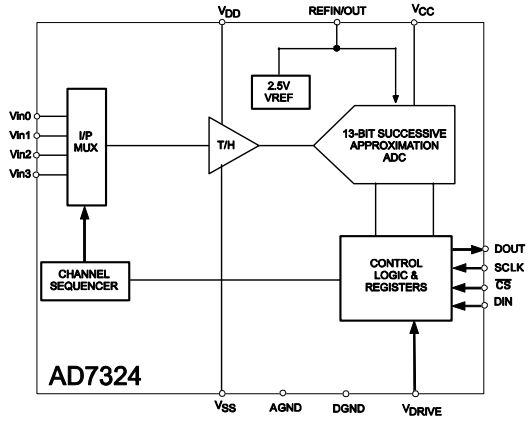

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD7324 can accept True Bipolar Analog Input signals, ±10V, ±5V, ±2.5V and 0 to 10V unipolar signals.

2. The Four Analog Inputs can be configured as 4 Single-Ended inputs, 2 True Differential, 2 Pseudo Differential or 3 Pseudo Differential Inputs. The AD7324 has high Impedance Analog Inputs.

3. The AD7324 features a High Speed Serial Interface. Throughput Rates up to 1 MSPS can be achieved on the AD7324.

4. Low Power, 26 mW at maximum throughput rate of 1 MSPS.

Device Number	Number of Bits	Number of Channels
AD7328	12-Bits Plus Sign	8
AD7322	12-Bits Plus Sign	2

*i*CMOS™ Process Technology
For analog systems designers within industrial/instrumentation equipment OEMs who need high performance ICs at higher-voltage levels, *i*CMOS is a technology platform that enables the development of analog ICs capable of 30V and operating at +/- 15V supplies while allowing dramatic reductions in power consumption and package size, and increased AC and DC performance.

Rev. PrH

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REVISION HISTORY

Revision PrH: Preliminary Version

AD7324—SPECIFICATIONS[1]

Table 1. Unless otherwise noted, V_{DD} = + 12V to +16.5V, V_{SS} = -12V to –16.5V, V_{CC} = 2.7V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, V_{REF} = 2.5V Internal/External, f_{SCLK} = 20 MHz, f_S = 1 MSPS T_A = T_{MAX} to T_{MIN}

Parameter	Specification	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			F_{IN} = 50 kHz Sine Wave
Signal to Noise Ratio (SNR) [2]	76	dB min	Differential Mode
	72	dB min	Single-Ended /Pseudo Differential Mode
Signal to Noise + Distortion (SINAD)[2]	75	dB min	Differential Mode
	71.5	dB min	Single-Ended/Pseudo Differential Mode
Total Harmonic Distortion (THD)[2]	-80	dB max	
Peak Harmonic or Spurious Noise (SFDR) [2]	-80	dB max	
Intermodulation Distortion (IMD) [2]			F_a = 40.1 kHz, F_b = 41.5 kHz
Second Order Terms	-88	dB typ	
Third Order Terms	-88	dB typ	
Aperature Delay[2]	10	ns max	
Aperature Jitter[2]	50	ps typ	
Common Mode Rejection (CMRR)[2]	TBD	dB typ	
Channel-to-Channel Isolation[2]	-80	dB typ	F_{IN} = 400 kHz
Full Power Bandwidth[2]	7	MHz typ	@ 3 dB
	1.5	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	12+Sign	Bits	
Integral Nonlinearity[2]	±1.5	LSB max	
Differential Nonlinearity[2]	± 0.95	LSB max	Guaranteed No Missing Codes to 13-Bits
Offset Error[3]	±8	LSB max	Unipolar Range with Straight Binary output coding
Offset Error Match[2]	±0.5	LSB max	
Gain Error[2]	±6	LSB max	
Gain Error Match[2]	±0.6	LSB max	
Positive Full-Scale Error[2]	±3	LSB max	Bipolar Range with Twos Complement Output Coding
Positive Full Scale Error Match[2]	±0.6	LSB max	
Bipolar Zero Error[2]	±8	LSB max	
Bipolar Zero Error Match[2]	±0.5	LSB max	
Negative Full Scale Error[2]	±4	LSB max	
Negative Full Scale Error Match[2]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Ranges	±10V	Volts	V_{DD} = +10V min , V_{SS} = -10V min, V_{CC} = 2.7V to 5.25V
(Programmed via Range Register)	±5V		V_{DD} = +5V min, V_{SS} = -5V min, V_{CC} = 2.7V to 5.25V
	±2.5V		V_{DD} = +5V min, V_{SS} = - 5V min, V_{CC} = 2.7V to 5.25V
	0 to 10V		V_{DD} = +10V min, V_{SS} = 0 V min, V_{CC} = 2.7V to 5.25V
			See Table 5
DC Leakage Current	±10	nA max	
Input Capacitance	12	pF typ	When in Track, ±10V Range
	15	pF typ	When in Track, ±5V, 0 to 10V Range
	20	pF typ	When in Track, ±2.5V Range
	3	pF typ	When in Hold
REFERENCE INPUT/OUTPUT			
Input Voltage Range	+2.5 to +3V	V min to max	
Input DC Leakage Current	±1	µA max	
Input Capactiance	20	pF typ	
Reference Output Voltage	2.49/2.51	Vmin/max	
Reference Temperature Coefficient	25	ppm/°C max	10 ppm/°C typ
Reference Output Impedance	25	Ω typ	

Parameter	Specification	Units	Test Conditions/Comments
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input High Voltage, V_{INL}	0.8	V max	V_{CC} = 4.75 to 5.25 V
	0.4	V max	V_{CC} = 2.7 to 3.6 V
Input Current, I_{IN}	± 1	µA max	V_{IN} = 0V or V_{CC}
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE}- 0.2V	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating State Leakage Current	±1	µA max	
Floating State Output Capacitance[3]	10	pF max	
Output Coding	Straight Natural Binary		Coding bit set to 1 in Control Register
	Two's Complement		Coding bit set to 0 in Control Register
CONVERSION RATE			
Conversion Time	800	ns max	16 SCLK Cycles with SCLK = 20 MHz
Track-and-Hold Acquisition Time	200	ns max	Sine Wave Input
	200	ns max	Full Scale Step input
Throughput Rate	1	MSPS max	See Serial Interface section
POWER REQUIREMENTS			Digital Inputs = 0V or V_{CC}
V_{DD}[4]	12V/+16.5V	V min/max	See Table 5
V_{SS}[4]	-12V/16.5V	V min/max	See Table 5
V_{CC}	2.7V / 5.25V	V min/max	See Table 5
V_{DRIVE}	2.7V/5.25V	V min/max	
Normal Mode			
I_{DD}	300	µA max	V_{DD} = +16.5V
I_{SS}	370	µA max	V_{SS} = -16.5V
I_{CC}	2	mA max	V_{CC} = 5.25V
Auto-Standby Mode			F_{SAMPLE} = TBD
I_{DD}	TBD	µA max	
I_{SS}	TBD	µA max	
I_{CC}	1.6	mA typ	
Auto-Standby Mode			F_{SAMPLE} = TBD
I_{DD}	TBD	µA max	
I_{SS}	TBD	µA max	
I_{CC}	1	mA typ	
Full Shutdown Mode			
I_{DD}	0.9	µA max	
I_{SS}	0.9	µA max	
I_{CC}	0.9	µA max	SCLK On or Off
POWER DISSIPATION			
Normal Mode	26	mW max	V_{DD} = +16.5V, V_{SS} = -16.5V, V_{CC} = 5.25V,
Full Shutdown Mode	35	µW max	V_{DD} = +16.5V, V_{SS} = -16.5V, V_{CC} = 5.25V,

NOTES
[1] Temperature ranges as follows: -40°C to +85°C
[2] See Terminology
[3] Guaranteed by Characterization
[4] Functional from V_{DD} = +4.75V and V_{SS} = -4.75V
Specifications subject to change without notice.

TIMING SPECIFICATIONS

Table 2. Unless otherwise noted, V_{DD} = +12V to + 16.5V, V_{SS} = -12V to –16.5V, V_{CC} =2.7V to 5.25, V_{DRIVE}=2.7V to 5.25, V_{REF} = 2.5V Internal/External, T_A = T_{MAX} to T_{MIN}

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	16×t_{SCLK}	ns max	T_{SCLK} = 1/f_{SCLK}
t_{QUIET}	50	ns max	Minimum Time between End of Serial Read and Next Falling Edge of $\overline{CS}$
t_1	10	ns min	Minimum $\overline{CS}$ Pulse width
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3	20	ns max	Delay from $\overline{CS}$ until D_{OUT} Three-State Disabled
t_4	TBD	ns max	Data Access Time after SCLK Falling Edge.
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulsewidth
t_6	0.4t_{SCLK}	ns min	SCLK High Pulsewidth
t_7	10	ns min	SCLK to Data Valid Hold Time
t_8	25	ns max	SCLK Falling Edge to D_{OUT} High Impedance
	10	ns min	SCLK Falling Edge to D_{OUT} High Impedance
t_9	TBD	ns min	DIN set-up time prior to SCLK falling edge
t_{10}	5	ns min	DIN hold time after SCLK falling edge
	1	µs max	Power up from Auto Standby
	TBD	µs max	Power up from Full Shutdown/Auto Shutdown Mode

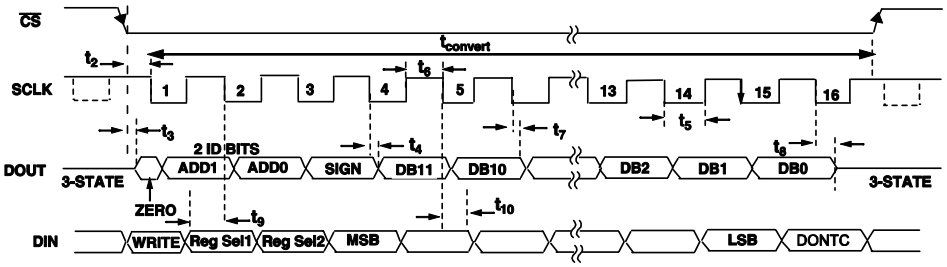


Figure 2. Serial Interface timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. T_A = 25°C, unless otherwise noted

V_{DD} to AGND, DGND	-0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to –16.5 V
V_{CC} to AGND, DGND	-0.3V to +7V
V_{DRIVE} to V_{CC}	-0.3 V to V_{CC} + 0.3V
AGND to DGND	-0.3 V to +0.3 V
Analog Input Voltage to AGND	V_{SS} -0.5V to V_{DD} + 0.5V
Digital Input Voltage to DGND	-0.3 V to +7 V
Digital Output Voltage to GND	-0.3 V to V_{DRIVE} +0.3V
REF_{IN} to AGND	-0.3 V to V_{CC} +0.3V
Input Current to Any Pin Except Supplies[2]	±10mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143 °C/W
θ_{JC} Thermal Impedance	45 °C/W
Pb-free Temperature, Soldering	
Reflow	260(+0)°C
ESD	TBD

Pin Functional Descriptions

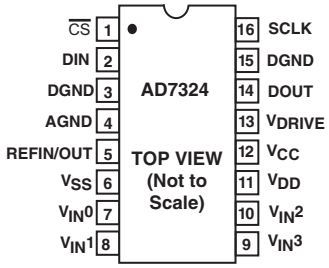


Figure 3. AD7324 Pin Configuration TSSOP

Table 4. AD7324 Pin Function Descriptions

Pin Mnemonic	Pin Number	Description
SCLK	16	Serial Clock. Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7324. This clock is also used as the clock source for the conversion process.
D_{OUT}	14	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input and 16 SCLKs are required to access the data. The data stream consists of one leading zero followed by two channel identification bits, followed by the sign bit followed by the 12 bits of conversion data. The data is provided MSB first. See the Serial Interface section.
$\overline{CS}$	1	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7324 and frames the serial data transfer.
DIN	2	Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the register on the falling edge of SCLK. See Register section.
AGND	4	Analog Ground. Ground reference point for all analog circuitry on the AD7324. All analog input signals and any external reference signal should be referred to this AGND voltage.
REF_{IN}/REF_{OUT}	5	Reference Input/ Reference Output pin. The on-chip reference is available on this pin for use external to the AD7324. Alternativley, the internal reference can be disabled and an external reference applied to this input. When using the AD7324 with an external reference, the internal reference must be disabled via the control register. The nominal reference voltage is 2.5 V, which appears at the pin. A 470 nF decoupling capacitor sgould be placed on the Reference pin.
V_{CC}	12	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7324. This supply should be decoupled to AGND.
V_{DD}	11	Positive power supply voltage. This is the positive supply voltage for the Analog Input section.
V_{SS}	6	Negative power supply voltage. This is the negavtive supply voltage for the Analog Input section.
V_{DRIVE}	13	The voltage applied to this pin determines the voltage at which the serial interface operates.
DGND	3,15	This is the Digital Ground Connection.
Vin0-Vin3	7,8,9,10	Analog input 0 through Analog Input 3. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address bits, ADD1 through ADD0, in the control register. The inputs can be configured as 4 Single-Ended Inputs, 2 True Differential Input pairs, 2 Pseudo Differential inputs or 3 Pseudo Differential Inputs. The configuration of the Analog inputs is selected by programming the Mode bits, Mode1 and Mode0, in the Control Register. The input range on each input channel is controlled by programming the range register. Input ranges of ±10V, ±5V, ±2.5V and 0 to 10V can be selected on each analog input channel. See Register section.

TERMINOLOGY

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Offset Code Error
This applies to Straight Binary output coding. It is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match
This is the difference in Offset Error between any two input channels.

Gain Error
This applies to Straight Binary output coding. It is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., 4 x VRef – 1 LSB, 2 x V_{REF} –1 LSB, V_{REF} –1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain Error between any two input channels channels.

Bipolar Zero Code Error
This applies when using twos complement output coding and a bipolar Analog Input. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, i.e., AGND - 1 LSB.

Bipolar Zero Code Error Match
This refers to the difference in Bipolar Zero Code Error between any two input channels.

Positive Full Scale Error
This applies when using twos complement output coding and any of the bipolar Analog Input ranges. It is the deviation of the last code transition (011…110) to (011…111) from the ideal (+4 x V_{REF} - 1 LSB, + 2 x V_{REF} – 1 LSB, + V_{REF} – 1 LSB) after the bipolar Zero Code Error has been adjusted out.

Positive Full Scale Error Match

This is the difference in Positive Full Scale error between any two input channels.

Negative Full Scale Error
This applies when using twos complement output coding and any of the bipolar Analog Input ranges. This is the deviation of the first code transition (10…000) to (10…001) from the ideal (i.e., - 4 x V_{REF} + 1 LSB, - 2 x V_{REF} + 1 LSB, - V_{REF} + 1 LSB) after the Bipolar Zero Code Error has been adjusted out.

Negative Full Scale Error Match

This is the difference in Negative Full Scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode after the fifteenth SCLK falling edge. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (Noise + Distortion) = (6.02N + 1.76) dB

Thus for a 13-bit converter, this is 80.02 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7324 it is defined as:

$$THD(dB) = 20\log\frac{\sqrt{V_2^{\,2}+V_3^{\,2}+V_4^{\,2}+V_5^{\,2}+V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 400 kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in

the selected channel with a 50 kHz signal. The figure given is the worst-case across all eight channels for the AD7324.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with non-linearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7324 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSR (Power Supply Rejection)
Variations in power supply will affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. See Typical Performance Curves.

Theory of Operation

CIRCUIT INFORMATION

The AD7324 is a fast, 4-Channel, 12-Bit Plus Sign, Bipolar Input, Serial A/D converter. The AD7324 can accept bipolar input ranges that include ±10V, ±5V, ±2.5V, it can also accept 0 to 10V unipolar input range. A different Analog input range can be programmed on each analog input Channel via the on-chip range register. The AD7324 has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

The AD7324 requires V_{DD} and V_{SS} dual supplies for the high voltage Analog input structure. These supplies must be equal to or greater than the Analog input range. See Table 5 for the minimum requirements on these supplies for each Analog Input Range. The AD7324 requires a low voltage 2.7V to 5.25 V V_{CC} supply to power the ADC core.

Table 5. Reference and Supply Requirements for each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full Scale Input Range(V)	AV_{CC} (V)	Minimum V_{DD}/V_{SS} (V)
±10	2.5	±10	3/5	±10
	3.0	±12	3/5	±12
± 5	2.5	±5	3/5	±5
	3.0	±6	3/5	±6
±2.5	2.5	±2.5	3/5	±5
	3.0	±3	3/5	±5
0 to 10	2.5	0 to 10	3/5	+10/AGND
	3.0	0 to 12	3/5	+12/AGND

In order to meet the specified performance specifications when the AD7324 is configured with the minimum V_{DD} and V_{SS} supplies for a chosen Analog input range the throughput rate should be decreased from the maximum throughput range. See typical performance curves.

The Analog Inputs Can be configured as either 4 Single-Ended inputs, 2 True Differential Inputs, 2 Pseudo Differential Inputs or 3 Pseudo Differential Inputs. Selection can be made by programming the Mode bits, Mode0 and Mode1, in the Control Register.

The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The AD7324 has an on-chip 2.5 V reference. However the AD7324 can also work with an external Reference. On power up the external reference operation is the default option. If the internal Reference is the preferred option the user must write to the reference bit in the control register to select the internal Reference operation.

The AD7324 also features power-down options to allow power saving between conversions. The power-down modes are selected by programming the on-chip Control Register, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7324 is a successive approximation analog-to-digital converter, based around two capacitive DACs. Figure 4 and Figure 5 show simplified schematics of the ADCs in Single Ended Mode during the acquisition and conversion phase, respectively. Figure 6 and Figure 7 show simplified schematics of the ADCs in Differential Mode during acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and a capacitive DAC. In Figure 4 (the acquisition phase), SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor array acquires the signal on the input.

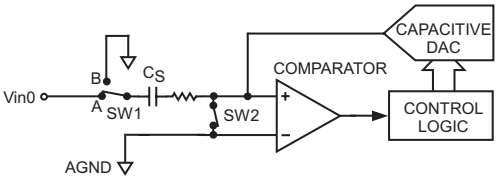


Figure 4. ADC Acquisition Phase(Single Ended)

When the ADC starts a conversion (Figure 5), SW2 will open and SW1 will move to position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC is used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC output code

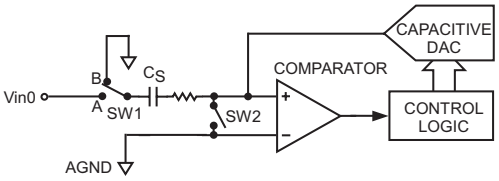


Figure 5. ADC Conversion Phase(Single Ended)

Figure 6 shows the differential configuration during the Acquisition phase. For the Conversion Phase, SW3 will open, SW1 and SW2 will move to position B, see Figure 7. The output impedances of the source driving the Vin+ and Vin- pins must be matched; otherwise the two inputs will have different settling times, resulting in errors.

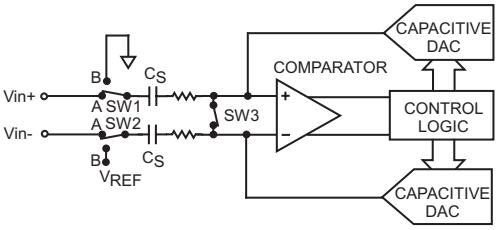


Figure 6. ADC Differential Configuration during Acquisition Phase

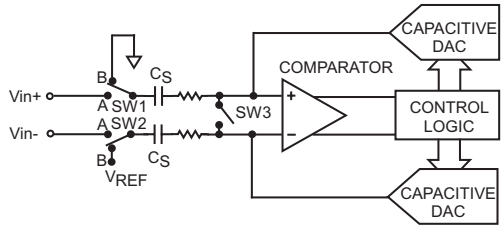


Figure 7. ADC Differential Configuration during Conversion Phase

Output Coding

The AD7324 default output coding is set to two's complement. The output coding is controlled by the Coding bit in the Control Register. To change the output coding to Straight Binary Coding the Coding bit in the Control Register must be set. When operating in Sequence mode the output coding for each channel in the sequence will be the value written to the coding bit during the last write to the Control Register.

Transfer Functions

The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size is dependant on the Analog input Range selected.

Table 6. LSB sizes for each Analog Input Range

Input Range	Full Scale Range/8192	LSB Size
±10V	20V/8192	2.441 mV
±5V	10V/8192	1.22 mV
±2.5V	5V/8192	0.61 mV
0 to 10V	10V/8192	1.22 mV

The ideal transfer characteristic for the AD7324 when Twos Complement coding is selected is shown in Figure 8, and the ideal transfer characteristic for the AD7324 when Straight Binary coding is selected is shown in Figure 9.

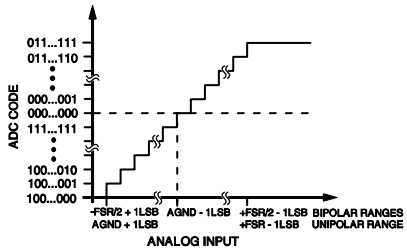


Figure 8 Twos Complement Transfer Characteristic (Bipolar Ranges)

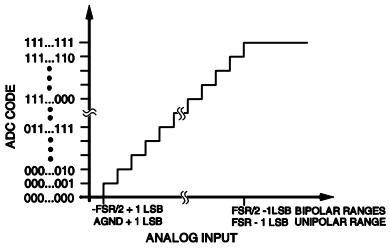


Figure 9. Straight Binary Transfer Characteristic (Bipolar Ranges)

ANALOG INPUT

The analog inputs of the AD7324 may be configured as Single-Ended, True differential or Pseudo Differential via the Control Register Mode Bits as shown Table 9 of the Register Section. The AD7324 can accept True bipolar input signals. On power up the Analog inputs will operate as 4 Single-Ended Analog Input Channels. If True Differential or Pseudo Differential is required, a write to the Control register is necessary to change this configuration after power up.

Figure 10 shows the equivalent Analog input circuit of the AD7324 in Single-Ended Mode. Figure 11 shows the equivalent Analog input structure in Differential mode. The Two Diodes provide ESD protection for the Analog Inputs.

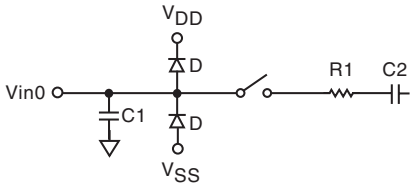


Figure 10. Equivalent Analog Input Circuit-(Single Ended)

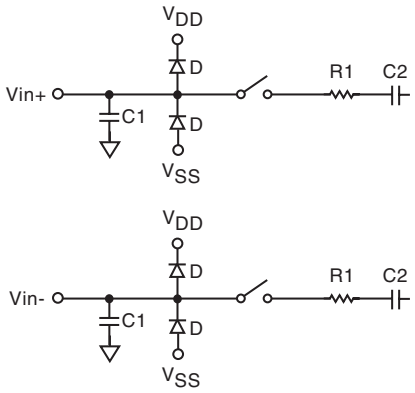


Figure 11. Equivalent Analog Input Circuit-(Differential)

Care should be taken to ensure the Analog Input never exceeds the V_{DD} and V_{SS} supply rails by more than 300 mV. This will cause the diodes to become forward biased and start conducting into either the V_{DD} or V_{SS} rails. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The Capacitor C1, in Figure 10 and Figure 11 is typically 4 pF and can primarily be attributed to pin capacitance. The resistor R1, is a lumped component made up of the on-resistance of the input multiplexer and the track-and-hold switch. The Capacitor C2, is the sampling capacitor, its capacitance will vary depending on the Analog input range selected.

Track-and-Hold Section

The Track-and-Hold on the Analog Input of the AD7324 allows the ADC to accurately convert an input sine wave of full scale amplitude to 12-Bit Plus Sign accuracy. The input bandwidth of the Track-and-Hold is greater than the Nyquist rate of the ADC, the AD7324 can handle frequencies up to 7 MHz.

The Track-and-Hold enters its tracking mode on the 15th SCLK falling edge after the $\overline{CS}$ falling edge. The time required to acquire an input signal will depend on how quickly the sampling capacitor is charged. With zero source impedance 200 ns will be sufficient to acquire the signal to the 13-Bit level.

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R)\ C)$$

where C is the Sampling Capacitance and R is the resistance seen by the track-and-hold amplifier looking back on the input. For the AD7324, the value of R will include the on-resistance of the input multiplexer. The value of R is typically 300 Ω. R_{SOURCE} should include any extra source impedance on the Analog input.

The AD7324 enters track on the fifteenth SCLK falling edge. When running the AD7324 at a throughput rate of 1 MSPS with a 20 MHz SCLK signal the ADC will have approx. 1 SCLK period plus t_8 plus the quiet time, T_{QUIET}, in order to acquire the analog input signal. The ADC goes back into hold on the $\overline{CS}$ falling edge.

TYPICAL CONNECTION DIAGRAM

Figure 12 shows a typical connection diagram for the AD7324. In this configuration the AGND pin is connected to the Analog ground plane of the system. The DGND pin is connected to the Digital ground plane of the system. The Analog Inputs on the AD7324 can be configured to operate in Single Ended, True Differential or Pseudo Differential Mode. The AD7324 can operate with either the internal or an external reference. In Figure 12, the AD7324 is configured to operate with the internal 2.5V reference. A 470 nF decoupling capacitor is required when operating with the internal reference.

The V_{CC} pin can be connected to either a 3V or a 5V supply voltage. The V_{DD} and V_{SS} are the dual supplies for the high voltage analog input structures. The voltage on these pins must be equal to or greater than the highest analog input range selected on the analog input channels, see Table 5 for more information. The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface.

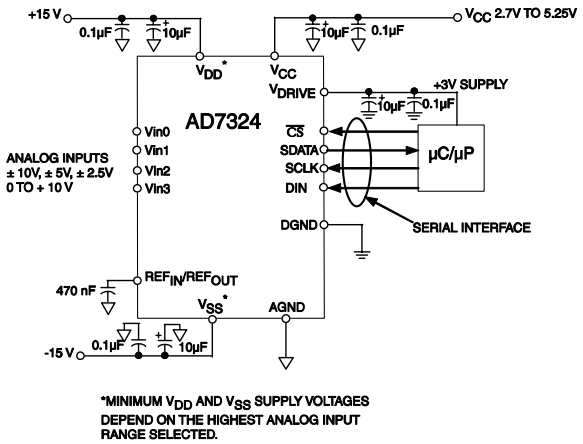


Figure 12. Typical Connection Diagram

AD7324 REGISTERS

The AD7324 has three-programmable registers, the **Control Register**, **Sequence Register**, and the **Range Register**. These registers are write only registers.

Addressing these Registers

A serial transfer on the AD7324 consists of 16 SCLK cycles. The three MSBs on the DIN line during this 16 SCLK transfer are decoded to determine which register is addressed during the serial transfer. The three MSBs consists of the Write bit, Register Select 1 bit and Register Select 2 bit. The Register Select bits are used to determine which of the four on-board registers is selected. The Write bit will determine if the Data on the DIN line following the Register select bits will be loaded into the addressed register or not. If the Write bit is 1 the bits will be loaded into the register addressed by the Register Select bits. If the Write Bit is a 0 the data on the DIN will not be loaded into any register.

Table 7. Decoding Register Select bits and Write bit.

Write	Register Select1	Register Select2	Comment
0	0	0	Data on the DIN line during this serial transfer will be ignored
1	0	0	This combination selects the Control Register. The subsequent 12 bits will be loaded into the Control Register.
1	0	1	This combination selects the Range Register. The subsequent 8 bits will be loaded into the Range Register.
1	1	1	This combination selects the Sequence Register. The subsequent 8 bits will be loaded into the Sequence Register.

CONTROL REGISTER

The Control Register is used to select the Analog Input configuration, Reference, Coding, Power mode etc. The Control Register is a write only 12-bit register. Data loaded on the DIN line corresponds to the AD7324 configuration for the next conversion. Data should be loaded into the Control Register after the Range Register and the Sequence Register has been initialized, that is if the Sequence register is being used. The bit functions of the Control Register are outlined in Table 8.

Control Register (The Power-up status of all bits is 0)

Table 8. Control Register

MSB LSB

Write	Register Select 1	Register Select 2	DONTC	ADD1	ADD0	Mode1	Mode0	PM1	PM0	Coding	Ref	Seq1	Seq2	ZERO	0

Bit	Mnemonic	Comment
12	DONTC	Don't Care. The value written to this bit of the Control Register is a don't care, i.e., it doesn't matter if the bit is 0 or 1.
11,10	ADD1, ADD0	These two Channel Address bits are used to select the analog input channel for the next conversion if the Sequencer is not being used. If the Sequencer is being used, these two Channel Address bits are used to select the final channel in a consecutive sequence.
9, 8	Mode1, Mode0	These two mode bits are used to select the configuation on the four Analog Input Pins. They are used in conjunction with the channel Address bits. On the AD7324 the analog inputs can be configured as either 4 Single Ended Inputs, 2 Fully Differential Inputs, 2 Pseudo Differential inputs or 3 Pseudo Differential Inputs. See Table 9
7,6	PM1, PM0	Power Management Bits. These two bits are used to select different power mode options. Table 10.
5	Coding	This bit is used to select the type of output coding the AD7324 will use for the next conversion result. If the

		Coding = 0 then the output coding will be 2s Complement. If Coding = 1, then the output coding will be Straight Binary. When operating in Sequence mode the output coding for each channel will be the value written to the coding bit during the last write to the Control Register.
4	Ref	Reference bit. This bit is used to enable or disable the internal reference. If this Ref = 0 then the External Reference will be enabled and used for the next conversion and the internal reference will be disabled. If ref = 1 then the Internal Reference will be used for the next conversion. When operating in Sequence mode the Reference used for each channel will be the value written to the Ref bit during the last write to the Control Register.
3,2	Seq1/Seq2	The Sequence 1 and Sequence 2 bits are used to control the operation of the Sequencer. See Table 11.
1	ZERO	A zero must be written to this bit to ensure correct operation of the AD7324.

Table 9. Analog Input Configuration Selection

Channel Address Bits		**Mode1 =1, Mode0 = 1**		**Mode1 = 1, Mode0 =0**		**Mode1 = 0, Mode0 =1**		**Mode1 =0, Mode0 =0**	
		3 Pseudo Differential I/ps		4 Fully Differential i/ps		2 Pseudo Differential i/ps		Four-Single Ended i/ps	
ADD1	**ADD0**	**Vin+**	**Vin-**	**Vin+**	**Vin-**	**Vin+**	**Vin-**	**Vin+**	**Vin-**
0	0	Vin0	Vin3	Vin0	Vin1	Vin0	Vin1	Vin0	AGND
0	1	Vin1	Vin3	Vin0	Vin1	Vin0	Vin1	Vin1	AGND
1	0	Vin2	Vin3	Vin2	Vin3	Vin2	Vin3	Vin2	AGND
1	1	Not Allowed		Vin2	Vin3	Vin2	Vin3	Vin3	AGND

Table 10. Power Mode Selection

PM1	**PM0**	**Description**
1	**1**	**Full Shutdown Mode,** In this mode all internal circuitry on the AD7324 is powered down. Information in the Control register is retained when the AD7324 is in Full Shutdown Mode.
1	**0**	**Auto Shutdown Mode,** The AD7324 will enter Full Shut down at the end of each conversion when the control register is updated. All internal circuitry is powered down in Full Shutdown.
0	**1**	**Auto Standby Mode,** In this mode all internal circuitry is powered down excluding the internal Reference. The AD7324 will enter Auto Standby Mode at the end of the Conversion after the control register is updated.
0	**0**	**Normal Mode,** All internal Circuitry is powered up at all times.

Table 11. Sequencer Selection

Seq1	Seq2	Sequence type
0	0	The Channel Sequencer is not used. The Analog Channel selected by programming the ADD1 and ADD0 bits in the Control Register selects the next channel for conversion.
0	1	This selects the Sequence of Channels as previously programmed in the Sequence register for conversion. The AD7324 will start converting on the lowest channel in the sequence. It converts the channels in ascending order. If uninterrupted the AD7324 will keep converting the sequence. The range for each channel selected will default to the Ranges previously written into the Range Registers.
1	0	This Configuration is used in conjunction with the Channel Address Bits in the Control Register. It allows continuous conversions on a consecutive sequence of channels, from channel 0, up to and including, a final channel selected by the Channel Address Bits in the control register. The range for each channel will default to the Ranges previously written into the Range Registers.
1	1	The Channel Sequencer is not used. The Analog Channel selected by programming the ADD1 and ADD0 bits in the Control Register selects the next channel for conversion.

THE SEQUENCE REGISTER

The Sequence Register on the AD7324 is a 4-Bit Write only register. Each of the four Analog input channels has one corresponding bit in the Sequence Register. To select a channel for inclusion in the sequence set the corresponding channel bit to 1 in the Sequence Register.

Table 12. Sequencer Register

MSB LSB

Write	Register Select 1	Register Select 2	Vin0	Vin1	Vin2	Vin3	0	0	0	0	0	0	0	0	0

RANGE REGISTER

The Range register to used to select one Analog input Range per Analog input channel. Range. It is an 8-Bit write only Register, with two dedicated Range bits for each of the Analog Input Channels from Channel 0 to Channel3 . There are four Analog input Ranges to choose from, ±10V, ±5V, ±2.5V, 0 to 10V. A write to the Range Register is selected by setting the Write bit to 1 and the Register Select bits to 0, 1. Once the initial write to the Range Register occurs the AD7324 automatically configures the Analog inputs from Channel 0 to Channel 3 to the appropriate range, as indicated by the Range register, each time any one of these analog input channels is selected. The ±10V input Range is selected by default on each analog input channel. See Table 13.

Table 13. Range Register

MSB LSB

Write	Reg Select 1	Reg Select2	Vin0A	Vin0B	Vin1A	Vin1B	Vin2A	Vin2B	Vin3A	Vin3B	0	0	0	0	0

VinXA	VinXB	Description
0	0	This combination selects the ± 10V Input Range on Analog Input X.
0	1	This combination selects the ±5V Input Range on Analog Input X.
1	0	This combination selects the ± 2.5V Input Range on Analog Input X.
1	1	This combination selects the 0 to 10V Input Range on Analog Input X.

SEQUENCER OPERATION

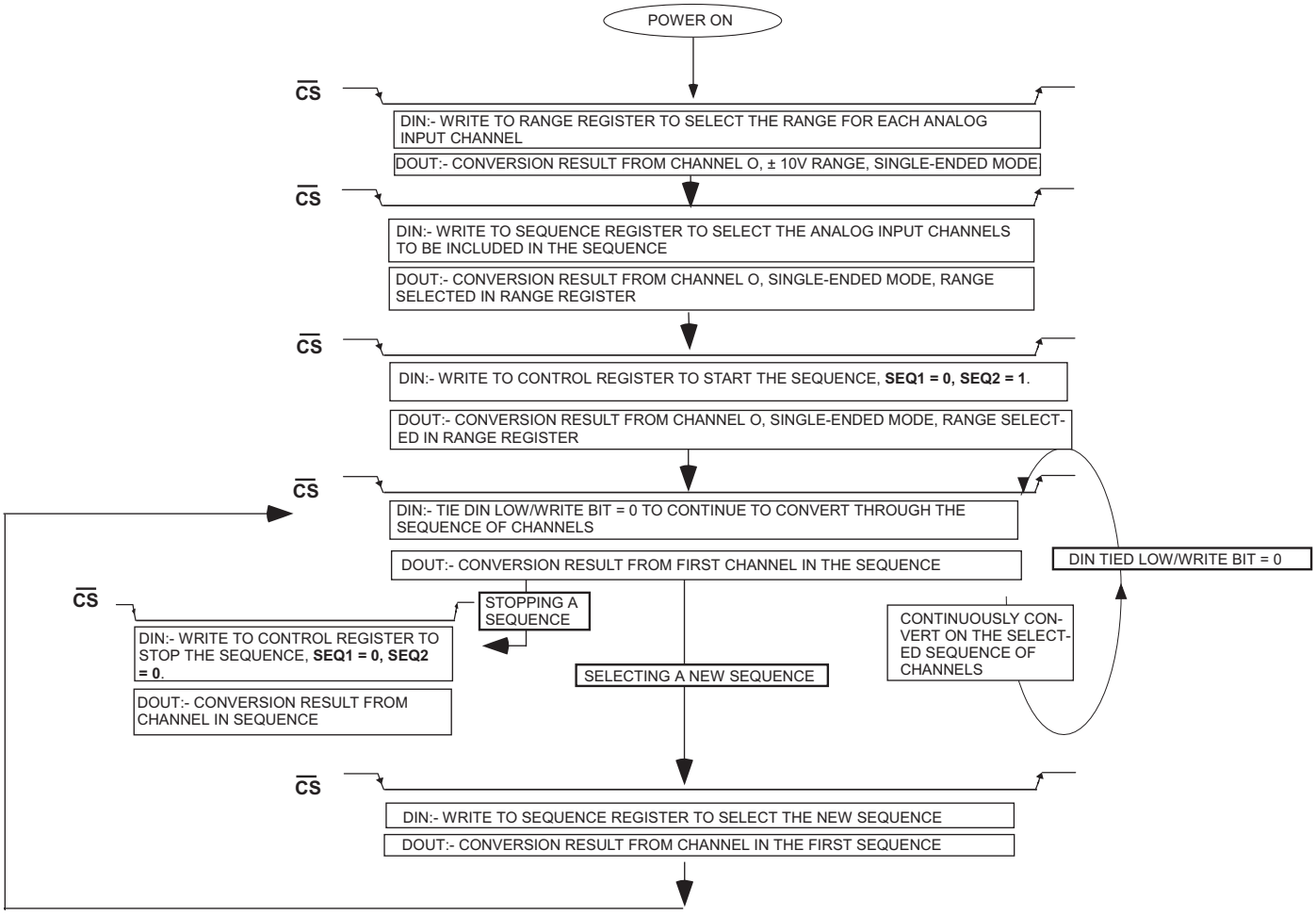


Figure 13. Programmable sequence Flow Chart

The AD7324 can be configured to automatically cycle through a number of selected channels using the on-chip sequence register and the SEQ1 and SEQ2 bits in the control register. Figure 13 shows how to program the AD7324 register in order to operate in sequence mode.

After power up all of the three on-chip registers will contain default values. Each analog input will have a default input range of ± 10V. If different Analog input ranges are required then a write to the range register is required, this is shown in the first serial transfer in Figure 13. This initial serial transfer is only necessary if Input ranges other than the default Ranges are required. After the Analog Input ranges are configured a write to the Sequence register is necessary to select the channels to be included in the sequence. Once the channels for the sequence have been selected, the sequence can be initiated by writing to the control register and setting the SEQ1 =0, SEQ2 = 1. The AD7324 will continue to convert through the selected sequence uninterrupted provided the Sequence Register remains unchanged and SEQ1 = 0 and SEQ2 = 1 in the Control Register.

If during a sequence a change to one of the range registers is required, it is first necessary to stop the sequence by writing to the Control Register and setting SEQ1 = 0 and SEQ2 = 0. Next the write to the range register can be completed to change the required range. Then the previously selected sequence can be initiated again by writing to the Control Register and setting SEQ1 = 0 and SEQ2 = 1, the ADC will then convert on the first channel in the sequence.

The AD7324 can be configured to convert a sequence of consecutive channels, See Figure 14. This sequence will begin by converting on channel 0 and end with a final channel as selected by bits ADD1 to ADD0 in the Control Register. In this configuration there is no need for a write to the Sequence register. To operate the AD7324 in this mode set SEQ1 = 1 and SEQ2 = 0 and select the final channel in the sequence by programming bits ADD1 to ADD0 in the Control Register. Once the control register is configured to operate the AD7324 in this mode the DIN line can be held low or the WRITE bit can be set to 0, the AD7324 will then continue operating in this

mode. To return to traditional multichannel operation a write to the Control Register is necessary, setting SEQ1 = 0 and SEQ2 =0.

When the SEQ1 and SEQ2 are both set to 0 or when both are set to 1 the AD7324 is configured to operate in traditional Multichannel mode where a write to the channel Address bits, ADD1 to ADD0, in the Control Register selects the next channel for conversion. In traditional multichannel mode it is necessary to write to the AD7324 in each serial transfer to select the next channel for conversion. However if a number of conversions are required on one channel then one write to the control register is necessary to select this channel via the channel address bits, ADD1, ADD0. The DIN line can then be held low or the write bit set to zero during the require number of conversions.

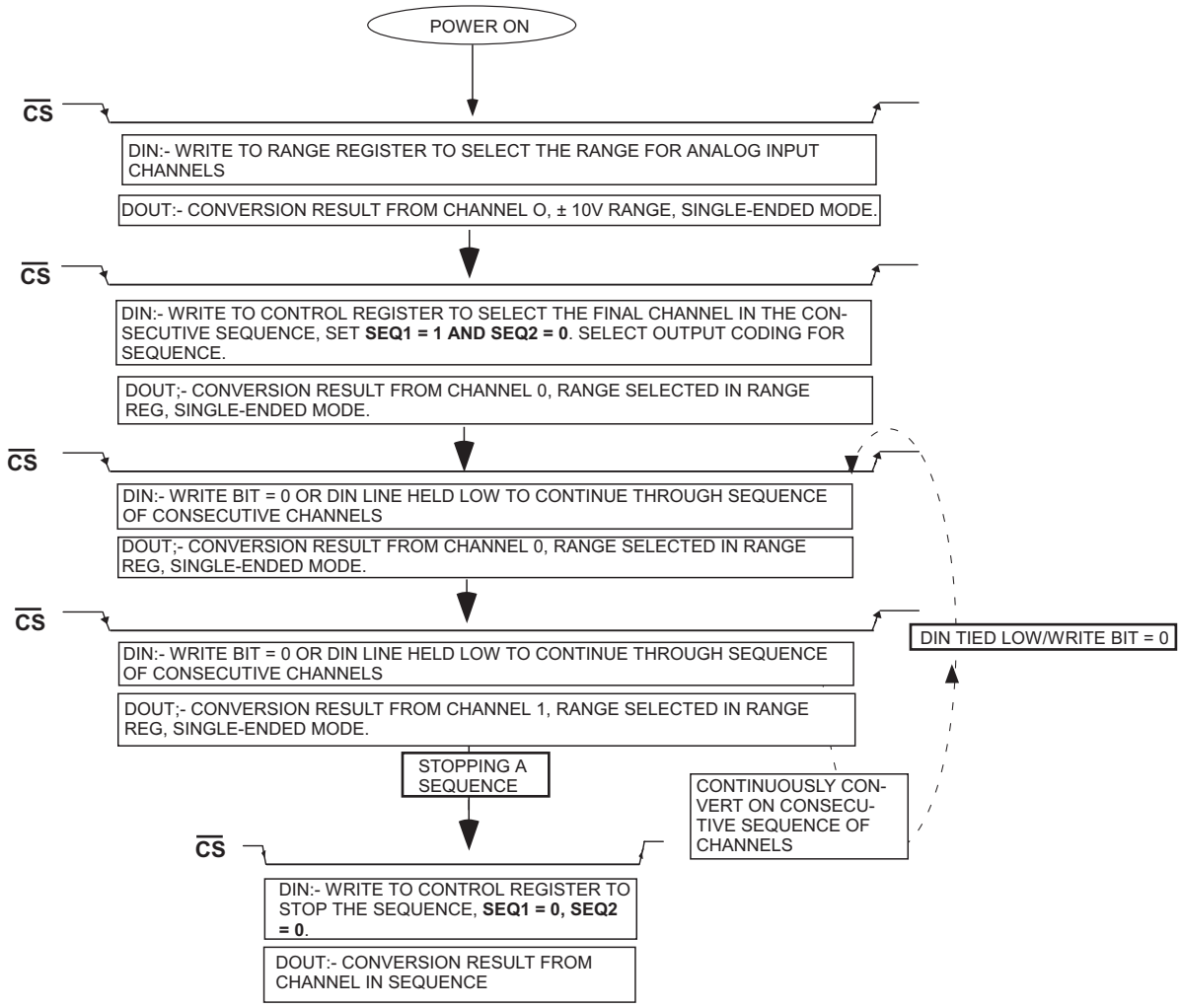


Figure 14. Flow Chart for Consecutive Sequence of Channels

REFERENCE

The AD7324 can operate with either the internal 2.5V on-chip reference or an externally applied reference. The internal reference is selected by setting the REF bit in the Control Register to 1. On power up the REF bit will be 0, selecting the external Reference for the AD7324 conversion. For external reference operation the REF_{IN}/REF_{OUT} pin should be decoupled to AGND with a 470 nF capacitor.

The internal Reference circuitry consists of a 2.5V band gap reference and a reference buffer. When operating the AD7324 in internal Reference mode the 2.5V internal reference is available at the REF_{IN}/REF_{OUT} pin. When using the AD7324 with the internal reference the REFIN/REFOUT pin should be decoupled to AGND using a 470 nF cap. It is recommended that the Internal Reference be buffered before applying it else where in the system.

The AD7324 is specified for a 2.5V to 3V reference range. When a 3V reference is selected the ranges will be, ±12V, ±6V, ±3V and 0 to 12V. For these ranges the V_{DD} and V_{SS} supply must be equal to or greater than the max Analog Input Range selected.

On power up if the internal reference operation is required for the ADC conversion, a write to the control register is necessary to set the REF bit to 1. During the Control Register write the conversion result from the first initial conversion will be invalid. The reference buffer will require TBD us to power up and charge the 470 nF decoupling cap, during the power up time the conversion result from the ADC will be invalid.

MODES OF OPERATION

The AD7324 has a number of different modes of operation. These modes are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for the differing application requirements. The mode of operation of the AD7324 is controlled by the Power Management bits, PM1 and PM0, in the Control register as detailed in **Table 10**.The default mode is Normal Mode, where all internal circuitry is fully powered up.

Normal Mode (PM1 = PM0 = 0)

This mode is intended for the fastest throughput rate performance, the AD7324 is fully powered up at all times. Figure 15 shows the general diagram of operation of the AD7324 in Normal Mode.

The Conversion is initiated on the falling edge of $\overline{CS}$ and the track and hold will enter hold mode as described in the Serial Interface Section. The Data on the DIN line during the 16 SCLK transfer will be loaded into one of the on-chip registers, provided the Write bit is set. The register is selected by programming the Register select bits, see **Table 7** of the Register section.

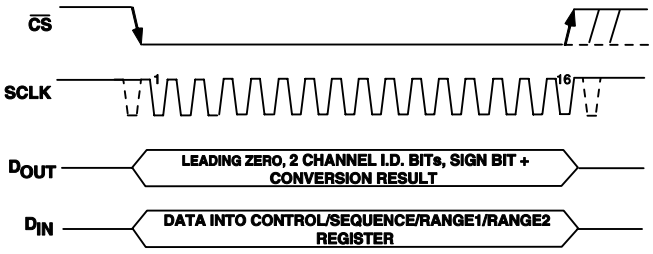


Figure 15. Normal Mode

The AD7324 will remain fully powered up at the end of the conversion provided both PM1 and PM0 contain 0 in the control Register.

Sixteen serial clock cycles are required to complete the conversion and access the conversion result. At the end of the conversion $\overline{CS}$ may idle high until the next conversion or may idle low until sometime prior to the next conversion.

Once the data transfer is complete, another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed.

Full Shutdown Mode (PM1 = PM0 = 1)

In this mode all internal circuitry on the AD7324 is powered down. The part retains information in the Registers during Full Shut down. The AD7324 remains in Full shutdown mode until the power managements bits in the Control Register, PM1 and PM0, are changed.

If a write to the control register occurs while the part is in Full Shut down mode, with the power management bits, PM1 and PM0 set to 0, normal mode, the part will begin to power up on the $\overline{CS}$ rising edge.

To ensure the AD7324 is fully powered up, $t_{POWER\ UP}$, should elapse before the next $\overline{CS}$ falling edge.

Auto Shutdown Mode (PM1 = 1, PM0 = 0)

Once the Auto Shutdown mode is selected the AD7324 will automatically enter shutdown at the end of each conversion. The AD7324 retains information in the registers during Shutdown. The track-and-hold is in hold during shutdown. On the falling $\overline{CS}$ edge, the track-and-hold that was in hold during shutdown will return to track.

The power-up from Auto Shutdown is TBD μs

In this mode the power consumption of the AD7324 is greatly reduced with the part entering shutdown at the end of each conversion. When the control registers is programmed to move into Auto Shutdown mode, it does so at the end of the conversion.

Auto Standby Mode (PM1 = 0, PM0 =1)

In Auto Standby mode portions of the AD7324 are powered down but the on-chip reference remains powered up. The reference bit in the Control register should be 0 to ensure the on-chip reference is enabled. This mode is similar to Auto Shutdown but allows the AD7324 to power up much faster, allowing faster throughput rates to be achieved.

The AD7324 will enter standby at the end of the conversion. The part retains information in the Registers during Standby. The AD7324 will remain in standby until it receives a $\overline{CS}$ falling edge. The ADC will begin to power up on the $\overline{CS}$ falling edge. On this $\overline{CS}$ falling edge the track-and-hold that was in hold mode while the part was in Standby will return to track. Wake-up time from Standby is 1 μs. The user should ensure that 1 μs has elapsed before attempting a valid conversion. When running the AD7324 with the maximum 20 MHz SCLK, one dummy conversion of 16 x SCLKs is sufficient to power up the ADC. This dummy conversion effectively halves the throughput rate of the AD7324, with every second conversion result being a valid result. Once Auto Standby mode is selected, the ADC can move in and out of the low power state by controlling the $\overline{CS}$ signal.

SERIAL INTERFACE

Figure 16 shows the timing diagram for the serial interface of the AD7324. The serial clock applied to the SCLK pin provides the conversion clock and also controls the transfer of information to and from the AD7324 during a conversion.

The $\overline{CS}$ signal initiates the data transfer and the conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, take the bus out of three-state and the analog input signal is sampled at this point. Once the conversion is initiated it will require 16 SCLK cycles to complete.

The track-and-hold will go back into track on the 15th SCLK falling edge. On the sixteenth SCLK falling edge, the DOUT line will return to three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLK cycles have elapsed, the conversion will be terminated, the DOUT line will return to three-state, and depending on when the $\overline{CS}$ signal is brought high the addressed register may or may not be updated. Data is clocked into the AD7324 on the SCLK falling edge. The three MSB on the DIN line are decoded to select which register is being addressed. The Control Register is an eleven bit register, if the control register is addressed by the three MSB, the data on the DIN line will be loaded into the Control on the 15th SCLK falling edge. If the Sequence register or the Range register is addressed the data on the DIN line will be loaded into the addressed register on the 11th SCLK falling edge.

Conversion data is clocked out of the AD7324 on each SCLK falling edge. Data on the DOUT line will consist of two leading zeros, two channel identifier bits and the 12-Bit Plus Sign conversion result. The channel identifier bits are used to indicate which channel the conversion result corresponds to.

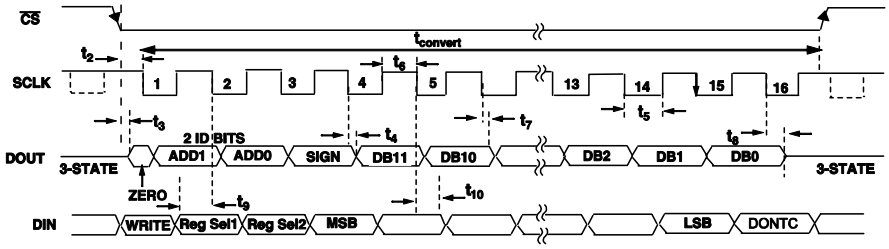
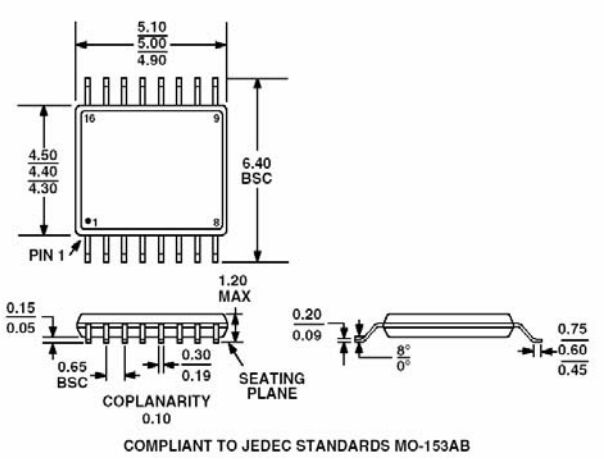


Figure 16. Serial Interface timing Diagram (Control register write)

OUTLINE DIMENSIONS

16-Lead Thin Shrink Small Outline (TSSOP)

(RU-16)



Ordering Guide

AD7324 Products	Temperature Package	Package Description	Package Outline
AD7324BRUZ	–40°C to +85°C	TSSOP	RU-16
EVAL-AD7324CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	

NOTES

1 This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL Board for evaluation/demonstration purposes.

2 This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board, e.g., EVAL-AD7324CB, the EVAL-CONTROL BRD2, and a 12V transformer must be ordered. See relevant Evaluation Board Technical note for more information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.