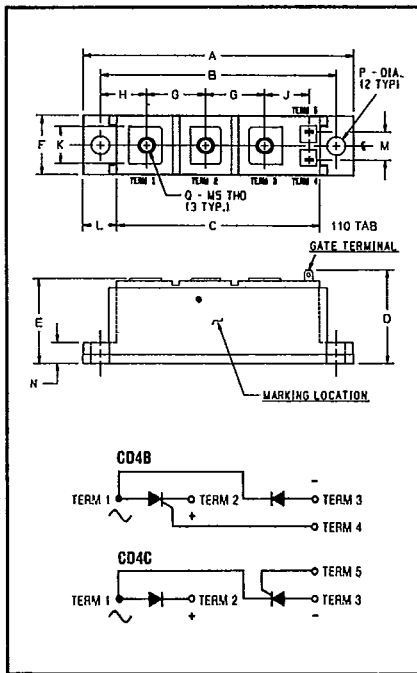




CD4B \_\_\_ 90  
CD4C \_\_\_ 90

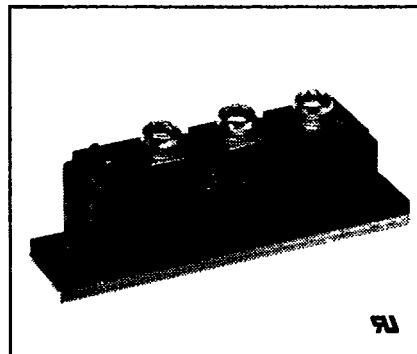
Powerex, Inc., Hillis Street, Youngwood, Pennsylvania 15697 (412) 925-7272  
Powerex Europe, S.A., 428 Avenue G. Durand, BP107, 72003 Le Mans, France (43) 72.75.15

**SCR/Diode  
POW-R-BLOK™ Modules  
90 Amperes/1200-1600 Volts**



**1200-1600 Volts  
CD4B \_\_\_ 90, CD4C \_\_\_ 90  
Outline Drawing**

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	3.602	3.640	91.49	92.45
B	3.146	3.154	79.91	80.11
C	2.705	2.735	68.71	69.47
D	1.24	1.28	31.50	32.51
E	1.125	1.165	28.58	29.59
F	.795	.805	20.19	20.45
G	.788	.798	19.76	20.27
H	.608	.628	15.44	15.95
J	.585	.605	14.86	15.36
K	.480	.520	12.19	13.21
L	.43	.47	10.92	11.94
M	.36	.40	9.14	10.16
N	.265	.285	6.73	7.24
P	.245	.255	6.22	6.48
Q	—	—	M5 x 0.8	



**CD4B \_\_\_ 90, CD4C \_\_\_ 90  
SCR/Diode POW-R-BLOK™ Modules  
90 Amperes/1200-1600 Volts**

**Ordering Information**

Example: Select the complete eight digit rating module part number you desire from the table — i.e. CD4B1290 is a 1200 Volt, 90 Ampere SCR/Diode POW-R-BLOK™ Module.

Type	V <sub>RRM</sub> Volts (x100)	Current Rating Amperes (90)
CD4B	12	90
CD4C	14	90
	16	

**Description**

Powerex SCR/Diode POW-R-BLOK™ Modules combine multiple power semiconductor devices in a single, electrically isolated module. This dense, cost-effective packaging is made possible by Powerex's proprietary *glass passivation* process, in which each semiconductor junction is sealed with a protective layer of glass. Exhaustive testing at high voltages and high temperatures has demonstrated the excellent parameter stability of these glass-protected products.

The POW-R-BLOK™ features a self-contained electrical isolation system. The use of BeO ceramic isolators with high thermal conductivity has achieved excellent circuit-to-baseplate isolation (≥2500 volts RMS), while maintaining efficient cooling of the semiconductors. POW-R-BLOK™ has been tested and recognized by Underwriters Laboratories (QQX2 Power Switching Semiconductors).

**Features:**

- Glass Passivated Chips
- Hybrid Construction
- Isolated Base Plate
- Low Thermal Impedance
- Metal Base Plate
- UL Recognized
- Quick Connect Gate Terminals
- High dv/dt
- Low Gate Sensitivity

**Applications:**

- Motor Speed Control
- Battery Chargers
- Tap Changers
- Transfer Switches
- Lighting Controls
- Power Line Applications of 120, 240 or 480 Volts

**Benefits:**

- No Additional Insulating Components Required
- Easy Installation
- Reduced Engineering Time
- Improved Heat Transfer
- Voltage Stability



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CD4B \_\_\_ 90, CD4C \_\_\_ 90  
SCR/Diode POW-R-BLOK™ Modules  
90 Amperes/1200-1600 Volts

### Absolute Maximum Ratings

Characteristics	Symbol	CD4B1290 CD4C1290	CD4B1490 CD4C1490	CD4B1690 CD4C1690	Units
Peak Forward Blocking Voltage	V <sub>DRM</sub>	1200	1400	1600	Volts
Peak Reverse Blocking Voltage	V <sub>RRM</sub>	1200	1400	1600	Volts
Transient Peak Reverse Blocking Voltage (Non-Repetitive) t < 5 ms	V <sub>RSM</sub>	1450	1700	1950	Volts



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CD4B — 90, CD4C — 90  
SCR/Diode POW-R-BLOK™ Modules  
90 Amperes/1200-1600 Volts

### Absolute Maximum Ratings

Characteristics	Symbol	CD4B — 90 CD4C — 90	Units
RMS On-State Current	$I_{T(RMS)}, I_{F(RMS)}$	145	Amperes
Average On-State Current	$I_{T(AV)}, I_{F(AV)}$	90	Amperes
Peak One-Cycle Surge (Non-Repétitive) On-State Current (60Hz)	$I_{TSM}, I_{FSM}$	1925	Amperes
Peak Three-Cycle Surge (Non-Repétitive) On-State Current (60Hz)	$I_{TSM}, I_{FSM}$	1390	Amperes
Peak Ten-Cycle Surge (Non-Repétitive) On-State Current (60Hz)	$I_{TSM}, I_{FSM}$	1250	Amperes
Peak One-Cycle Surge (Non-Repétitive) On-State Current (50Hz)	$I_{TSM}, I_{FSM}$	1755	Amperes
$I^2t$ (for Fusing), 8.3 milliseconds	$I^2t$	15375	A <sup>2</sup> sec
Critical Rate-of-Rise of On-State Current $\text{\textcircled{D}}$ (Non-Repétitive)	$di/dt$	800	Amperes/ $\mu$ s
Peak Gate Power Dissipation	$P_{GM}$	16	Watts
Average Gate Power Dissipation	$P_{G(AV)}$	3.0	Watts
Peak Forward Gate Voltage	$V_{GFM}$	10	Volts
Peak Reverse Gate Voltage	$V_{GRM}$	5.0	Volts
Peak Forward Gate Current	$I_{GFM}$	4.0	Amperes
Storage Temperature	$T_{STG}$	-40 to 150	°C
Operating Temperature	$T_J$	-40 to 125	°C
Maximum Mounting Torque M6 Mounting Screw	—	50	in.-lb.
Maximum Terminal Torque M5 Terminal Screw	—	35	in.-lb.
Module Weight (Typical)	—	142	Grams
V Isolation	$V_{RMS}$	2500	Volts

$\text{\textcircled{D}}$  Per JEDEC STD RS-397, 5.2.26.



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CD4B \_\_\_ 90, CD4C \_\_\_ 90  
SCR/Diode POW-R-BLOK™ Modules  
90 Amperes/1200-1600 Volts

### Electrical and Thermal Characteristics, $T_J = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Test Conditions	CD4B ___ 90	Units
			CD4C ___ 90	
<b>Blocking State Maximums</b>				
Forward Leakage Current, Peak	$I_{DRM}$	$T_J = 125^\circ\text{C}$ , $V_{DRM} = \text{rated}$	15	mA
Reverse Leakage Current, Peak	$I_{RRM}$	$T_J = 125^\circ\text{C}$ , $V_{RRM} = \text{rated}$	15	mA
<b>Conducting State Maximums</b>				
Peak On-State Voltage	$V_{TM}$	$I_{TM} = 250\text{A}$	1.55	Volts
Peak On-State Voltage	$V_{FM}$	$I_{FM} = 250\text{A}$	1.3	Volts
<b>Switching Minimums</b>				
Critical Rate of Rise of Off-State Voltage	$dv/dt$	$T_J = 125^\circ\text{C}$ , Exponential to $V_{DRM}$	1000	Volts/ $\mu\text{sec}$
Typical Turn-Off Time	$t_q$	$I_{TM} = 50\text{A}$ , $T_J = 125^\circ\text{C}$ , $di/dt = 5\text{A}/\mu\text{s}$ reapplied $dv/dt = 20\text{V}/\mu\text{s}$ linear to $0.8 V_{DRM}$	100	$\mu\text{sec}$
Typical Turn-On Time	$t_{on}$	$I_{TM} = 100\text{A}$ , $V_D = 100\text{V}$	4	$\mu\text{sec}$
<b>Thermal Maximums</b>				
Thermal Resistance, Junction to Case	$R_{\theta JC}$	Per Device	0.28	$^\circ\text{C}/\text{Watt}$
Thermal Resistance, Case to Sink Lubricated	$R_{\theta CS}$	Per Device	0.2	$^\circ\text{C}/\text{Watt}$
<b>Gate Parameters Maximums</b>				
Gate Current to Trigger	$I_{GT}$	$V_D = 12\text{V}$	100	mA
Gate Voltage to Trigger	$V_{GT}$	$V_D = 12\text{V}$	3.0	Volts
Non-Triggering Gate Voltage	$V_{GDM}$	$T_J = 125^\circ\text{C}$ , $V_D = V_{DRM}$	0.15	Volts

#### WARNING:

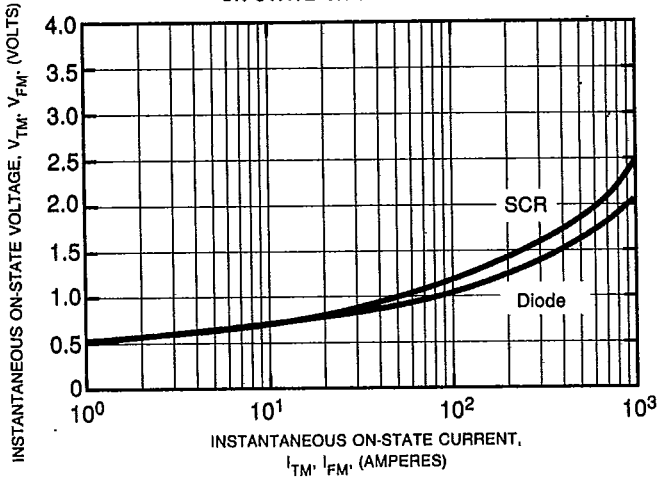
Internal insulation used is Beryllium Oxide. User should avoid grinding, crushing or abrading these portions. Care must be exercised in properly disposing of unwanted modules.



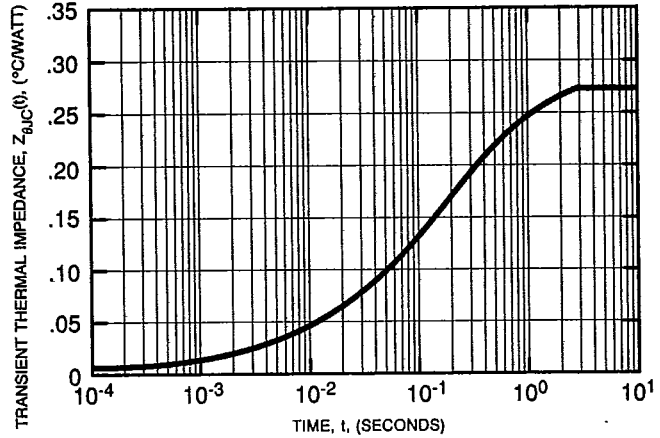
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CD4B — 90, CD4C — 90  
 SCR/Diode POW-R-BLOK™ Modules  
 90 Amperes/1200-1600 Volts

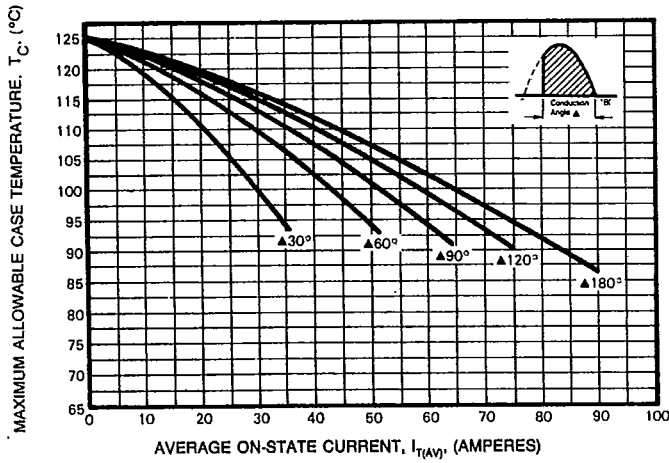
MAXIMUM ON-STATE CHARACTERISTICS



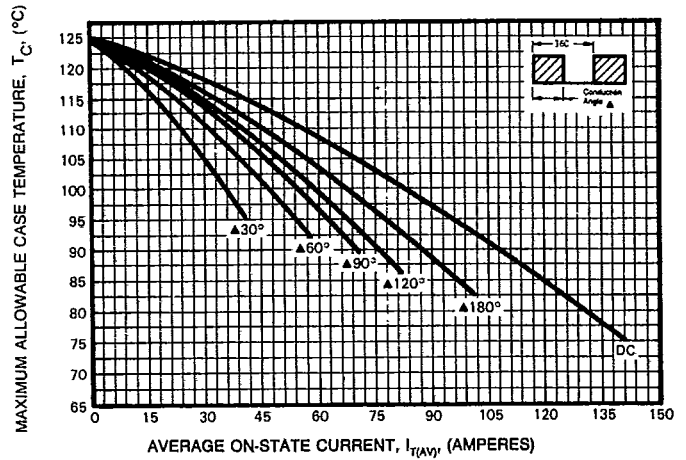
TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS (JUNCTION TO CASE)



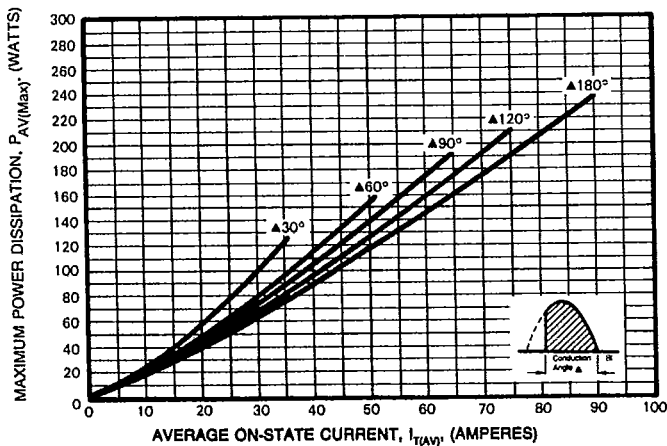
MAXIMUM ALLOWABLE CASE TEMPERATURE



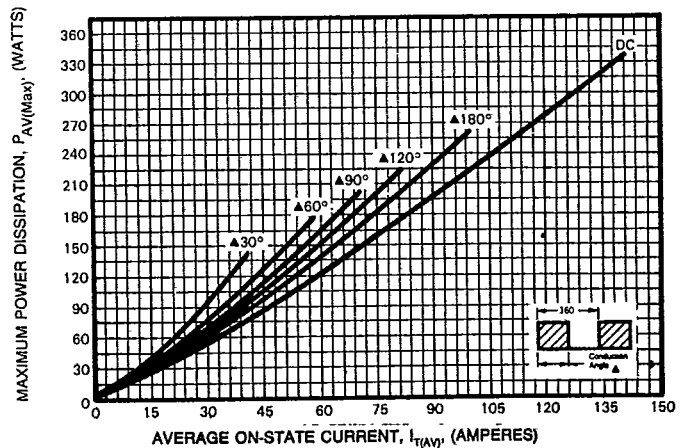
MAXIMUM ALLOWABLE CASE TEMPERATURE



MAXIMUM ON-STATE POWER DISSIPATION



MAXIMUM ON-STATE POWER DISSIPATION



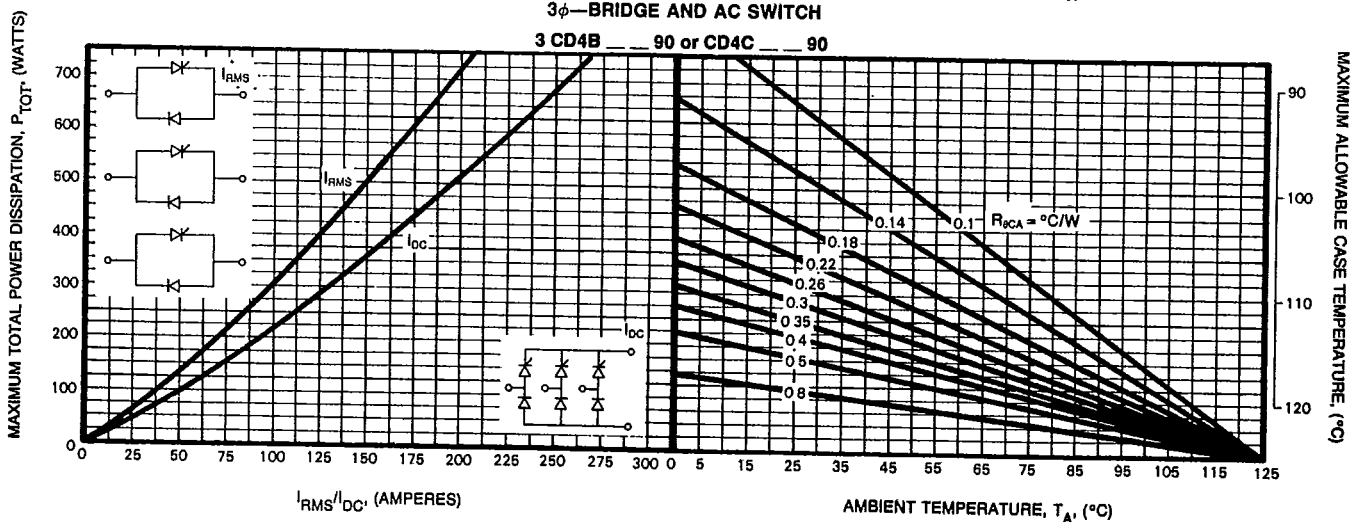
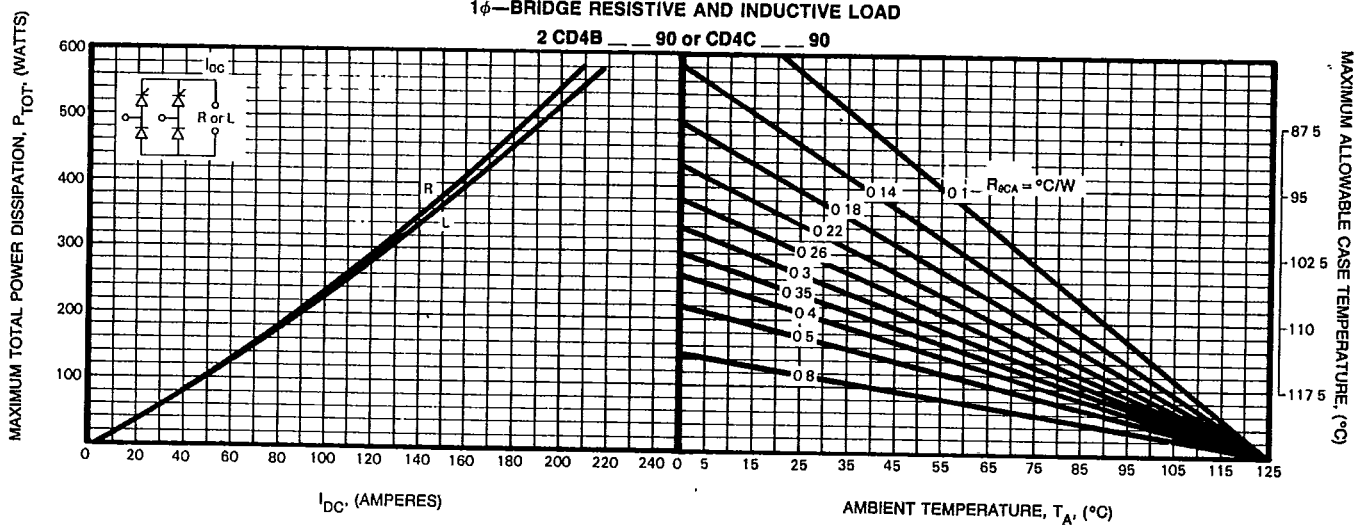
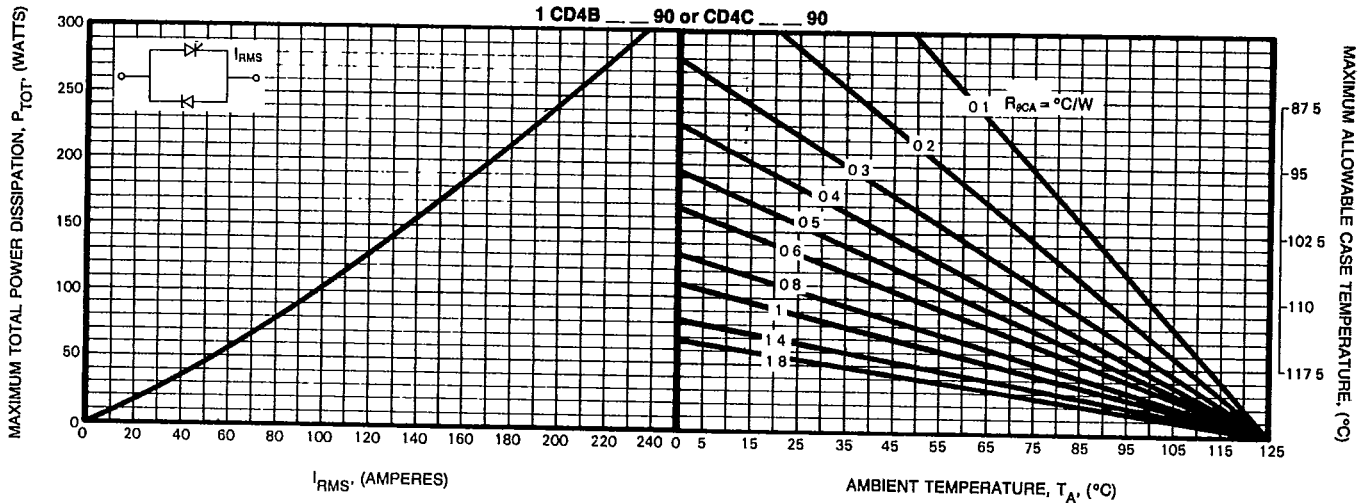


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CD4B — 90, CD4C — 90  
 SCR/Diode POW-R-BLOK™ Modules  
 90 Amperes/1200-1600 Volts

**MAXIMUM TOTAL POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURES**  
 AC SWITCH





T-91-01

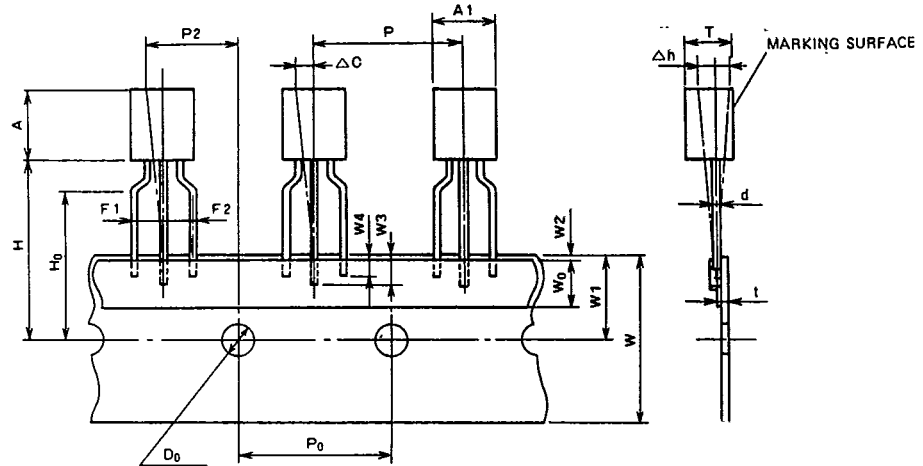
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## Taping

### STANDARD SPECIFICATIONS FOR TAPING OF MOLDED PACKAGE THYRISTORS AND TRIACS

#### TO-92 Package

Thyristor  
CR02AM, CR03AM, CR04AM  
Triac  
BCR1AM



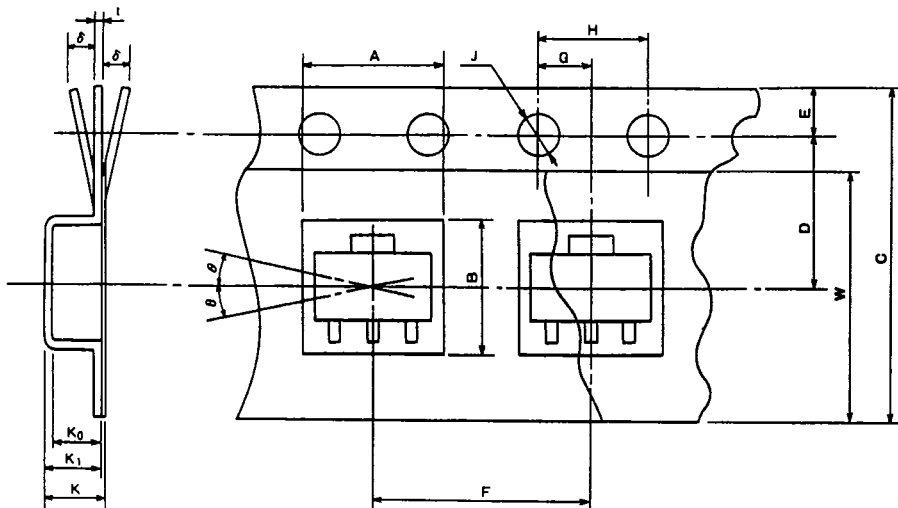
Taping dimensions

Description of symbol	Symbol	Dimensions (Unit:mm)	Remark
Product width	A1	5.0 MAX	
Product height	A	5.0 MAX	
Product thickness	T	3.7 MAX	
Lead wire diameter	d	0.6 MAX	
Sticker lead wire length (1)	W3	2.5 MIN	
Sticker lead wire length (2)	W4	2.0 MIN	
Pitch between products	P	12.7 ± 1.0	
Feed hole pitch	P <sub>0</sub>	12.7 ± 0.3	The cumulative pitch error is ± 1mm per 20 pitches.
Feed hole deviation (1)	P2	6.35 ± 1.3	
Distance between lead wires	F1, F2	2.5 ± 0.4	
Defective product (1)	Δh	0 ± 2.0	
Tape width	W	18.0 ± <sup>1.0</sup> / <sub>0.5</sub>	
Sticker tape width	W <sub>0</sub>	6.0 ± 0.5	
Feed hole deviation (2)	W1	9.0 ± 0.5	
Sticker tape deviation	W2	0.5 MAX	
Position of product bottom surface	H	17.5 MIN	
Lynch height of lead wire	H <sub>0</sub>	16.0 ± 0.5	
Feed hole diameter	D <sub>0</sub>	4.0 ± 0.2	
Tape thickness	t	0.7 ± 0.2	
Defective product (2)	ΔC	0 ± 1.0	



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Powerex Semiconductor Data Book  
 Taping



SOT-89 Package

Thyristor  
 CR08AS

Taping dimensions

Description of symbol		Symbol	Dimensions/angles Unit:mm	Remark
Parts Insertion	Height	A	$5.0 \pm 0.1$	Cross-section of the surface 0.5mm above the Inner bottom
	Width	B	$4.6 \pm 0.1$	Cross-section of the surface 0.5mm above the inner bottom
Concave square hole	Depth	$K_0$	$1.8 \pm 0.1$	Inner space
	Pitch	F	$8.0 \pm 0.1$	Cumulative error +0.1/-0.3 MAX/10 pitches
Round feed hole	Diameter	J	$\phi 1.5 \pm 0.05$	
	Pitch	H	$4.0 \pm 0.1$	Cumulative error +0.1/-0.3 MAX/10 pitches
	Position	E	$1.5 \pm 0.1$	Distance between the tape edge and the hole center
Distance between center lines	Vertical	G	$2.0 \pm 0.5$	Center line of concave square hole and round feed hole
	Horizontal	D	$5.65 \pm 0.05$	Center line of concave square hole and round feed hole
Cover tape	Width	W	$9.5 + 0.3/-0$	Thickness: 0.1 MAX
Carrier tape	Width	C	$12 \pm 0.2$	Warp $\pm 0.3$ MAX
	Thickness	t	$0.3 \pm 0.05$	
	Package hole depth	$K_1$	$2.1 \pm 0.1$	
Device	Package dimensions	—	—	As shown in (e)
	Inclination	$\theta$	30° MAX.	
Total Thickness		K	$2.3 \pm 0.1$	Total thickness including cover and carrier tapes