DDR SDRAM Module 256Mbyte (32Mx72bit), based on32Mx8,4Banks, 8K Ref., ECC Unbuffered SO-DIMM Part No. HDD32M72B9

GENERAL DESCRIPTION

The HDD32M72B9 is a 32M x 72 bit Double Data Rate(DDR) Synchronous Dynamic RAM high-density memory module. The module consists of nine CMOS 32M x 8 bit with 4banks DDR SDRAMs in 66pin TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 200-pin glass-epoxy. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The HDD32M72B9 is a SO-DIMM(Small Outline Dual in line Memory Module) .Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications. All module components may be powered from a single 2.5V DC power supply and all inputs and outputs are SSTL_2 compatible.

FEATURES

• Part Identification

HDD32M72B9 – 16B : 166MHz (CL=2.5)

HDD32M72B9 – 13A : 133MHz (CL=2)

HDD32M72B9 – 13B : 133MHz (CL=2.5)

• 256MB(32Mx64) Unbuffered DDR SO-DIMM based on 32Mx8 DDR SDRSM with ECC

• 2.5V ± 0.2V VDD and VDDQ power supply

• Auto & self refresh capability (8192 Cycles/64ms)

• All input and output are compatible with SSTL_2 interface

• Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock

• All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock

• MRS cycle with address key programs

- Latency (Access from column address) : 2, 2.5
- Burst length : 2, 4, 8
- Burst type : Sequential & Interleave

• Data(DQ), Data strobes and write masks latched on the rising and falling edges of the clock

• All Addresses and control inputs except Data(DQ), Data strobes and Data masks latched on the rising edges of the clock

• The used device is 8M x 8bit x 4Banks DDR SDRAM

• Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)

• Serial Presence detect with EEPROM

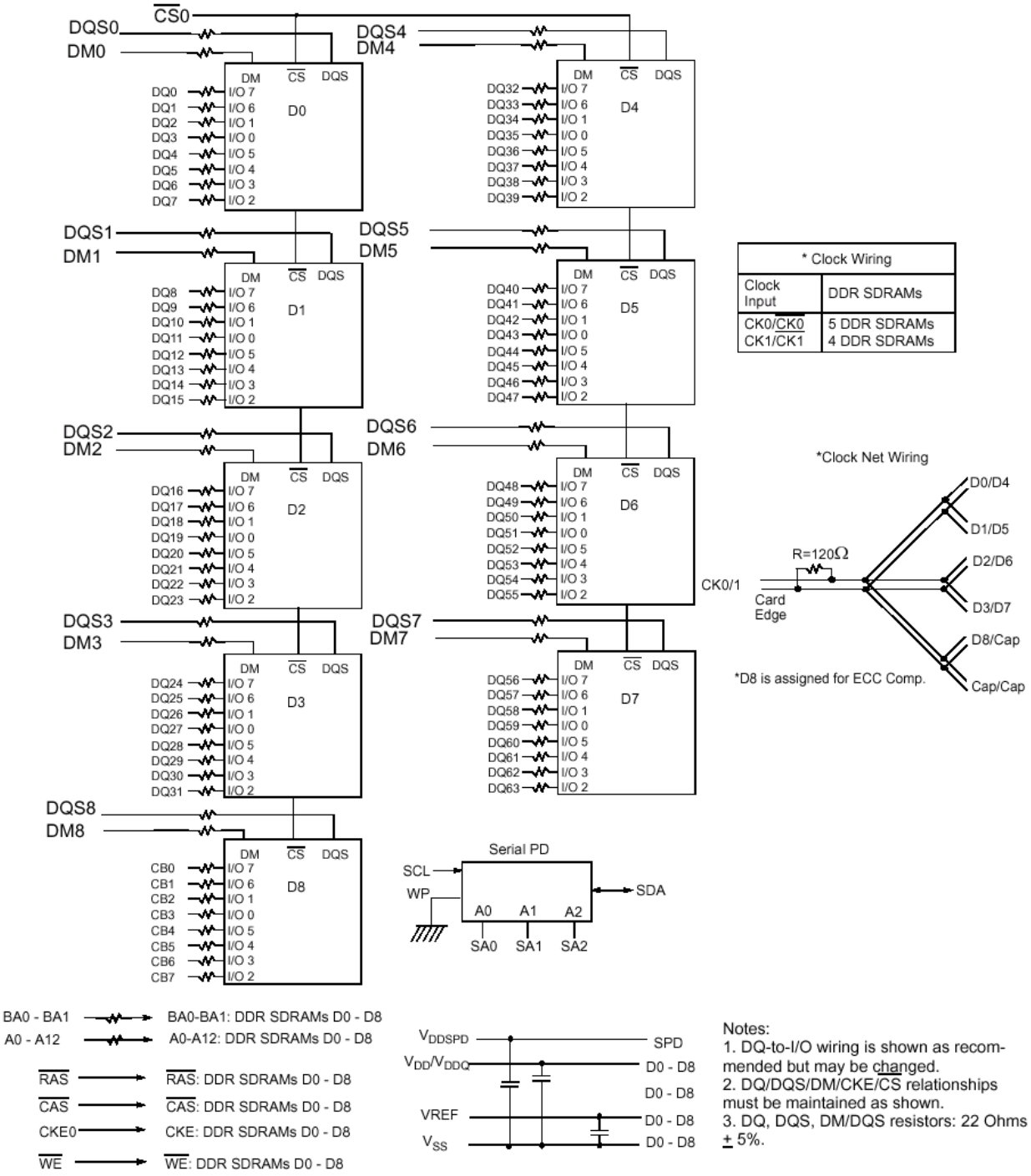
PIN ASSIGNMENT

PIN	Front	PIN	Back	PIN	Frontl	PIN	Back	PIN	Front	PIN	Back
1	VREF	2	VREF	67	DQ27	68	DQ31	133	DQS4	134	DM4
3	VSS	4	VSS	69	VDD	70	VDD	135	DQ34	136	DQ38
5	DQ0	6	DQ4	71	CB0	72	CB4	137	VSS	138	VSS
7	DQ1	8	DQ5	73	CB1	74	CB5	139	DQ35	140	DQ39
9	VDD	10	VDD	75	Vss	76	Vss	141	DQ40	142	DQ44
11	DQS0	12	DM0	77	DQS8	78	DM8	143	VDD	144	VDD
13	DQ2	14	DQ6	79	CB2	80	CB6	145	DQ41	146	DQ45
15	VSS	16	VSS	81	VDD	82	VDD	147	DQS5	148	DM5
17	DQ3	18	DQ7	83	CB3	84	CB7	149	VSS	150	VSS
19	DQ8	20	DQ12	85	NC	86	NC(/RESET)	151	DQ42	152	DQ46
21	VDD	22	VDD	87	VSS	88	VSS	153	DQ43	154	DQ47
23	DQ9	24	DQ13	89	CK2	90	VSS	155	VDD	156	VDD
25	DQS1	26	DM1	91	/CK2	92	VDD	157	VDD	158	/CK1
27	VSS	28	VSS	93	VDD	94	VDD	159	VSS	160	CK1
29	DQ10	30	DQ14	95	CKE1	96	CKE0	161	VSS	162	VSS
31	DQ11	32	DQ15	97	NC(A13)	98	NC (BA2)	163	DQ48	164	DQ52
33	VDD	34	VDD	99	A12	100	A11	165	DQ49	166	DQ53
35	CK0	36	VDD	101	A9	102	A8	167	VDD	168	VDD
37	/CK0	38	VSS	103	VSS	104	VSS	169	DQS6	170	DM6
39	VSS	40	VSS	105	A7	106	A6	171	DQ50	172	DQ54
41	DQ16	42	DQ20	107	A5	108	A4	173	VSS	174	VSS
43	DQ17	44	DQ21	109	A3	110	A2	175	DQ51	176	DQ55
45	VDD	46	VDD	111	A1	112	A0	177	DQ56	178	DQ60
47	DQS2	48	DM2	113	VDD	114	VDD	179	VDD	180	VDD
49	DQ18	50	DQ22	115	A10/AP	116	BA1	181	DQ57	182	DQ61
51	VSS	52	VSS	117	BA0	118	/RAS	183	DQS7	184	DM7
53	DQ19	54	DQ23	119	/WE	120	/CAS	185	VSS	186	VSS
55	DQ24	56	DQ28	121	/CS0	122	NC	187	DQ58	188	DQ62
57	VDD	58	VDD	123	NC	124	NC	189	DQ59	190	DQ63
59	DQ25	60	DQ29	125	VSS	126	VSS	191	VDD	192	VDD
61	DQS3	62	DM3	127	DQ32	128	DQ36	193	SDA	194	*SA0
63	VSS	64	VSS	129	DQ33	130	DQ37	195	SCL	196	*SA1
65	DQ26	66	DQ30	131	VDD	132	VDD	197	VDDSPD	198	*SA2
								199	VDDID	200	NC

*These pins should be NC in the system which does not support SPD

PIN	PIN DESCRIPTION	PIN	PIN DESCRIPTION
A0~A12	Address input	VDD	Power supply(2.5V)
BA0~BA1	Bank Select Address	VDDQ	Power supply for DQs(2.5V)
DQ0~DQ63(CB0~CB7)	Data input/output (Check Bit Data In/Out)	VREF	Power supply for reference
DQS0~DQS8	Data Strobe input/output	VDDSPD	Serial EEPROM Power supply(2.3V~3.3V)
DM0~DM8	Data-in Mask	VSS	Ground
CK0~CK2,/CK0~/CK2	Clock input	SA0~SA2	Address in EEPROM
CKE0~CKE1	Clock enable input	SDA	Serial data I/O
/CS0	Chip Select input	SCL	Serial clock
/RAS, /CAS	Row / Column Address strobe	WP	Write protection
NC	No connection	VDDID	VDD identification flag

FUNCTIONAL BLOCK DIAGRAM



* Clock Wiring	
Clock Input	DDR SDRAMs
CK0/CK0	5 DDR SDRAMs
CK1/CK1	4 DDR SDRAMs

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms ± 5%.

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CK, /CK	Clock	CK and CK are differential clock inputs. All address and control input signals are sam-pled on the positive edge of CK and negative edge of CK. Output (read) data is referenced to both edges of CK. Internal clock signals are derived from CK/CK.
CKE	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, CK and CKE are disabled during power-down and self refresh modes, providing low standby power. CKE will recognizean LVCMOS LOW level prior to VREF being stable on power-up.
/CS	Chip Select	CS enables(registered LOW) and disables(registered HIGH) the command decoder. All commands are masked when CS is registered HIGH. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
A0 ~ A12	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRE-CHARGE command is being applied.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQS0 ~ 8	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, cen-tered in write data. Used to capture write data.
DM0~8	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to matches the DQ and DQS load-ing.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	Check Bit	Check Bits for ECC data are multiplexed on the same pins.
VDDQ	Supply	DQ Power Supply : +2.5V ± 0.2V.
VDD	Supply	Power Supply : +2.5V ± 0.2V (device specific).
VSS	Supply	DQ Ground.
VREF	Supply	SSTL_2 reference voltage.
VDDSPD	Supply	Serial EEPROM Power Supply : 3.3v
VDDID		VDD identification Flag

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNTE
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	8.0	W
Short circuit current	I_{OS}	50	mA

Notes : Permanent device damage may occur if ABSOLUTE MAXIUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 IN/OUT)

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference Voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination Voltage(system)	V_{TT}	V_{REF} – 0.04	V_{REF} + 0.04	V	2
Input High Voltage	V_{IH} (DC)	V_{REF} + 0.15	V_{REF} + 0.3	V	4
Input Low Voltage	V_{IL} (DC)	-0.3	V_{REF} - 0.15	V	4
Input Voltage Level, CK and /CK inputs	V_{IN} (DC)	-0.3	V_{DDQ} + 0.3	V	
Input Differential Voltage, CK and /CK inputs	V_{ID} (DC)	0.3	V_{DDQ} + 0.6	V	3
Input leakage current	I_{LI}	-2	2	uA	5
Output leakage current	I_{OZ}	-5	5	uA	
Output High current (Normal Strenth driver (V_{OUT} = V_{TT} + 0.84V)	I_{OH}	-16.8		mA	
Output Low current (Normal Strenth driver (V_{OUT} = V_{TT} - 0.84V)	I_{OL}	16.8			
Output High current (Normal Strenth driver (V_{OUT} = V_{TT} + 0.45V)	I_{OH}	-9			
Output Low current (Normal Strenth driver (V_{OUT} = V_{TT} - 0.45V)	I_{OL}	9		mA	

Notes :

1. Includes ±25mV margin for DC offset on VREF, and a combined total of ±50mV margin for all AC noise and DC offset on VREF,bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of ¡Â3nH.
2. VTT is not applied directly to the device. V TT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on CK.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
6. These characterictеristics obey the SSTL-2 class II standards.

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, V_{DD} = 2.5V, T =25°C)

Symbol		16B(DDR333@CL=2.5)	13A(DDR266@CL=2)	13B(DDR266@CL=2.5)	Unit	Notes
IDD0		810	720	720	mA	
IDD1		1080	990	990	mA	
IDD2P		27	27	27	mA	
IDD2F		225	180	180	mA	
IDD2Q		80	165	165	mA	
IDD3P		315	270	270	mA	
IDD3N		495	405	405	mA	
IDD4R		1,530	1,260	1,260	mA	
IDD4W		1,530	1,260	1,260	mA	
IDD5		1,620	1,480	1,480	mA	
IDD6	Normal	27	27	27	mA	
	Low power	14	14	14	mA	Optional
IDD7A		2,920	2,520	2,520	mA	

Module IDD was calculated on the basis of component I DD and can be differently measured according to DQ loading cap.

AC OPERATING CONDITIONS

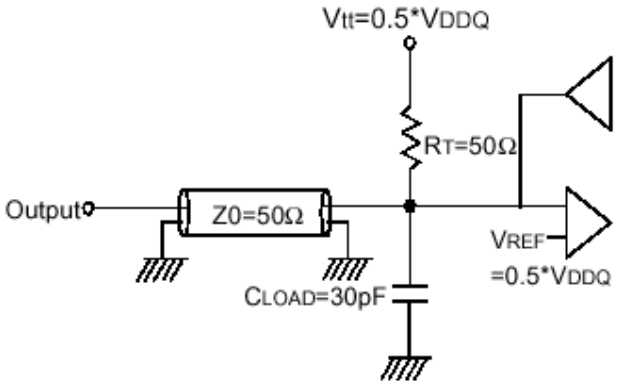
PARAMETER	STMBOL	MIN	MAX	UNIT	NOTE
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{IH} (AC)	VREF + 0.31			3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V_{IL} (AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V_{ID} (AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V_{IX} (AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Notes:

1. VID is the magnitude of the difference between the input level on CK and the input on CK*.
2. The value of V_{IX} is expected to equal 0.5* V_{DDQ} of the transmitting device and must track variations in the DC level of the same
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simula-tion. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS

PARAMETER	VALUE	UNIT	NOTE
Input reference voltage for Clock	0.5 * V_{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	VREF+0.31/VREF-0.31	V	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{TT}	V	
Output load condition	See Load Circuit	V	



(Fig. 1) Output Load Circuit (SSTL_2)

CAPACITANCE (V_{DD} = min to max, V_{DDQ} = 2.5V to 2.7V, T_A = 25°C, f = 100MHz)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A12, BA0~BA1, /RAS, /CAS,/WE)	C_{IN1}		44	pF
Input capacitance(CKE0,CKE1)	C_{IN2}		44	pF
Input capacitance(/CS0)	C_{IN3}		42	pF
Input capacitance(CK0~CK2, /CK0~/CK2)	C_{IN4}		38	pF
Input capacitance(DM0~DM8)	C_{IN5}		9	pF
Data input/output capacitance (DQ0 ~ DQ63, DQS0~DQS7)	C_{OUT1}		9	pF
Input capacitance(CB0~CB8)	C_{OUT2}		9	pF

AC CHARACTERISTICS (These AC charicteristics were tested on the Component)

PARAMETER		SYMBOL	DDR333 -16A		DDR266A -13A		DDR266B -13B		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
Row cycle time		t_{RC}	60		65		65		ns	
Refresh row cycle time		t_{RFC}	72		75		75		ns	
Row active time		t_{RAS}	42	70K	45	120K	45	120K	ns	
/RAS to /CAS delay		t_{RCD}	18		20		20		ns	
Row precharge time		t_{RP}	18		20		20		ns	
Row active to Row active delay		t_{RRD}	12		15		15		ns	
Write recovery time		t_{WR}	15		15		5		t_{CK}	
Last data in to Read command		t_{CDLR}	1		1		1		t_{CK}	
Col. address to Col. address delay		t_{CCD}	1		1		1		t_{CK}	
Clock cycle time	CL=2.0	t_{CK}	7.5	12	7.5	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12	ns	5
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
DQS-out access time from CK/CK*		t_{DQSCK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK*		t_{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to ouput data edge		t_{DQSQ}	-	0.45	-	0.5	-	0.5	ns	5
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
CK to valid DQS-in		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS-in setup time		t_{WPRES}	0		0		0		ns	2
DQS-in hold time		t_{WPREH}	0.25		0.25		0.25		t_{CK}	
DQS-in falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}	
DQS-in falling edge to CK rising hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}	
DQS-in high level width		t_{DQSH}	0.35		0.35		0.35		t_{CK}	
DQS-in low level width		t_{DQSL}	0.35		0.35		0.35		t_{CK}	
DQS-in cycle time		t_{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
Address and Control Input setup time(fast)		t_{IS}	0.75		0.9		0.9		ns	6
Address and Control Input hold time(fast)		t_{IH}	075		0.9		0.9		ns	6
Address and Control Input hold time(slow)		t_{IS}	0.8		10		1.0		ns	6
Address and Control Input hold time(slow)		t_{IH}	0.8		1.0		1.0		ns	6
Data-out high impedance time from CK/CK*		t_{HZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data-out low impedance time from CK/CK*		t_{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Input Slew Rate(for input only pins)		$t_{SL(I)}$	0.5		0.5		0.5		V/ns	6

Input Slew Rate(for I/O pins)	$t_{SL(IO)}$	0.5		0.5		0.5		V/ns	7
Output Slew Rate (x4, x8)	$t_{SL(O)}$	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)	t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		
Mode register set cycle time	t_{MRD}	12		15		15		ns	
DQ & DM setup time to DQS	t_{DS}	0.45		0.5		0.5		ns	7,8,9
DQ & DM hold time to DQS	t_{DH}	0.45		0.5		0.5		ns	7,8,9
DQ & DM input pulse width	t_{DIPW}	1.75		1.75		1.75		ns	
Power down exit time	t_{PDEX}	6		7.5		7.5		ns	
Control & Address input pulse width	t_{IPW}	2.2		2.2		2.2		ns	
Exit self refresh to bank active command	t_{XSA}	80		75		75		ns	
Exit self refresh to non-read command	t_{XSNR}	75		75		75		ns	4
Exit self refresh to read command	t_{XSRD}	200		200		200		t_{CK}	
Refresh interval time	T_{REFI}	7.8		7.8		7.8		us	1
Output DQS valid window	T_{QH}	tHPmin -tQHS		tHPmin -tQHS		tHPmin -tQHS		ns	5
Clock half period	T_{HP}	tCLmin or tCHS		tCLmin or tCHS		tCLmin or tCHS		ns	
Data hold skew factor	T_{QHS}		0.55		0.75		0.75	ns	
DQS write postamble time	T_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	3
Active to Read with Auto precharge command	T_{RAP}	20		20		20			
Autoprecharge write recovery + Precharge time	T_{DAL}	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		1CK	11

Notes :

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previou s write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade acc ordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are ¡Ã45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	.tIS	.tIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t IS /t IH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating.

Input Setup/Hold Slew Rate	.tDS	.tDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t DS /t DH in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating.

I/O Input Level	.tDS	.tDH
(mV)	(ps)	(ps)
±280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ±310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating.

Delta Rise/Fall Rate	.tDS	.tDH
(V/ns)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

SIMPLIFIED COMMAND TRUTH TABLE

(V=VALID, X=DON ¡ÇT CARE, H=LOGIC HIGH, L=LOGIC LOW)

COMMAND			CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DM	BA 0,1	A10/AP	A11 A9~A0	NOTE
Register	Extended MRS		H	X	L	L	L	L	X	OP code			1,2
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~A9)	4
	Auto precharge eable										H		4
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		5
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DM			H	X					V	X			8
No operation command			H	X	H	X	X	X	X	X			9
					L	H	H	H					9

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

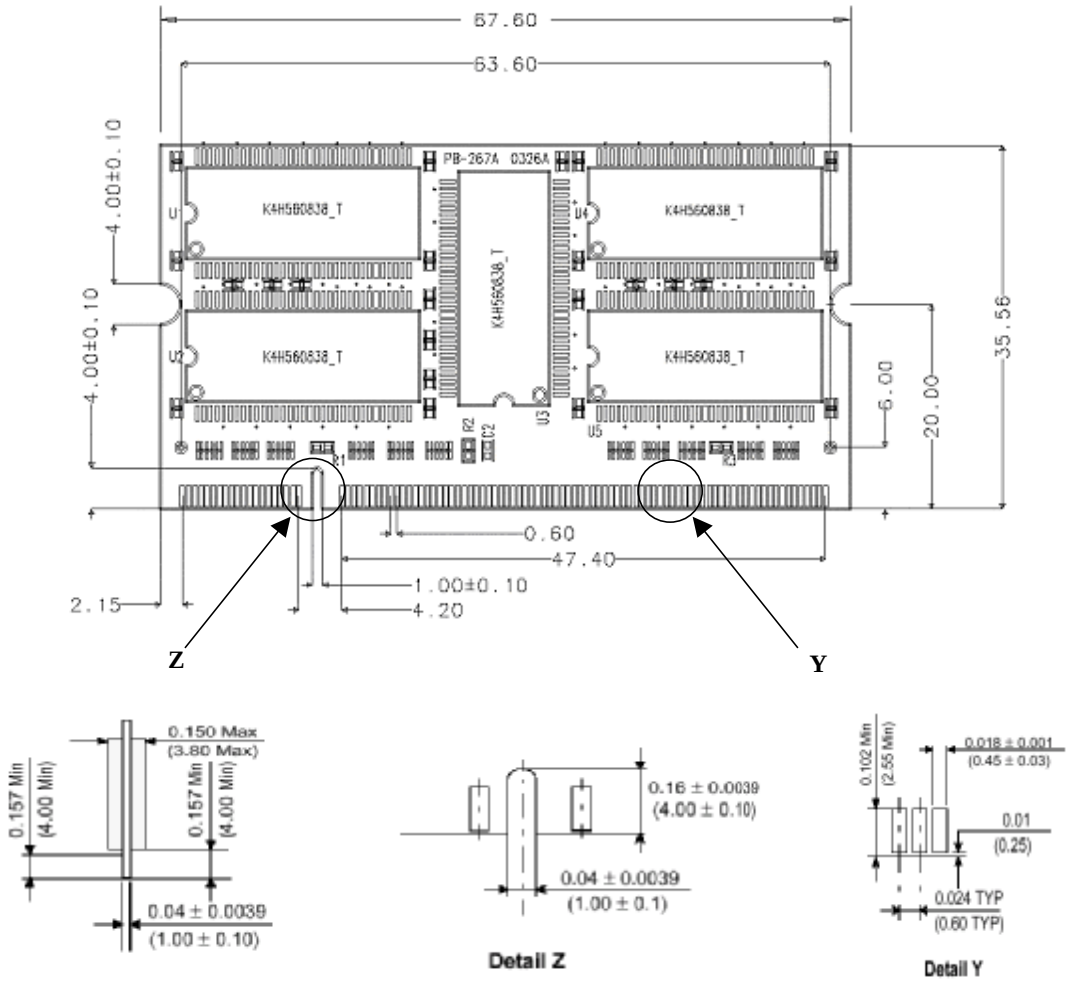
Notes :

1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected..
6. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges
   (Write DM latency is 0)
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

PACKAGING INFORMATION

Unit : mm

Front –Side



PCB 두께 : 1.0 ±0.1mm

ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HDD32M72B9-16B	256MByte	32M x 72	200PIN SO-DIMM	8K	2.5V	DDR	166MHz/CL2.5
HDD32M72B9-13A	256MByte	32M x 72	200PIN SO-DIMM	8K	2.5V	DDR	133MHz/CL2
HDD32M72B9-13B	256MByte	32M x 72	200PIN SO-DIMM	8K	2.5V	DDR	133MHz/CL2.5