PRELIMINARY

AMD

Am29LV004

4 Megabit (512 K x 8-Bit)
CMOS 3.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **High performance**
  - — Full voltage range: access times as fast as 100 ns
  - — Regulated voltage range: access times as fast as 90 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 10 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Typical 1,000,000 write cycles per sector (100,000 cycles minimum guaranteed)**
- **Package option**
  - — 40-pin TSOP
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

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GENERAL DESCRIPTION

The Am29LV004 is an 4 Mbit, 3.0 volt-only Flash memory organized as 524,288 bytes. The device is offered in a 40-pin TSOP package. The byte-wide (x8) data appears on DQ7–DQ0. This device requires only a single, 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

The standard device offers access times of 90, 100, 120, and 150 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

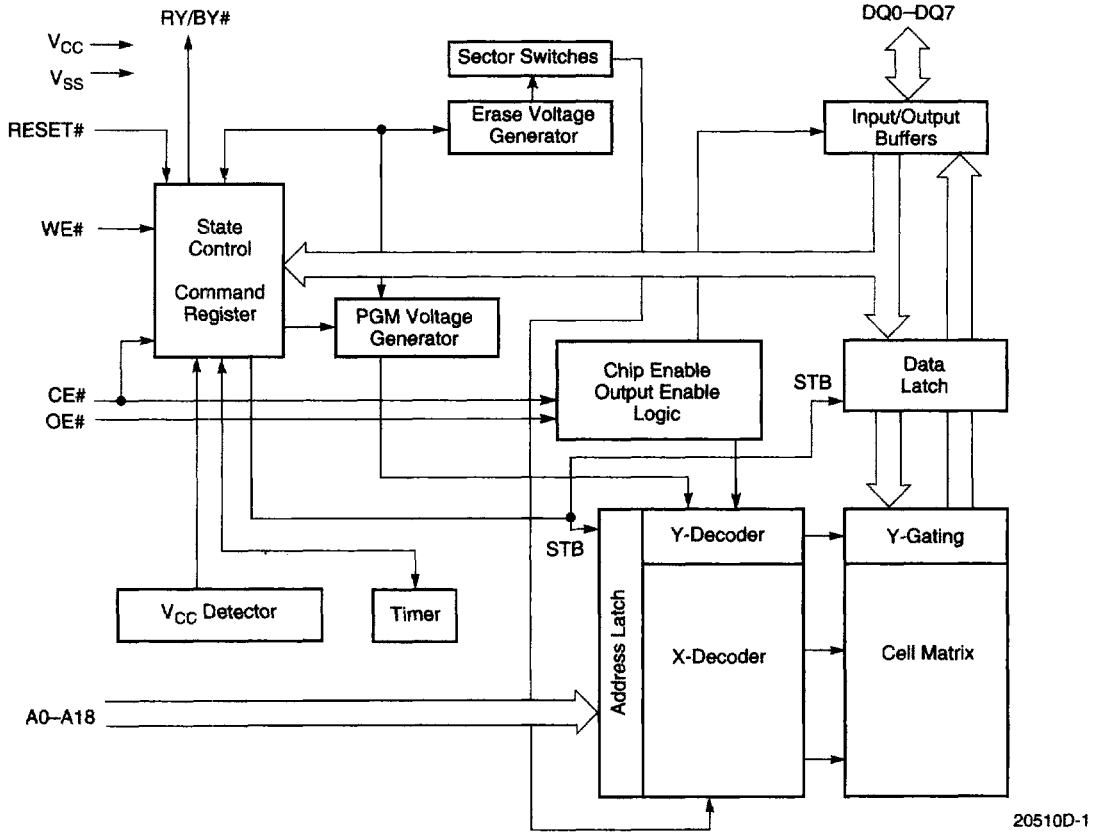
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

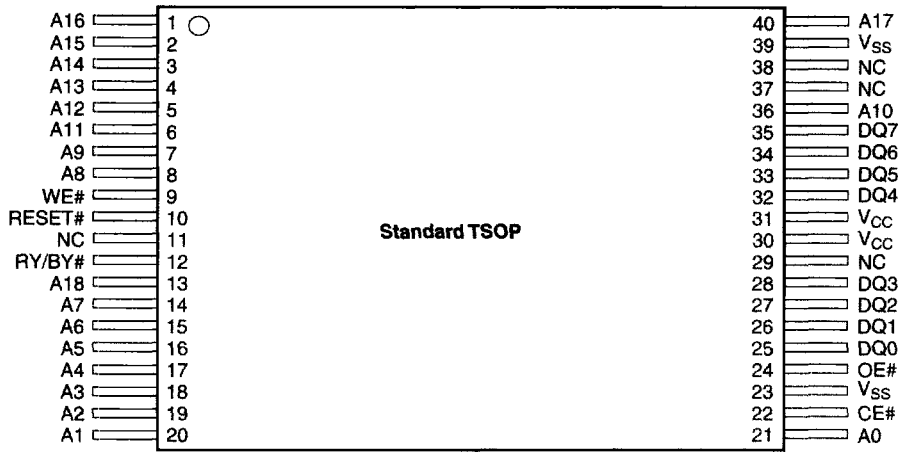
Family Part Number		Am29LV004			
Speed Options	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**-90R**			
	Full Voltage Range: V_{CC} = 2.7–3.6 V		**-100**	**-120**	**-150**
Max access time, ns (t_{ACC})		90	100	120	150
Max CE# access time, ns (t_{CE})		90	100	120	150
Max OE# access time, ns (t_{OE})		40	40	40	55

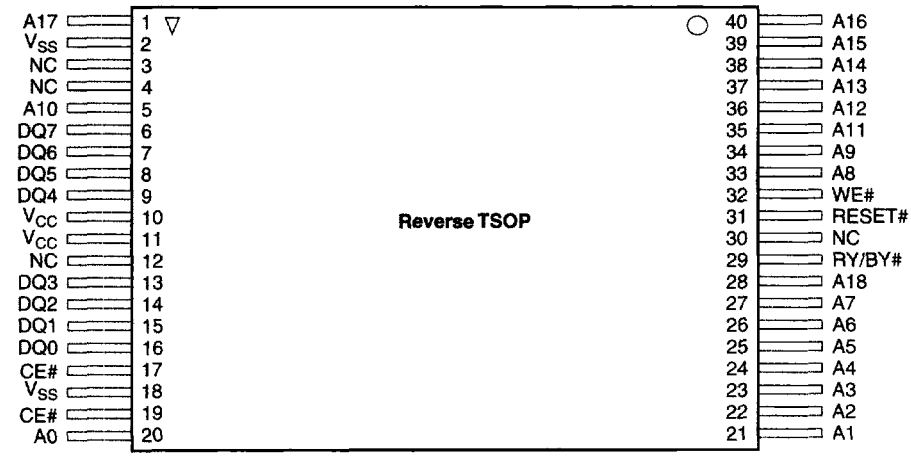
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



CONNECTION DIAGRAMS





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PIN CONFIGURATION

A0–A18 = 19 addresses

DQ0–DQ7 = 8 data inputs/outputs

CE# = Chip enable

OE# = Output enable

WE# = Write enable

RESET# = Hardware reset pin, active low

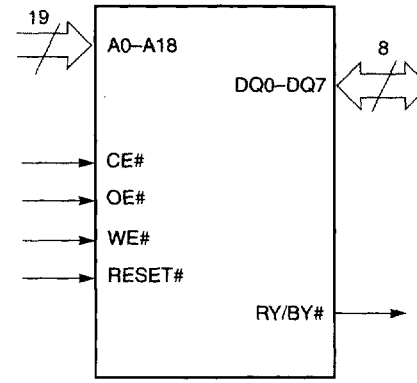
RY/BY# = Ready/Busy# output

V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{SS} = Device ground

NC = Pin not connected internally

LOGIC SYMBOL



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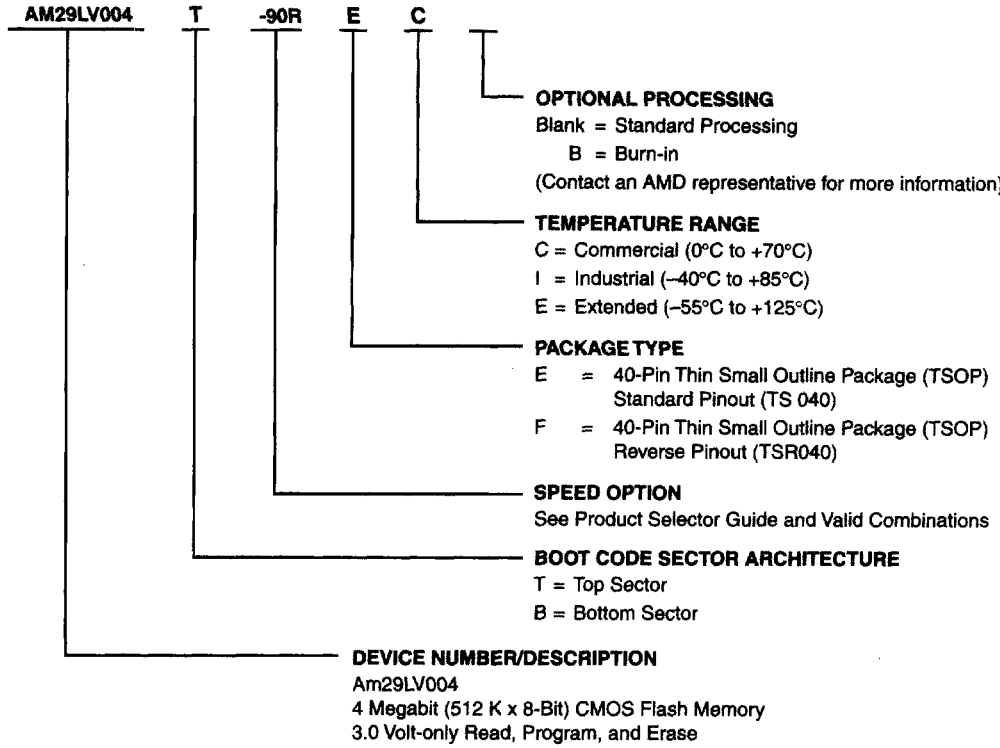
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
AM29LV004T-70R, AM29LV004B-70R	EC, EI, FC, FI
AM29LV004T-80, AM29LV004B-80	EC, EI, EE, FC, FI, FE
AM29LV004T-90, AM29LV004B-90	
AM29LV004T-120, AM29LV004B-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

Table 1. Am29LV004 Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	Addresses (Note)	DQ0–DQ7
Read	L	L	H	H	A_{IN}	D_{OUT}
Write	L	H	L	H	A_{IN}	D_{IN}
Standby	$V_{CC} \pm 0.3$ V	X	X	$V_{CC} \pm 0.3$ V	X	High-Z
Output Disable	L	H	H	H	X	High-Z
Reset	X	X	X	L	X	High-Z
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Note: *Addresses are A18–A0.*

Table 2. Am29LV004T Top Boot Block Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range (in hexadecimal)
SA0	0	0	0	X	X	X	64	00000h-0FFFFh
SA1	0	0	1	X	X	X	64	10000h-1FFFFh
SA2	0	1	0	X	X	X	64	20000h-2FFFFh
SA3	0	1	1	X	X	X	64	30000h-3FFFFh
SA4	1	0	0	X	X	X	64	40000h-4FFFFh
SA5	1	0	1	X	X	X	64	50000h-5FFFFh
SA6	1	1	0	X	X	X	64	60000h-6FFFFh
SA7	1	1	1	0	X	X	32	70000h-77FFFh
SA8	1	1	1	1	0	0	8	78000h-79FFFh
SA9	1	1	1	1	0	1	8	7A000h-7BFFFh
SA10	1	1	1	1	1	X	16	7C000h-7FFFFh

Table 3. Am29LV004B Bottom Boot Block Sector Address Table

Sector	A18	A17	A16	A15	A14	A13	Sector Size (Kbytes)	Address Range (in hexadecimal)
SA0	0	0	0	0	0	X	16	00000h-03FFFh
SA1	0	0	0	0	1	0	8	04000h-05FFFh
SA2	0	0	0	0	1	1	8	06000h-07FFFh
SA3	0	0	0	1	X	X	32	08000h-0FFFFh
SA4	0	0	1	X	X	X	64	10000h-1FFFFh
SA5	0	1	0	X	X	X	64	20000h-2FFFFh
SA6	0	1	1	X	X	X	64	30000h-3FFFFh
SA7	1	0	0	X	X	X	64	40000h-4FFFFh
SA8	1	0	1	X	X	X	64	50000h-5FFFFh
SA9	1	1	0	X	X	X	64	60000h-6FFFFh
SA10	1	1	1	X	X	X	64	70000h-7FFFFh

Table 4. Am29LV004 Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A18 to A13	A12 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD	L	L	H	X	X	V_{ID}	X	L	X	L	L	01h
Device ID: Am29LV004T (Top Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	B5h
Device ID: Am29LV004B (Bottom Boot Block)	L	L	H	X	X	V_{ID}	X	L	X	L	H	B6h
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	01h (protected) 00h (unprotected)

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

COMMAND DEFINITIONS

Table 5. Am29LV004 Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 2-4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Auto-select (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID, Top Boot Block	4	555	AA	2AA	55	555	90	X01	B5				
	Device ID, Bottom Boot Block	4	555	AA	2AA	55	555	90	X01	B6				
	Sector Protect Verify (Note 8)	4	555	AA	2AA	55	555	90	(SA) X02	00				
										01				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (Note 9)		1	XXX	B0										
Erase Resume (Note 10)		1	XXX	30										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A18–A13 uniquely select any sector.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except when reading array or autoselect data, all commandbus cycles are write operations.*
4. *Address bits A18–A11 are don't cares for unlock and command cycles.*
5. *No unlock or command cycles required when reading array data.*
6. *The Reset command is required to return to reading array data when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status data).*
7. *The fourth cycle of the autoselect command sequence is a read cycle.*
8. *The data is 00h for an unprotected sector and 01h for a protected sector. See "Autoselect Command Sequence" for more information.*
9. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
10. *The Erase Resume command is valid only during the Erase Suspend mode.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied. . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC} (Note 1) . . . . . –0.5 V to +4.0 V

A9, OE#,
and RESET# (Note 2). . . . . –0.5 V to +12.5 V

All other pins
(Note 1). . . . . –0.5 V to V_{CC}+0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 2.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is –0.5 V. During voltage transitions, A9, OE#, and RESET# may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 1. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A). . . . . –55°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . . 3.0 V to 3.6 V

V_{CC} for full voltage range . . . . . 2.7 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

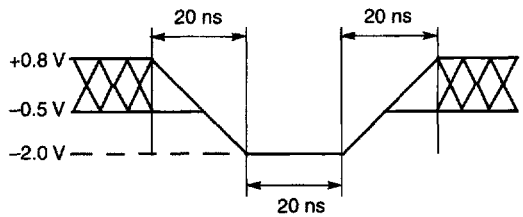


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Figure 1. Maximum Negative Overshoot Waveform

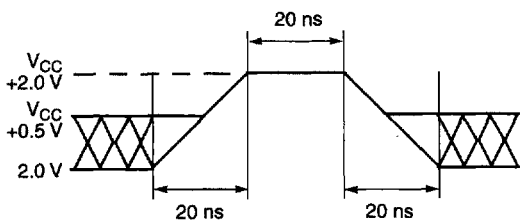

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Figure 2. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS

CMOS Compatible

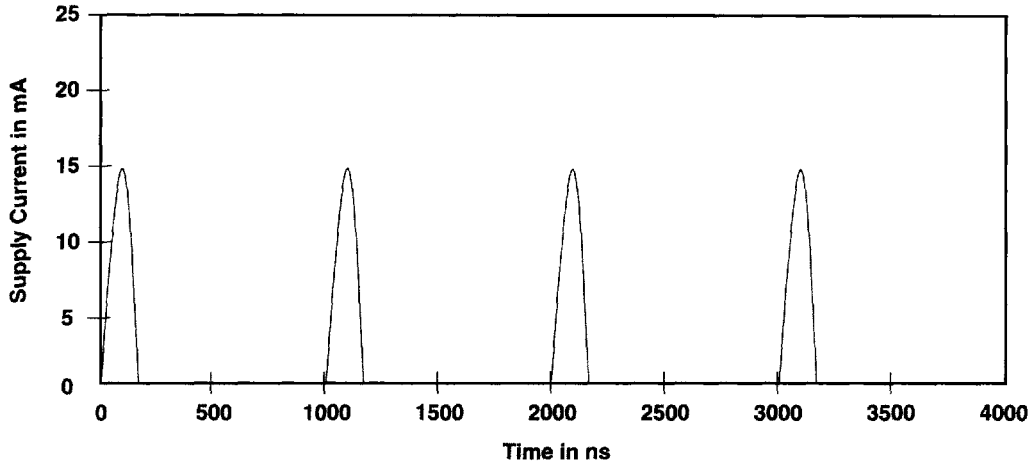
Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IH}	5 MHz		10	16	mA
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Notes 2 and 4)	CE# = V_{IL}, OE# = V_{IH}			20	30	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC\ max}$; CE#, RESET# = V_{CC}±0.3 V			0.2	5	µA
I_{CC4}	V_{CC} Reset Current	$V_{CC} = V_{CC\ max}$; RESET# = V_{SS} ± 0.3 V			0.2	5	µA
I_{CC5}	Automatic Sleep Mode (Note 3)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V			0.2	5	µA
V_{IL}	Input Low Voltage			–0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} + 0.3	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 3.3 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}. Typical V_{CC} is 3.0 V.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.*
4. *Not 100% tested.*

DC CHARACTERISTICS (Continued)

Zero Power Flash



Note: *Addresses are switching at 1 MHz*

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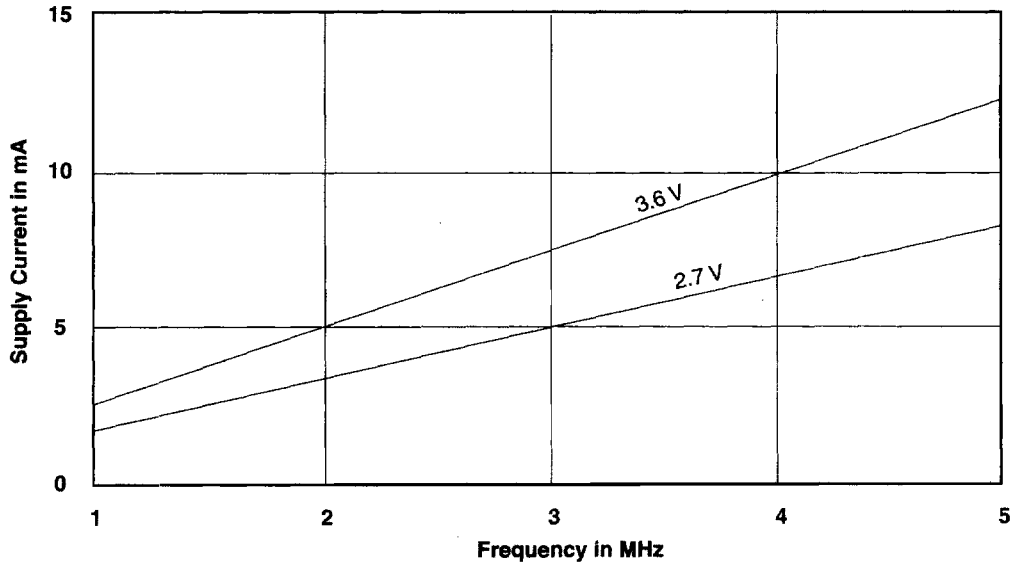
Figure 3. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

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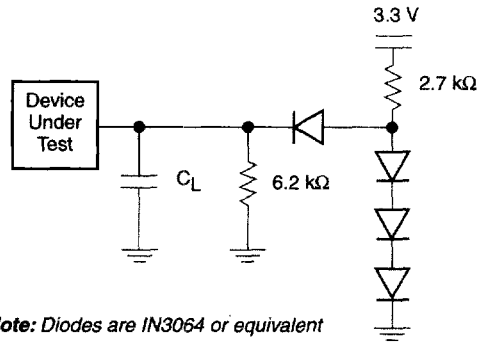
Figure 4. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

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Figure 5. Test Setup

Table 6. Test Specifications

Test Condition	-90R, -100	-120, -150	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0–3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

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Figure 6. Input Waveforms and Measurement Levels

AC CHARACTERISTICS
Read Operations

Parameter		Description		Test Setup		Speed Option				Unit
JEDEC	Std					-90R	-100	-120	-150	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	100	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		$CE\# = V_{IL}$ $OE\# = V_{IL}$	Max	90	100	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		$OE\# = V_{IL}$	Max	90	100	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	40	40	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	30	30	30	40	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	30	30	30	40	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0				ns
			Toggle and Data# Polling		Min	10				ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0				ns

Notes:
1. *Not 100% tested.*
2. *See Figure 5 and Table 6 for test specifications.*

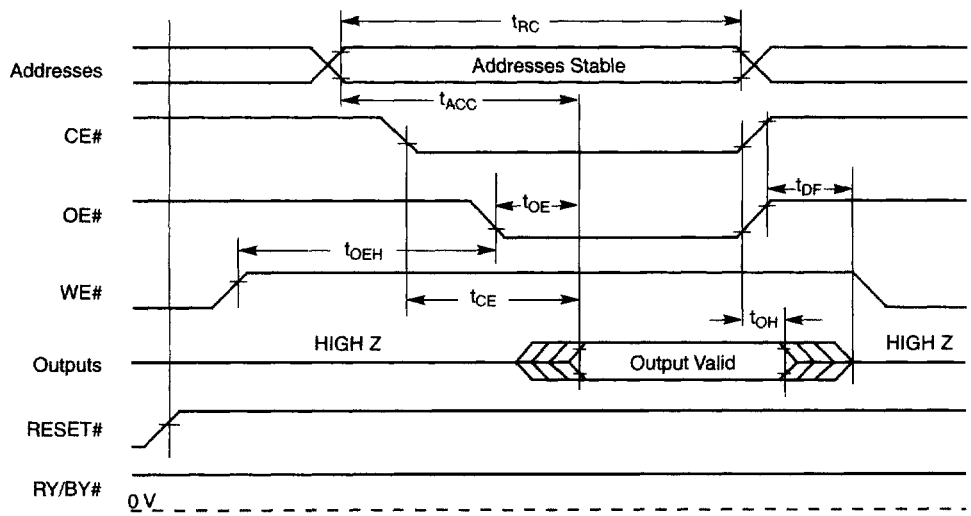

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Figure 7. Read Operations Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns

Note: *Not 100% tested.*

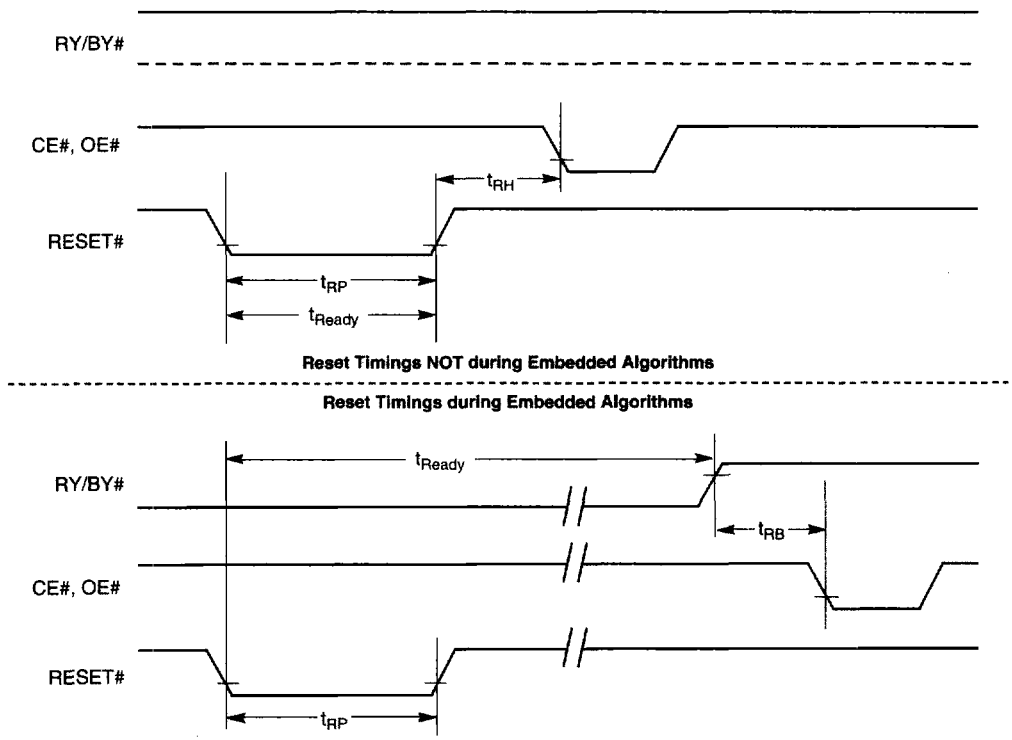


Figure 8. RESET# Timings

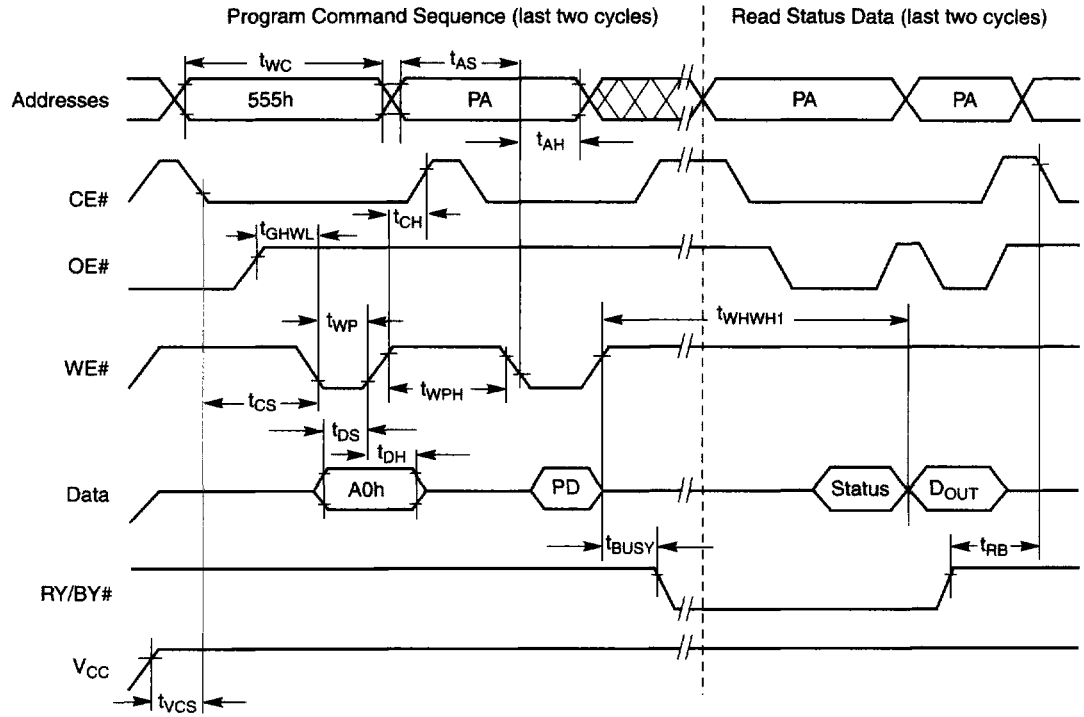
AC CHARACTERISTICS
Erase/Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			-90R	-100	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0				ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	50	50	50	65	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	50	50	50	65	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0				ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0				ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	50	50	50	65	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Notes 1, 2)	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2)	Typ					sec
	t_{VCS}	V_{CC} Setup Time	Min	50				µs
	t_{RB}	Recovery Time from RY/BY#	Min	0				ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90				ns

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS

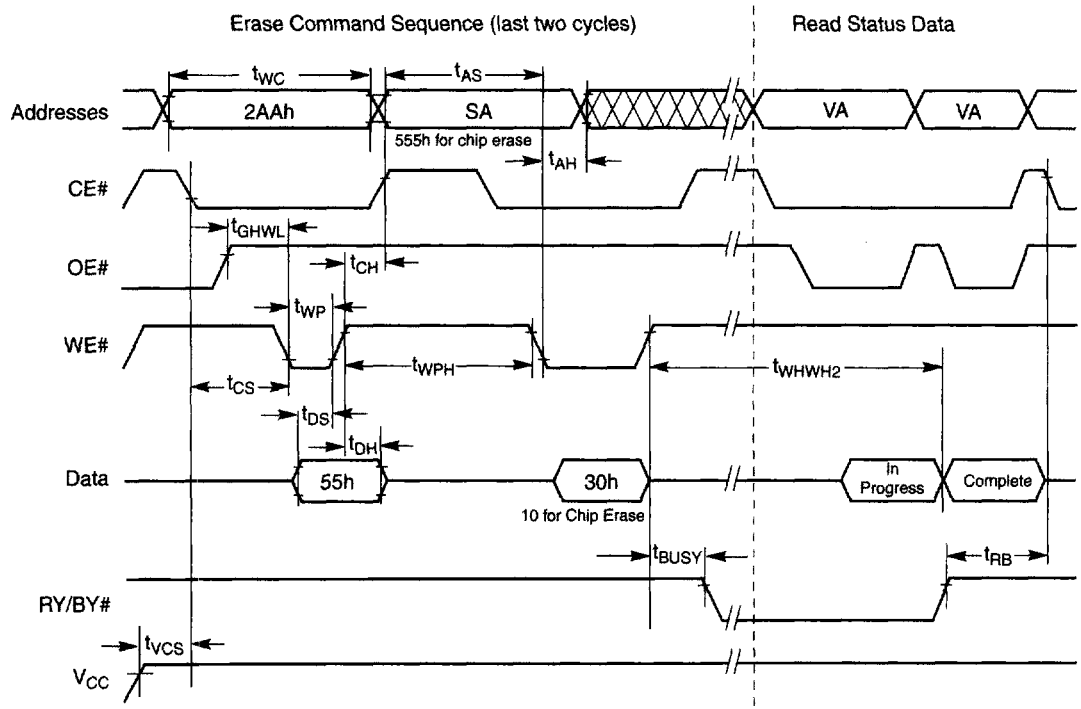


Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

20510D-12

Figure 9. Program Operation Timings

AC CHARACTERISTICS

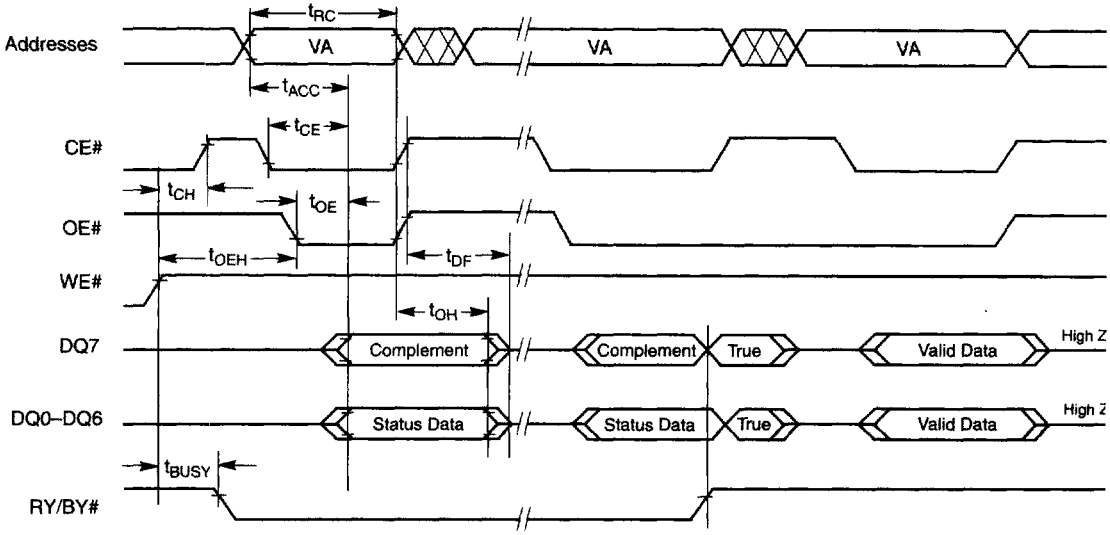


Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").*

20510D-13

Figure 10. Chip/Sector Erase Operation Timings

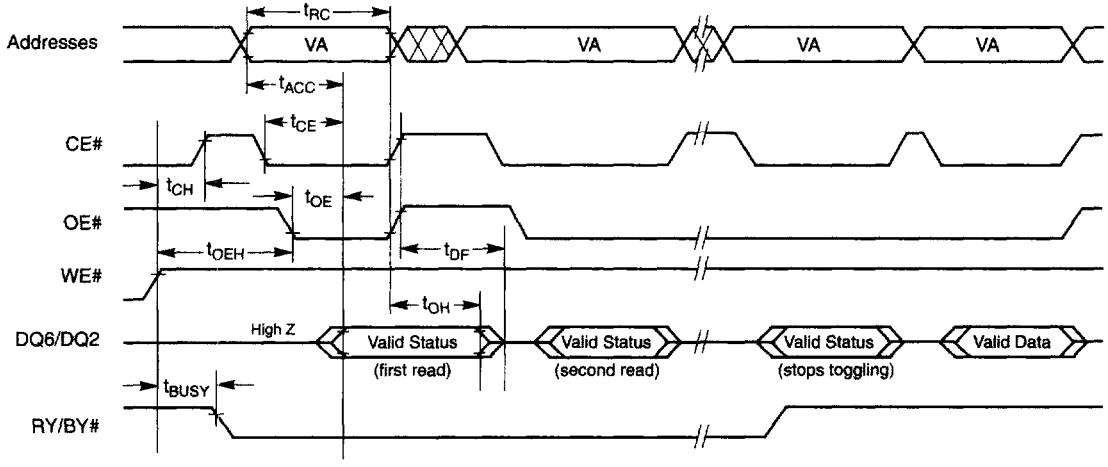
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

20510D-14

Figure 11. Data# Polling Timings (During Embedded Algorithms)

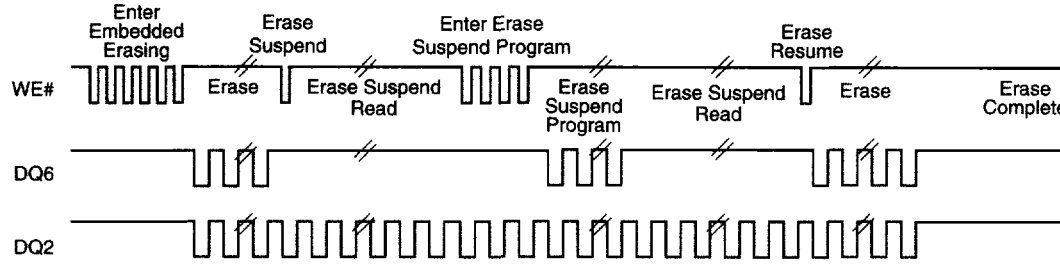


Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

20510D-15

Figure 12. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



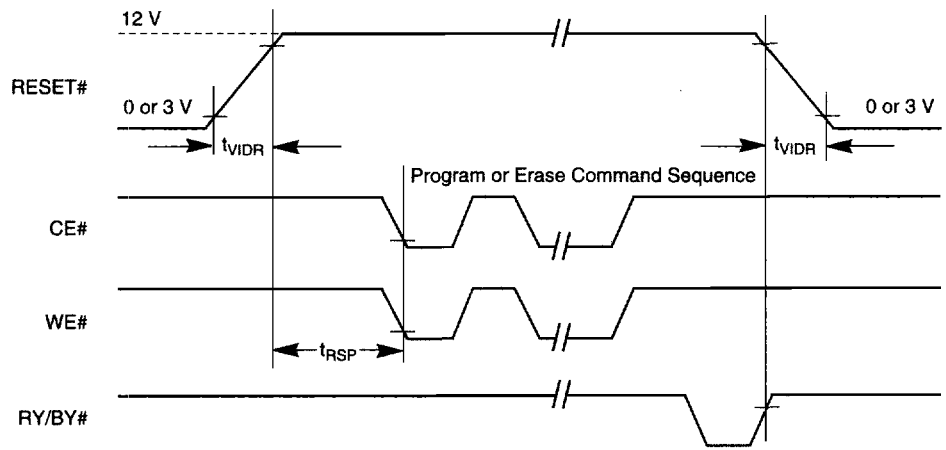
Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

20510D-16

Figure 13. DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs



20510D-17

Figure 14. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS

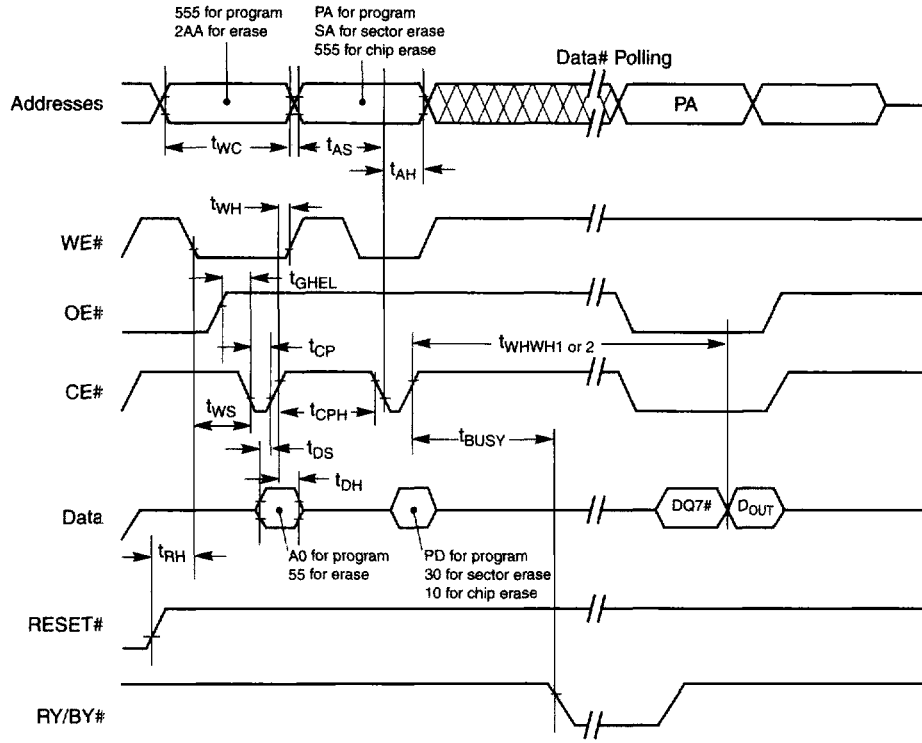
Alternate CE# Controlled Erase/Program Operations

Parameter		Description		Speed Options				Unit
JEDEC	Std			-90R	-100	-120	-150	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	90	100	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0				ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	50	50	50	65	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	50	50	50	65	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0				ns
	t_{OES}	Output Enable Setup Time	Min	0				ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0				ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0				ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0				ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	50	50	50	65	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30	30	30	35	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Notes 1, 2)	Typ	9				µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Notes 1, 2)	Typ					sec

Notes:

1. *Not 100% tested.*
2. *See the "Erase And Programming Performance" section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = Program Address, PD = Program Data, DQ7# = complement of the data written to the device, D_{OUT} is the data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

20510D-18

Figure 15. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	1	15	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	11		s	
Byte Programming Time	9	300	µs	Excludes system level overhead (Note 5)
Chip Programming Time (Note 3)	4.5	13.5	s	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the four-bus-cycle sequence for the program command. See Table 5 for further information on command definitions.*
6. *The device has a typical erase and program cycle endurance of 1,000,000 cycles. 100,000 cycles are guaranteed.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

REVISION SUMMARY

Global

Revised formatting to be consistent with other current 3.0 volt-only data sheets.