

1.5V Drive Pch+Pch MOSFET

TT8J21

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low On-resistance.
- 2) High Power Package.
- 3) Low voltage drive. (1.5 V)

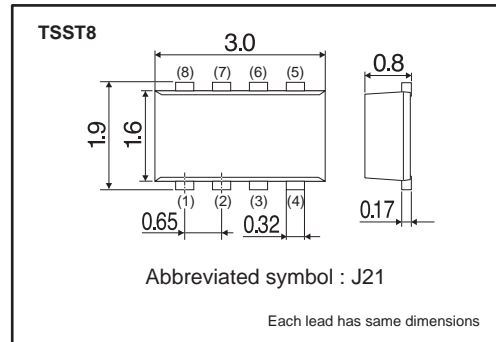
●Applications

Switching

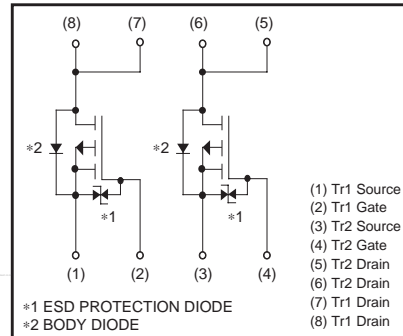
●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
TT8J21		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 10	V
Drain current	Continuous	I_D	± 2.5 A
	Pulsed	I_{DP} *1	± 10 A
Source current (Body diode)	Continuous	I_S	-0.8 A
	Pulsed	I_{SP} *1	-10 A
Total power dissipation	P_D *2	1.25	W / TOTAL
		1.0	W / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of Storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Mounted on a ceramic board

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}$ *	100	°C / W / TOTAL
		125	°C / W / ELEMENT

* Mounted on a ceramic board

●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-20	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS}=-20V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS}=-10V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	49	68	m Ω	$I_D=-2.5A, V_{GS}=-4.5V$
		-	68	95	m Ω	$I_D=-1.2A, V_{GS}=-2.5V$
		-	100	150	m Ω	$I_D=-1.2A, V_{GS}=-1.8V$
		-	140	280	m Ω	$I_D=-0.5A, V_{GS}=-1.5V$
Forward transfer admittance	$ Y_{fs} $ *	2.5	-	-	S	$V_{DS}=-10V, I_D=-2.5A$
Input capacitance	C_{iss}	-	1270	-	pF	$V_{DS}=-10V$
Output capacitance	C_{oss}	-	100	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	90	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	9	-	ns	$V_{DD}\approx -10V$
Rise time	t_r *	-	30	-	ns	$V_{GS}=-4.5V$ $I_D=-1.2A$
Turn-off delay time	$t_{d(off)}$ *	-	120	-	ns	$R_L\approx 8.3\Omega$
Fall time	t_f *	-	85	-	ns	$R_G=10\Omega$
Total gate charge	Q_g *	-	12	-	nC	$V_{DD}\approx -10V$ $V_{GS}=-4.5V$
Gate-source charge	Q_{gs} *	-	2.5	-	nC	$I_D=-2.5A$
Gate-drain charge	Q_{gd} *	-	2.0	-	nC	$R_L\approx 4\Omega / R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	-	-	-1.2	V	$I_S=-2.5A, V_{GS}=0V$

* Pulsed

●Electrical characteristic curves

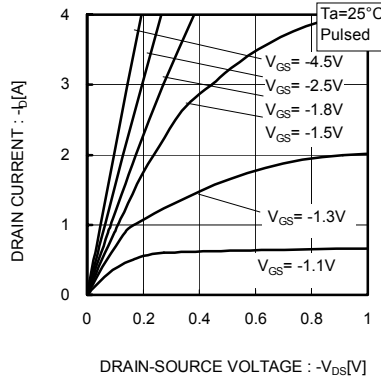


Fig.1 Typical Output Characteristics (I)

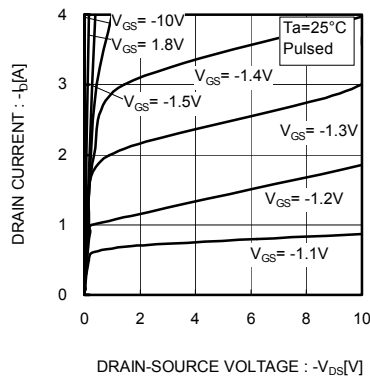


Fig.2 Typical Output Characteristics (II)

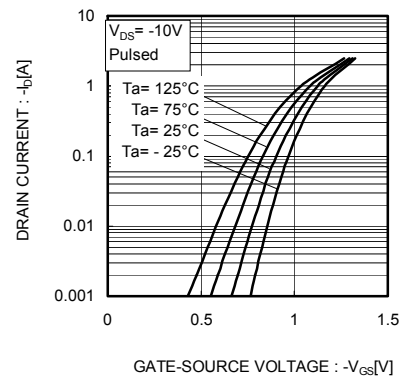


Fig.3 Typical Transfer Characteristics

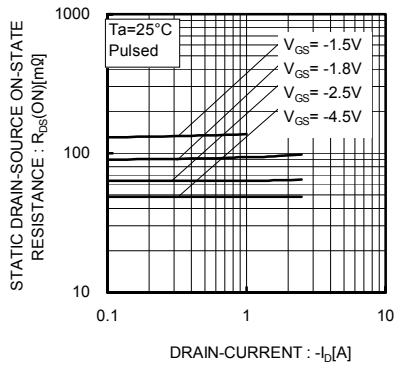


Fig.4 Static Drain-Source On-State Resistance vs. Drain

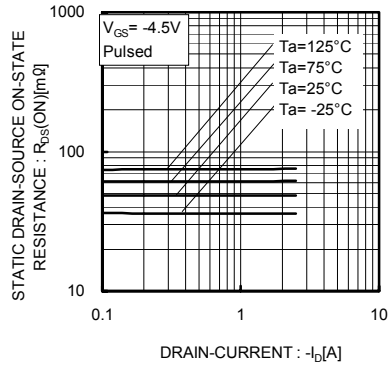


Fig.5 Static Drain-Source On-State Resistance vs. Drain

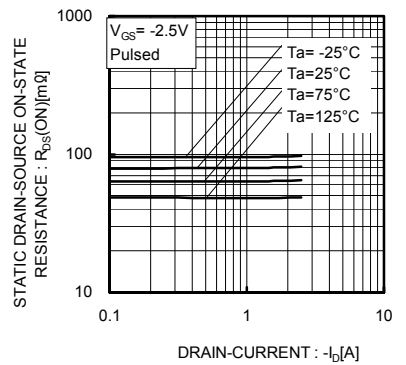


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

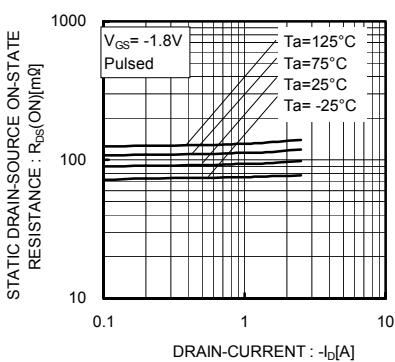


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

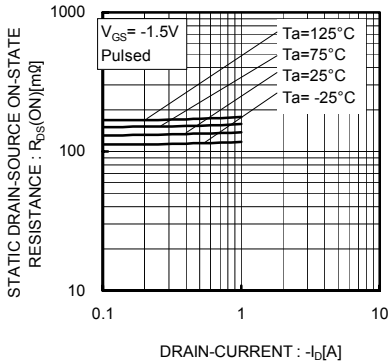


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

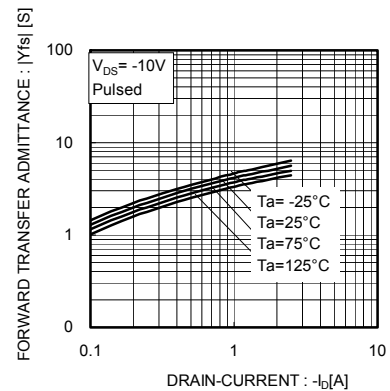
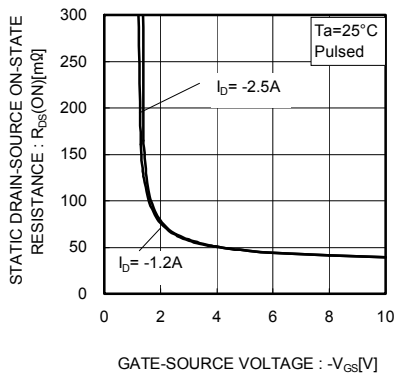
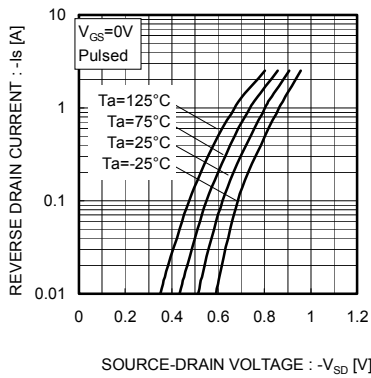


Fig.9 Forward Transfer Admittance vs. Drain Current



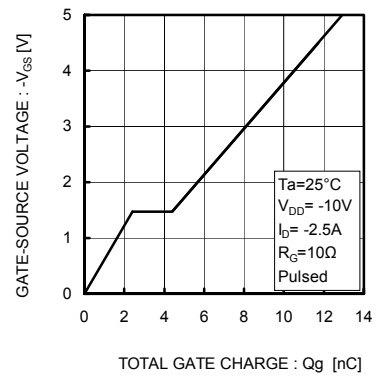
GATE-SOURCE VOLTAGE : $-V_{GS}[V]$

Fig.10 Static Drain-Source On-State Resistance vs. Gate Source Voltage



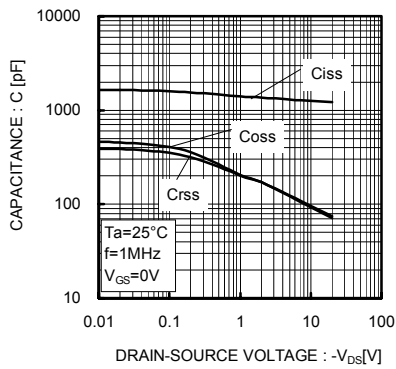
SOURCE-DRAIN VOLTAGE : $-V_{SD}[V]$

Fig.11 Reverse Drain Current vs. Source-Drain Voltage



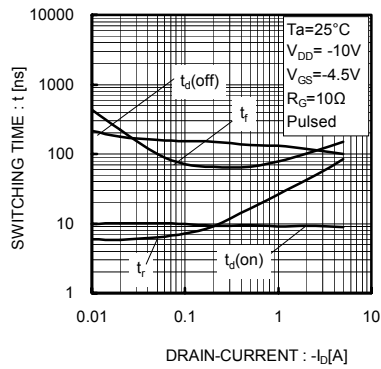
TOTAL GATE CHARGE : $Q_g[nC]$

Fig.12 Dynamic Input Characteristics



DRAIN-SOURCE VOLTAGE : $-V_{DS}[V]$

Fig.13 Typical Capacitance vs. Drain-Source



DRAIN-CURRENT : $-I_D[A]$

Fig.14 Switching Characteristics

●Measurement circuits

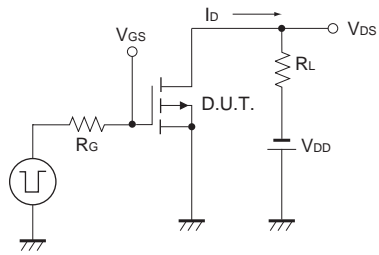


Fig.1-1 Switching Time Measurement Circuit

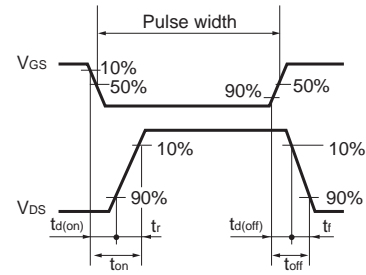


Fig.1-2 Switching Waveforms

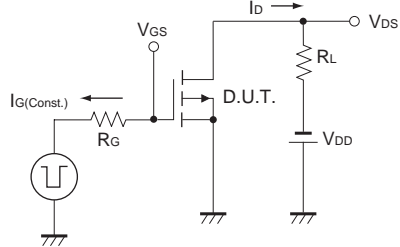


Fig.2-1 Gate Charge Measurement Circuit

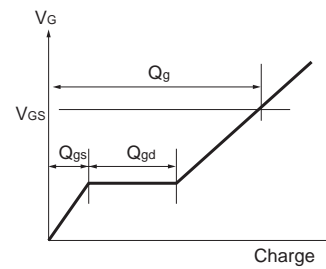


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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