

FEATURES

- 400 MWPS Nominal Conversion Rate
- RS-323-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- 50 and 75 Ohm Output Drive

APPLICATIONS

- Raster Graphics
- High Resolution Color or Monochrome Displays to 2k x 2k Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

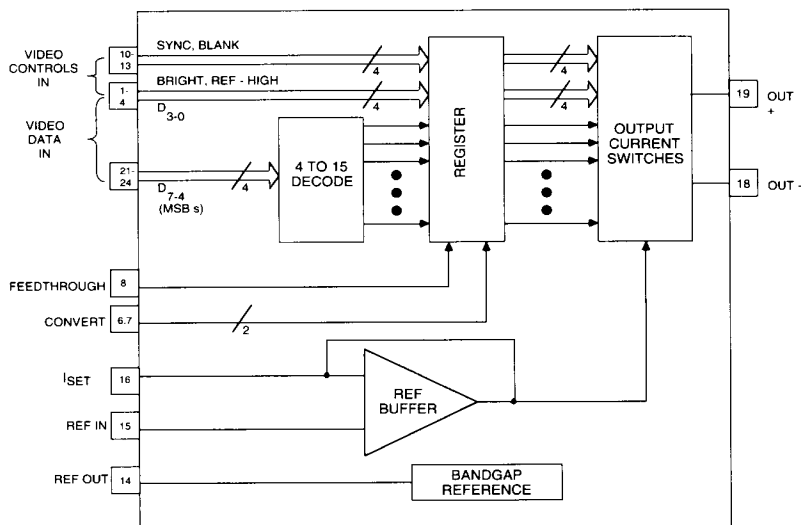
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GENERAL DESCRIPTION

The HDAC51400 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 400 MWPS. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC51400 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video

levels. Standard set-up level is 7.5 IRE. The HDAC51400 includes an internal precision bandgap reference which can drive two other HDAC51400s in an RGB graphics system. The HDAC51400 contains data and control input registers, video control logic, reference buffer, and current switches in a 24 Lead Cerdip package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)¹**Supply Voltages**

V_{EED} (measured to V_{CCD})	-7.0 to 0.5 V
V_{EEA} (measured to V_{CCA})	-7.0 to 0.5 V
V_{CCA} (measured to V_{CCD})	-0.5 to 0.5 V

REF+ (measured to V_{CCA})	V_{EEA} to 0.5 V
REF- (measured to V_{CCA})	V_{EEA} to 0.5 V

Input Voltages

CONV, Data, and Controls (measured to V_{CCD})	V_{EED} to 0.5 V
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Temperature

Operating, ambient	-55 to + 125 °C
junction	+ 175 °C
Lead, Soldering (10 seconds)	+ 300 °C
Storage	-60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$V_{CCD} = V_{CCA} = \text{ground}$, $V_{EEA} = V_{EED} = -5.2 \text{ V} \pm 0.3 \text{ V}$, $T_A = T_{\text{MIN}}$ to T_{MAX} , $C_C = 0 \text{ pF}$, $I_{\text{SET}} = 1.105 \text{ mA}$

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	$1.0 \text{ mA} < I_{\text{SET}} < 1.3 \text{ mA}$	I	-0.37 -0.95		+0.37 +0.95	% Full Scale LSB
Differential Linearity Error	$1.0 \text{ mA} < I_{\text{SET}} < 1.3 \text{ mA}$	I	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		I	-6.5		+6.5	% Full Scale
Gain Error Tempco		IV		150		PPM/°C
Bandgap Tempco		IV		100		PPM/°C
Input Capacitance, I_{SET} , REF OUT		V		5		pF
Compliance Voltage, + Output		I	-1.2		1.5	V
Compliance Voltage, - Output		I	-1.2		1.5	V
Equivalent Output Resistance		I	20			k Ω
Output Capacitance		V		9		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		I			0.5	LSB
Input Voltage, Logic HIGH		I	-1.0			V
Input Voltage, Logic LOW		I			-1.5	V
Convert Voltage, Common Mode Range		I	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		I			120	μA
Input Current, Logic HIGH, Data and Controls		I		10	120	μA
Input Current, Convert		I		2	60	μA
Reference Voltage Measured to V_{CCA}		IV		-1.2		V
Reference Output Current		I	-50			μA

ELECTRICAL SPECIFICATIONS

V_GCD=V_CCA = ground, V_EEA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		I	-120		+120	μA/V
Supply Current		I		175	220	mA
DYNAMIC CHARACTERISTICS (R _L = 37.5 Ohms, C _L = 5 pF, T _A =+25 °C, I _{SET} =1.105 mA)						
Maximum Conversion Rate		IV	385	400		MWPS
Rise Time	10% to 90% G.S.	IV			900	ps
Rise Time	10% to 90% G.S. R _L = 25 Ohms	IV			600	ps
Current Settling Time, Clocked Mode	To 0.2% G.S.	IV		4		ns
Current Settling Time, Clocked Mode	To 0.2% R _L = 25 Ω	IV		3		ns
Clock to Output Delay, Clocked Mode		III			4	ns
Data and Output Delay, Transparent Mode		III			6	ns
Convert Pulse Width, LOW		IV		1.25		ns
Glitch Energy	Area = 1/2 VT	V		10		pV-s
Convert Pulse Width, HIGH		III		1.25		ns
Reference Bandwidth, -3 dB		V		1.25		MHz
Set-up Time, Data and Controls		III		1		ns
Hold Time, Data and Controls		III	0.	-200		ps
Slew Rate	20% to 80% G.S.	V		700		V/μS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

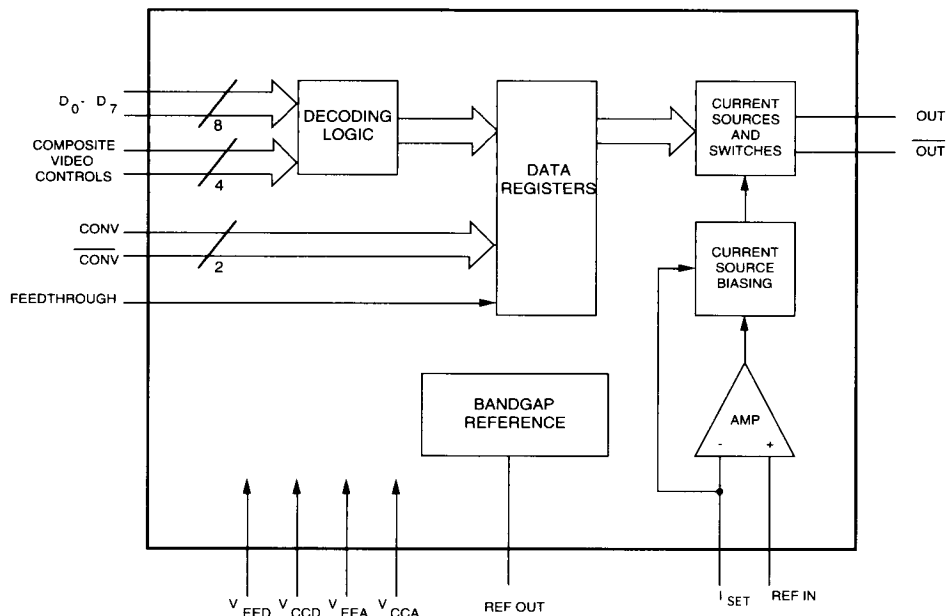
Unless otherwise noted, all tests are pulsed tests, therefore T_I = T_C = T_A.

TEST LEVEL

TEST PROCEDURE

- I100% production tested at the specified temperature.
- II100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
- IIIIQA sample tested only at the specified temperatures.
- IVParameter is guaranteed (but not tested) by design and characterization data.
- VParameter is a typical value for information purposes only.

FUNCTIONAL DIAGRAM



APPLICATION INFORMATION

The HDAC51400 is a high speed video Digital-to-Analog converter capable of up to 400 MWPS conversion rates. This makes the devices suitable for driving 2048 X 2048 pixel displays at 60 to 90 Hz update rates.

In addition, the HDAC51400 includes an internal bandgap reference which may be used to drive two other HDAC51400s if desired.

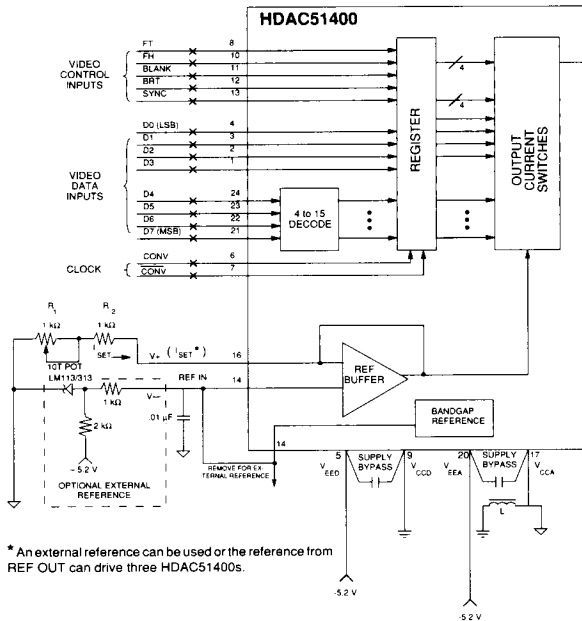
The HDAC51400 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC51400 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

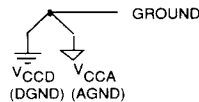
Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered VIDEO DACs.

Figure 1 - Typical Interface Circuit



NOTES:

1. $V_- = -1.2 \text{ V}$ (typical) for LM113 or V_{BG} (pin 14)
2. $V_+ = -1.2 \text{ V}$
3. $I_{SET} = \frac{V_+}{\alpha T(R_1 + R_2)}$; typ = -1.105 mA
4. $R_L = R_3 // R_4$
5. $V_{OUT} = K \left[\frac{255 - \text{DIGITAL INPUT CODE}}{255} \times I_{SET} \right] R_L + [K_1 \times I_{SET} \times R_L (\text{Bright})]$
6. $V_{SYNC} = (K \times I_{SET} \times R_L) + (K_2 \times I_{SET} \times R_L)$
7. $K = 15.8069$
 $K_1 = 1.7617$
 $K_2 = 10.0392$
8. All Reference Resistors 1/8 W 1% Metal Film Power Supply Decoupling 50 V Ceramic Disc.
9. $\frac{1}{\alpha} = \text{ECL Termination}$
10. To Power Supply



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC51400 in a color raster application is shown in Figure 1. The HDAC51400 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC51400 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC51400. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a -2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC51400 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC51400 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S .

POWER CONSIDERATIONS

The HDAC51400 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC51400 inherent supply noise rejection characteristics. As shown in Figure 1, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC51400 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD} . The analog supply return is V_{CCA} . All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC51400 has two reference inputs: REF IN and I_{SET} , and one reference output REF OUT. The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 7.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the (I_{SET}) input on the HDAC51400. A method and equations to set I_{SET} are shown in Figure 1. The HDAC51400 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF IN should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 to 1k Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased by 50% above for doubly-terminated 75 Ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The HDAC51400 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KHz and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC51400 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 2).

Figure 2 - Timing Diagram

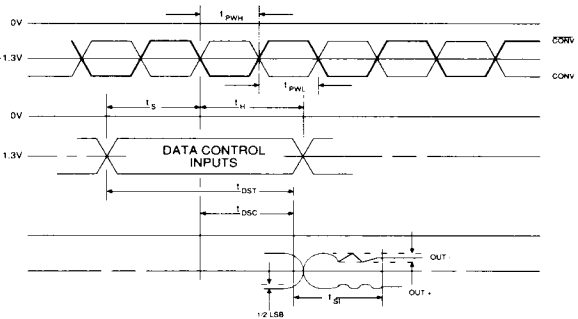


Table I - Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table I shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 8).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL drive, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC51400. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC51400 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{SET} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 4, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The OUT - output (Figure 8) will provide a video output waveform with the SYNC pulse bottom at the -1.07 V level. The OUT + is inverted with SYNC up.

Figure 3 - CONVerT, $\overline{\text{CONV}}$ Switching Levels

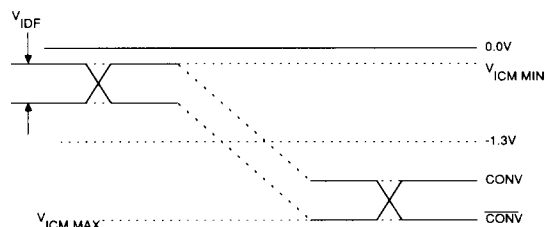


Figure 4A - Standard Load

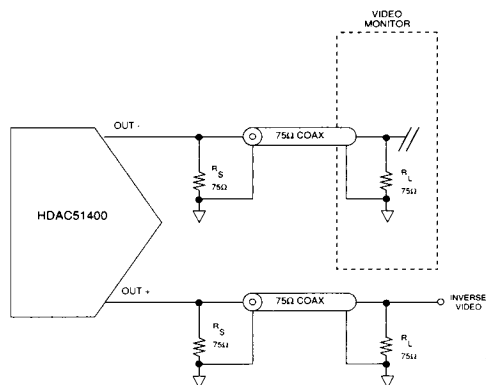
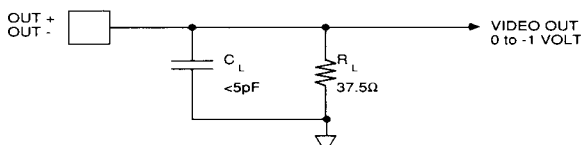


Figure 4B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC51400 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μ A to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 5 illustrate how a single HDAC51400 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC51400's reference output.

Figure 5 - Typical RGB Graphics System

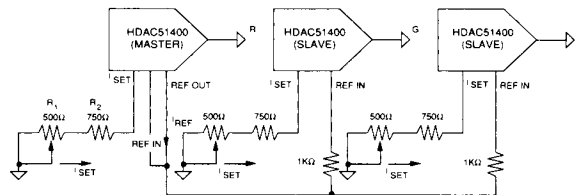


Figure 6 - Burn-In Circuit

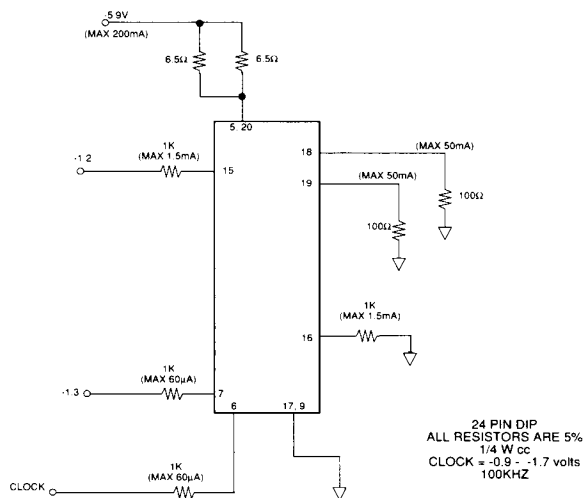


Figure 7 - DAC Output Circuit

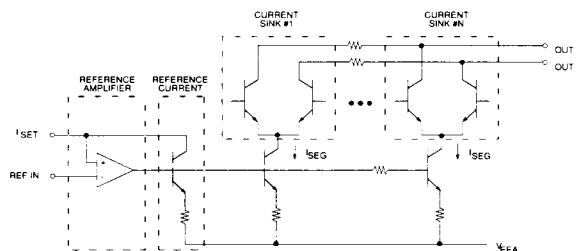


Figure 8 - Video Output Waveform for Standard Load

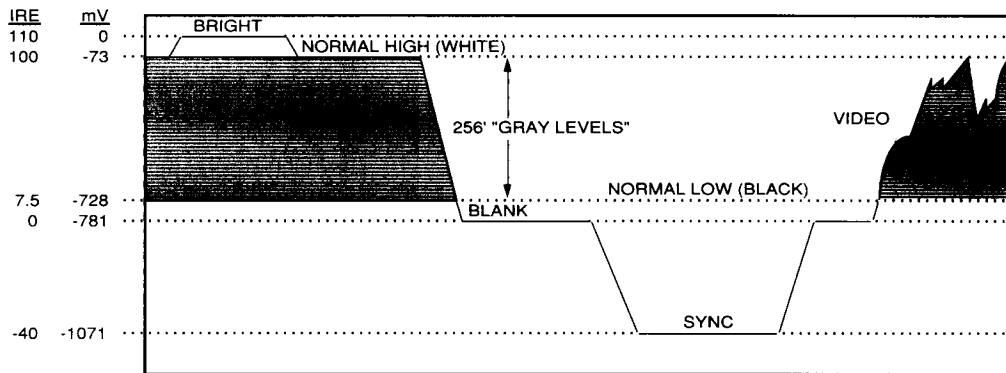
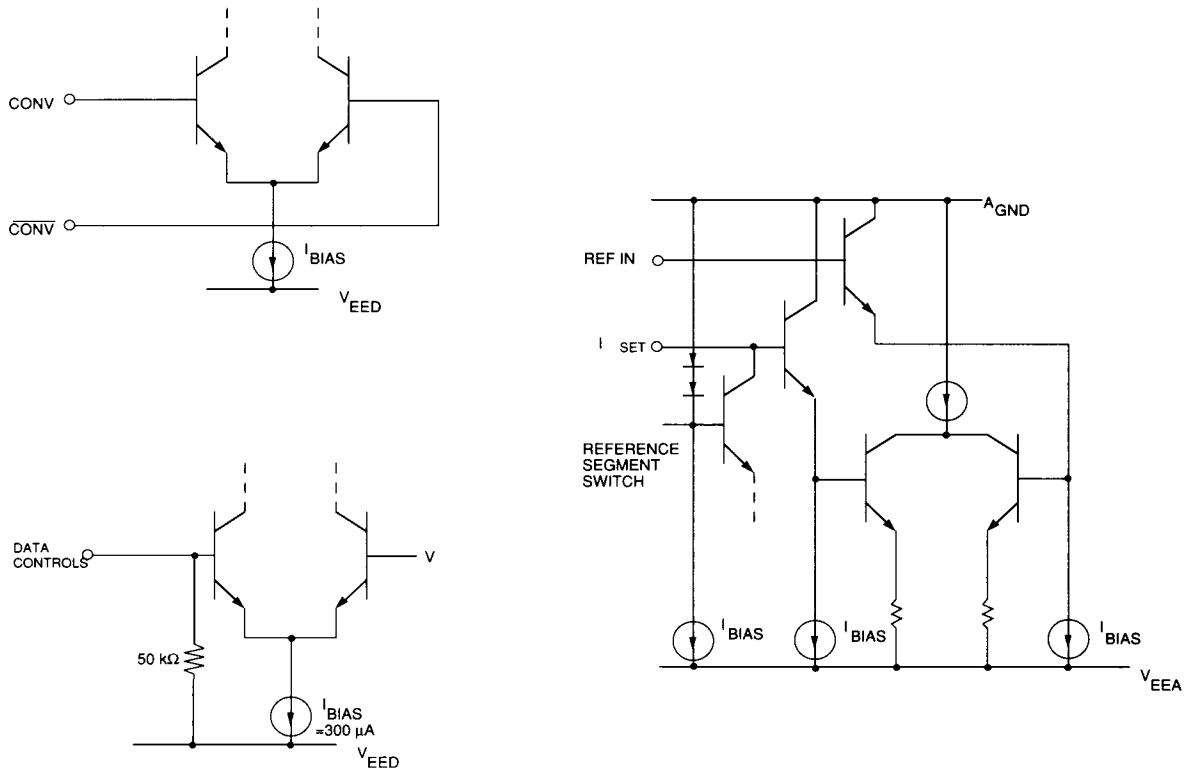
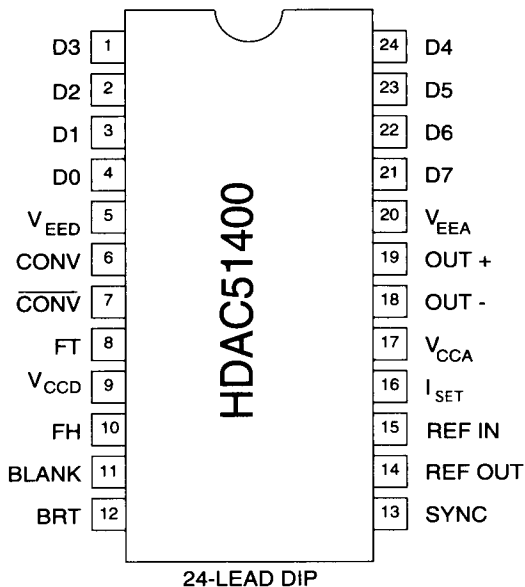


Figure 9 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V _{EED}	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
V _{CCD}	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
REF IN	Reference Input
I _{SET}	Reference Current
V _{CCA}	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
V _{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

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