1 Introduction

The DSP56371 is a high density CMOS device with 5.0-volt compatible inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Finalized specifications may be published after further characterization and device qualifications are completed.

2 DSP56371 Overview

2.1 Introduction

This manual describes the DSP56371 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules. The DSP56371 is a member of the DSP56300 family of programmable CMOS DSPs. The DSP56371 is targeted to applications that require digital audio compression/decompression, sound field processing, acoustic equalization and other digital audio algorithms. Changes in core functionality specific to the DSP56371 are also described in this manual. See Figure 1. for the block diagram of the DSP56371.

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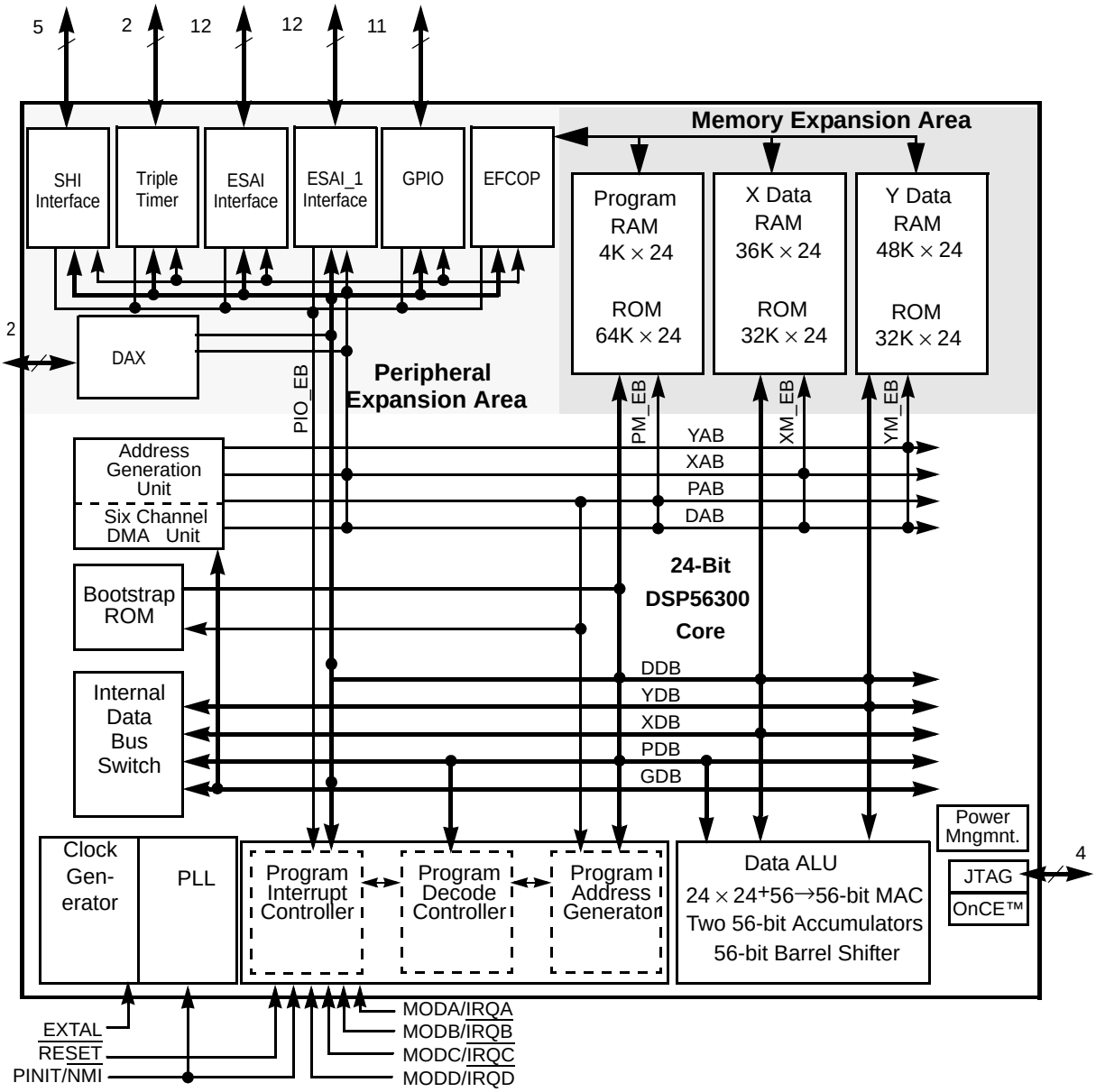


Figure 1. **DSP56371 Block Diagram**

2.2 DSP56300 Core Description

The DSP56371 uses the DSP56300 core, a high-performance, single clock cycle per instruction engine that provides up to twice the performance of Motorola's popular DSP56000 core family while retaining code compatibility with it.

The DSP56300 core family offers a new level of performance in speed and power, provided by its rich instruction set and low power dissipation, thus enabling a new generation of wireless, telecommunications and multimedia products. For a description of the DSP56300 core, see Section 2.4 *DSP56300 Core Functional Blocks*. Significant architectural enhancements to the DSP56300 core family include a barrel shifter, 24-bit addressing, an instruction patch module and direct memory access (DMA).

The DSP56300 core family members contain the DSP56300 core and additional modules. The modules are chosen from a library of standard predesigned elements such as memories and peripherals. New modules may be added to the library to meet customer specifications. A standard interface between the DSP56300 core and the on-chip memory and peripherals supports a wide variety of memory and peripheral configurations. Refer to DSP56371 User Manual, Section 3, *Memory Configuration*.

Core features are described fully in the *DSP56300 Family Manual*. Pinout, memory and peripheral features are described in this manual.

- DSP56300 modular chassis
  - 181 Million Instructions Per Second (MIPS) with a 181 MHz clock at an internal logic supply (QVDDL) of 1.25V.
  - Object Code Compatible with the 56K core.
  - Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
  - Program Control with position independent code support and instruction patch support.
  - EFCOP running concurrently with the core, capable of executing 181 million filter taps per second at peak performance.
  - Six-channel DMA controller.
  - Low jitter, PLL based clocking with a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
  - Internal address tracing support and OnCE for Hardware/Software debugging.
  - JTAG port.
  - Very low-power CMOS design, fully static design with operating frequencies down to DC.
  - STOP and WAIT low-power standby modes.
- On-chip Memory Configuration
  - 48Kx24 Bit Y-Data RAM and 32Kx24 Bit Y-Data ROM.
  - 36Kx24 Bit X-Data RAM and 32Kx24 Bit X-Data ROM.
  - 64Kx24 Bit Program and Bootstrap ROM.
  - 4Kx24 Bit Program RAM.
  - PROM patching mechanism.
  - Up to 32Kx24 Bit from Y Data RAM and 8Kx24 Bit from X Data RAM can be switched to Program RAM resulting in up to 44Kx24 Bit of Program RAM.
- Peripheral modules
  - Enhanced Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Left justified, Right justified, Sony, AC97, network and other programmable protocols.
  - Enhanced Serial Audio Interface I (ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Left justified, Right justified, Sony, AC97, network and other programmable protocols.
  - Serial Host Interface (SHI): SPI and I^2C protocols, multi master capability in I^2C mode, 10-word receive FIFO, support for 8, 16 and 24-bit words.
  - Triple Timer module (TEC).
  - 11 dedicated GPIO pins
  - Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
  - Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

2.3 DSP56371 Audio Processor Architecture

This section defines the DSP56371 audio processor architecture. The audio processor is composed of the following units:

- The DSP56300 core is composed of the Data ALU, Address Generation Unit, Program Controller, DMA Controller, Memory Module Interface, Peripheral Module Interface and the On-Chip Emulator (OnCE). The DSP56300 core is described in the document *DSP56300 24-Bit Digital Signal Processor Family Manual, Motorola publication DSP56300FM/AD*.
- Phased Lock Loop and Clock Generator
- Memory modules.
- Peripheral modules. The peripheral modules are defined in the following sections.

Memory sizes in the block diagram are defaults. Memory may be differently partitioned, according to the memory mode of the chip. See Section 2.4.7 *On-Chip Memory* for more details about memory size.

2.4 DSP56300 Core Functional Blocks

The DSP56300 core provides the following functional blocks:

- Data arithmetic logic unit (Data ALU)
- Address generation unit (AGU)

- Program control unit (PCU)
- DMA controller (with six channels)
- Instruction patch controller
- PLL-based clock oscillator
- OnCE module
- Memory

In addition, the DSP56371 provides a set of on-chip peripherals, described in Section 2.5 *Peripheral Overview*.

2.4.1 Data ALU

The Data ALU performs all the arithmetic and logical operations on data operands in the DSP56300 core. The components of the Data ALU are as follows:

- Fully pipelined 24-bit × 24-bit parallel multiplier-accumulator (MAC)
- Bit field unit, comprising a 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
- Conditional ALU instructions
- 24-bit or 16-bit arithmetic support under software control
- Four 24-bit input general purpose registers: X1, X0, Y1 and Y0
- Six Data ALU registers (A2, A1, A0, B2, B1 and B0) that are concatenated into two general purpose, 56-bit accumulators (A and B), accumulator shifters
- Two data bus shifter/limiter circuits

2.4.1.1 Data ALU Registers

The Data ALU registers can be read or written over the X memory data bus (XDB) and the Y memory data bus (YDB) as 24- or 48-bit operands (or as 16- or 32-bit operands in 16-bit arithmetic mode). The source operands for the Data ALU, which can be 24, 48, or 56 bits (16, 32, or 40 bits in 16-bit arithmetic mode), always originate from Data ALU registers. The results of all Data ALU operations are stored in an accumulator.

All the Data ALU operations are performed in two clock cycles in pipeline fashion so that a new instruction can be initiated in every clock, yielding an effective execution rate of one instruction per clock cycle. The destination of every arithmetic operation can be used as a source operand for the immediately following arithmetic operation without a time penalty (i.e., without a pipeline stall).

2.4.1.2 Multiplier-Accumulator (MAC)

The MAC unit comprises the main arithmetic processing unit of the DSP56300 core and performs all of the calculations on data operands. In the case of arithmetic instructions, the unit accepts as many as three input operands and outputs one 56-bit result of the following form- Extension:Most Significant Product:Least Significant Product (EXT:MSP:LSP).

The multiplier executes 24-bit × 24-bit, parallel, fractional multiplies, between two's-complement signed, unsigned, or mixed operands. The 48-bit product is right-justified and added to the 56-bit contents of either the A or B accumulator. A 56-bit result can be stored as a 24-bit operand. The LSP can either be truncated or rounded into the MSP. Rounding is performed if specified.

2.4.2 Address Generation Unit (AGU)

The AGU performs the effective address calculations using integer arithmetic necessary to address data operands in memory and contains the registers used to generate the addresses. It implements four types of arithmetic: linear, modulo, multiple wrap-around modulo and reverse-carry. The AGU operates in parallel with other chip resources to minimize address-generation overhead.

The AGU is divided into two halves, each with its own Address ALU. Each Address ALU has four sets of register triplets, and each register triplet is composed of an address register, an offset register and a modifier register. The two Address ALUs are identical. Each contains a 24-bit full adder (called an offset adder).

A second full adder (called a modulo adder) adds the summed result of the first full adder to a modulo value that is stored in its respective modifier register. A third full adder (called a reverse-carry adder) is also provided.

The offset adder and the reverse-carry adder are in parallel and share common inputs. The only difference between them is that the carry propagates in opposite directions. Test logic determines which of the three summed results of the full adders is output.

Each Address ALU can update one address register from its respective address register file during one instruction cycle. The contents of the associated modifier register specifies the type of arithmetic to be used in the address register update calculation. The modifier value is decoded in the Address ALU.

2.4.3 Program Control Unit (PCU)

The PCU performs instruction prefetch, instruction decoding, hardware DO loop control and exception processing. The PCU implements a seven-stage pipeline and controls the different processing states of the DSP56300 core. The PCU consists of the following three hardware blocks:

- Program decode controller (PDC)
- Program address generator (PAG)
- Program interrupt controller

The PDC decodes the 24-bit instruction loaded into the instruction latch and generates all signals necessary for pipeline control. The PAG contains all the hardware needed for program address generation, system stack and loop control. The Program interrupt controller arbitrates among all interrupt requests (internal interrupts, as well as the five external requests: $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$ and $\overline{\text{NMI}}$) and generates the appropriate interrupt vector address.

PCU features include the following:

- Position independent code support
- Addressing modes optimized for DSP applications (including immediate offsets)
- On-chip instruction cache controller
- On-chip memory-expandable hardware stack
- Nested hardware DO loops
- Fast auto-return interrupts

The PCU implements its functions using the following registers:

- PC—program counter register
- SR—Status register
- LA—loop address register
- LC—loop counter register
- VBA—vector base address register
- SZ—stack size register
- SP—stack pointer
- OMR—operating mode register
- SC—stack counter register

The PCU also includes a hardware system stack (SS).

2.4.4 Internal Buses

To provide data exchange between blocks, the following buses are implemented:

- Peripheral input/output expansion bus (PIO_EB) to peripherals
- Program memory expansion bus (PM_EB) to program memory
- X memory expansion bus (XM_EB) to X memory
- Y memory expansion bus (YM_EB) to Y memory
- Global data bus (GDB) between registers in the DMA, AGU, OnCE, PLL, BIU and PCU, as well as the memory-mapped registers in the peripherals
- DMA data bus (DDB) for carrying DMA data between memories and/or peripherals
- DMA address bus (DAB) for carrying DMA addresses to memories and peripherals
- Program Data Bus (PDB) for carrying program data throughout the core
- X memory Data Bus (XDB) for carrying X data throughout the core
- Y memory Data Bus (YDB) for carrying Y data throughout the core
- Program address bus (PAB) for carrying program memory addresses throughout the core
- X memory address bus (XAB) for carrying X memory addresses throughout the core
- Y memory address bus (YAB) for carrying Y memory addresses throughout the core

All internal buses on the DSP56300 family members are 24-bit buses. See Figure 1.

2.4.5 Direct Memory Access (DMA)

The DMA block has the following features:

- Six DMA channels supporting internal and external accesses
- One-, two- and three-dimensional transfers (including circular buffering)
- End-of-block-transfer interrupts
- Triggering from interrupt lines and all peripherals

2.4.6 PLL-based Clock Oscillator

The clock generator in the DSP56300 core is composed of two main blocks: the PLL, which performs clock input division, frequency multiplication, skew elimination and the clock generator (CLKGEN), which performs low-power division and clock pulse generation. PLL-based clocking:

- Allows change of low-power divide factor (DF) without loss of lock
- Provides output clock with skew elimination
- Provides a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31), PLL feedback multiplier (2 or 4), Output divide factor (1, 2 or 4) and a power-saving clock divider (2^i: i = 0 to 7) to reduce clock noise

The PLL allows the processor to operate at a high internal clock frequency using a low frequency clock input. This feature offers two immediate benefits:

- A lower frequency clock input reduces the overall electromagnetic interference generated by a system.
- The ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system.

NOTE

The PLL will momentarily overshoot the target frequency when the PLL is first enabled or when the VCO frequency is modified. It is important that when modifying the PLL frequency or enabling the PLL that the two step procedure defined in Section 3, *DSP56371 Overview* be followed.

2.4.7 On-Chip Memory

The memory space of the DSP56300 core is partitioned into program memory space, X data memory space and Y data memory space. The data memory space is divided into X and Y data memory in order to work with the two Address ALUs and to feed two operands simultaneously to the Data ALU. Memory space includes internal RAM and ROM and can not be expanded off-chip.

There is an instruction patch module. The patch module is used to patch program ROM. The memory switch mode is used to increase the size of program RAM as needed (switch from X data RAM and/or Y data RAM).

There are on-chip ROMs for program and bootstrap memory (64K x 24-bit), X ROM (32K x 24-bit) and Y ROM(32K x 24-bit).

More information on the internal memory is provided in DSP56371 User Manual, Section 3, *Memory*Section 3, .

2.4.8 Off-Chip Memory Expansion

Memory cannot be expanded off-chip. There is no external memory bus.

2.5 Peripheral Overview

The DSP56371 is designed to perform a wide variety of fixed-point digital signal processing functions. In addition to the core features previously discussed, the DSP56371 provides the following peripherals:

- As many as 39 dedicate or user-configurable general purpose input/output (GPIO) signals
- Timer/event counter (TEC) module, containing three independent timers
- Memory switch mode in on-chip memory
- Four external interrupt/mode control lines and one external non-maskable interrupt line
- Enhanced serial audio interface (ESAI) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols
- A second enhanced serial audio interface (ESAI_1) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols.
- Serial host interface (SHI) using SPI and I^2C protocols, with multi-master capability, 10-word receive FIFO and support for 8-, 16- and 24-bit words
- A Digital audio transmitter (DAX): a serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats

2.5.1 General Purpose Input/Output (GPIO)

The DSP56371 provides 11 dedicated GPIO and 28 programmable signals that can operate either as GPIO pins or peripheral pins (ESAI, ESAI_1, DAX, and TEC). The signals are configured as GPIO after hardware reset. Register programming techniques for all GPIO functionality among these interfaces are very similar and are described in the following sections.

2.5.2 Triple Timer (TEC)

This section describes a peripheral module composed of a common 21-bit prescaler and three independent and identical general purpose 24-bit timer/event counters, each one having its own register set.

Each timer can use internal or external clocking and can interrupt the DSP after a specified number of events (clocks). Two of the three timers can signal an external device after counting internal events. Each timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurred. Two of the three timers connect to the external world through bidirectional pins (TIO0, TIO1). When a TIO pin is configured as input, the timer functions as an external event counter or can measure external pulse width/signal period. When a TIO pin is used as output the timer is functioning as either a timer, a watchdog or a Pulse Width Modulator. When a TIO pin is not used by the timer it can be used as a General Purpose Input/Output Pin. Refer to DSP56371 User Manual, Section 11, *Triple Timer Module.*

2.5.3 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, microprocessors and peripherals that implement the Motorola SPI serial protocol. The ESAI consists of independent transmitter and receiver sections, each with its own clock generator. It is a superset of the DSP56300 family ESSI peripheral and of the DSP56000 family SAI peripheral. For more information on the ESAI, refer to DSP56371 User Manual, Section 8, *Enhanced Serial Audio Interface (ESAI).*

2.5.4 Enhanced Serial Audio Interface 1 (ESAI_1)

The ESAI_1 is a second ESAI interface. The ESAI_1 is functionally identical to ESAI. For more information on the ESAI_1, refer to DSP56371 User Manual, Section 9, *Enhanced Serial Audio Interface (ESAI_1).*

2.5.5 Serial Host Interface (SHI)

The SHI is a serial input/output interface providing a path for communication and program/coefficient data transfers between the DSP and an external host processor. The SHI can also communicate with other serial peripheral devices. The SHI can interface directly to either of two well-known and widely used synchronous serial buses: the Motorola serial peripheral interface (SPI) bus

and the Philips inter-integrated-circuit control (I^2C) bus. The SHI supports either the SPI or I^2C bus protocol, as required, from a slave or a single-master device. To minimize DSP overhead, the SHI supports single-, double- and triple-byte data transfers. The SHI has a 10-word receive FIFO that permits receiving up to 30 bytes before generating a receive interrupt, reducing the overhead for data reception. For more information on the SHI, refer to DSP56371 User Manual, Section 7, *Serial Host Interface.*

2.5.6 Digital Audio Transmitter (DAX)

The DAX is a serial audio interface module that outputs digital audio data in the AES/EBU, CP-340 and IEC958 formats. For more information on the DAX, refer to DSP56371 User Manual, Section 10, *Digital Audio*.

3 Signal/Connection Descriptions

3.1 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 1. and illustrated in Figure 2.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{DD})		12	Table 2.
Ground (GND)		12	Table 3.
Scan Pins		1	Table 4.
Clock and PLL		2	Table 5.
Interrupt and mode control		5	Table 6.
SHI		5	Table 7.
ESAI	Port C[1]	12	Table 8.
ESAI_1	Port E[2]	12	Table 9.
SPDIF Transmitter (DAX)	Port D[3]	2	Table 10.
Dedicated GPIO	Port F[4]	11	Table 11.
Timer		2	Table 12.
JTAG/OnCE Port		4	Table 13.

Notes:
1. Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
2. Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.
3. Port D signals are the GPIO port signals which are multiplexed with the DAX signals.
4. Port F signals are the dedicated GPIO port signals.

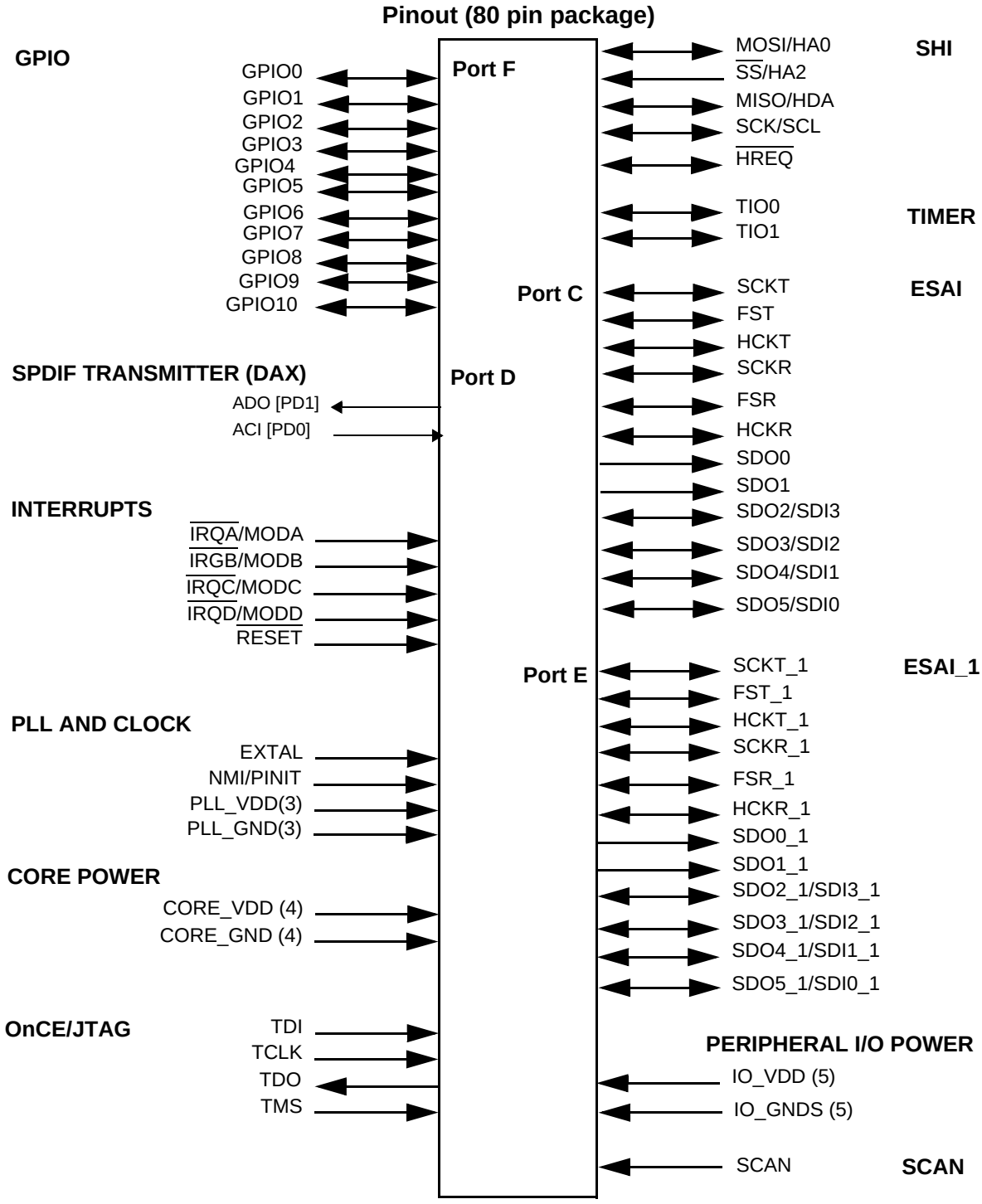


Figure 2. **Signals Identified by Functional Group**

3.2 Power

Table 2. Power Inputs

Power Name	Description
PLLA_VDD (1) PLLP_VDD(1)	**PLL Power**— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
PLLD_VDD (1)	**PLL Power—** The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
CORE_VDD (4)	**Core Power**—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate decoupling capacitors.
IO_VDD (5)	**SHI, ESAI, ESAI_1, DAX and Timer I/O Power** —The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, DAX and Timer I/O. The user must provide adequate external decoupling capacitors.

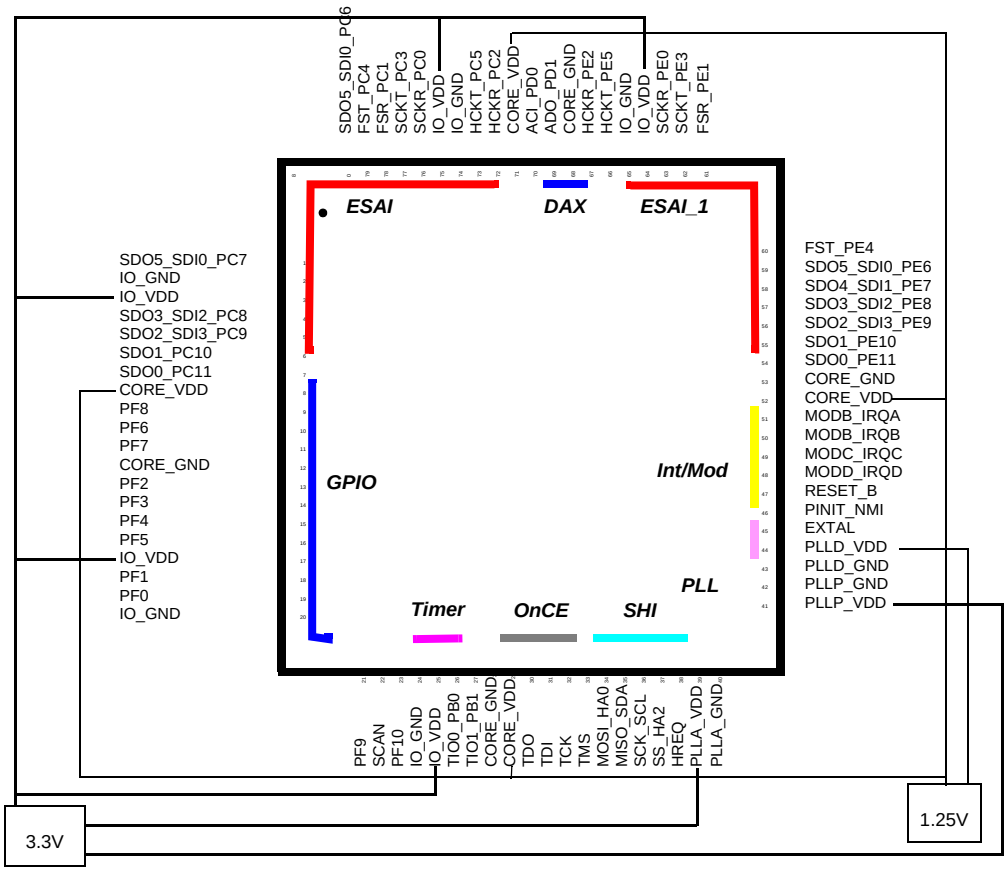


Figure 3. **VDD Connections**

3.3 Ground

Table 3. Grounds

Ground Name	Description
PLLA_GND(1) PLLP_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
PLLD_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
CORE_GND (4)	**Core Ground**—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND (5)	**SHI, ESAI, ESAI_1, DAX and Timer I/O Ground**—IO_GND is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

3.4 SCAN

Table 4. SCAN signals

Signal Name	Type	State during Reset	Signal Description
SCAN	Input	Input	**SCAN**—Manufacturing test pin. This pin should be pulled low. *Internal Pull down resistor.*

3.5 Clock and PLL

Table 5. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input cannot tolerate 5 V.*
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. *Internal Pull up resistor.* *This input is 5 V tolerant.*

3.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 6. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA/$\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/$\overline{\text{IRQA}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/$\overline{\text{IRQA}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into the OMR when the $\overline{\text{RESET}}$ signal is deasserted. If the processor is in the stop standby state and the MODA/$\overline{\text{IRQA}}$ pin is pulled to GND, the processor will exit the stop state. *Internal Pull up resistor.* *This input is 5 V tolerant.*
MODB/$\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/$\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. *Internal Pull up resistor.* *This input is 5 V tolerant.*
MODC/$\overline{\text{IRQC}}$	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/$\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. *Internal Pull up resistor.* *This input is 5 V tolerant.*
MODD/$\overline{\text{IRQD}}$	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. *Internal Pull up resistor.* *This input is 5 V tolerant.*

Table 6. Interrupt and Mode Control (Continued)

Signal Name	Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. *Internal Pull up resistor.* *This input is 5 V tolerant.*

3.7 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 7. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{\text{SS}}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		**I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through a pull-up resistor. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. *Internal Pull up resistor.* *This input is 5 V tolerant.*

Table 7. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
MISO	Input or output	Tri-stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		**I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and it is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. *Internal Pull up resistor.* *This input is 5 V tolerant.*
MOSI	Input or output	Tri-stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		**I^2C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for I^2C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^2C master mode. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. *Internal Pull up resistor.* *This input is 5 V tolerant.*

Table 7. Serial Host Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
$\overline{SS}$	Input	Tri-stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I^2C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for the I^2C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^2C master mode. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. *Internal Pull up resistor.* *This input is 5 V tolerant.*
$\overline{HREQ}$	Input or Output	Tri-stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for an external pull-up in this state. *Internal Pull up resistor.* *This input is 5 V tolerant.*

3.8 Enhanced Serial Audio Interface

Table 8. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected		**Port C2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
HCKT	Input or output	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected		**Port C5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 8. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR	Input or output	GPIO disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected		**Port C1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
FST	Input or output	GPIO disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		**Port C4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 8. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		**Port C0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SCKT	Input or output	GPIO disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		**Port C3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO5	Output	GPIO disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		**Port C6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 8. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO4	Output	GPIO disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		**Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		**Port C7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO3	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		**Port C8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 8. Enhanced Serial Audio Interface Signals (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO2	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		**Port C9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO1	Output	GPIO disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		**Port C10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO0	Output	GPIO disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		**Port C11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

3.9 Enhanced Serial Audio Interface_1

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		**Port E2**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
HCKT_1	Input or output	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		**Port E5**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	**Frame Sync for Receiver_1**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected		**Port E1**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
FST_1	Input or output	GPIO disconnected	**Frame Sync for Transmitter_1**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).
PE4	Input, output, or disconnected		**Port E4**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	**Receiver Serial Clock_1**—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected		**Port E0**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SCKT_1	Input or output	GPIO disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected		**Port E3**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO5_1	Output	GPIO disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		**Serial Data Input 0_1**—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		**Port E6**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO4_1	Output	GPIO disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		**Serial Data Input 1_1**—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		**Port E7**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		**Port E8**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO2_1	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		**Port E9**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO1_1 PE10	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 1**—SDO1_1 is used to transmit data from the TX1 serial transmit shift register. **Port E10**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
SDO0_1 PE11	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 0**—SDO0_1 is used to transmit data from the TX0 serial transmit shift register. **Port E11**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

3.10 SPDIF Transmitter Digital Audio Interface

Table 10. Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI PD0	Input Input, output, or disconnected	GPIO Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively). **Port D0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 10. Digital Audio Interface (DAX) Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
ADO	Output	GPIO Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/SPDIF, CP340 and IEC958 data in a biphase mark format.
PD1	Input, output, or disconnected		**Port D1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

3.11 Dedicated GPIO Interface

Table 11. Dedicated GPIO Signals

Signal Name	Type	State During Reset	Signal Description
PF0	Input, output, or disconnected	GPIO disconnected	**Port F0**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF1	Input, output, or disconnected	GPIO disconnected	**Port F1**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF2	Input, output, or disconnected	GPIO disconnected	**Port F2**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF3	Input, output, or disconnected	GPIO disconnected	**Port F3**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

Table 11. Dedicated GPIO Signals (Continued)

Signal Name	Type	State During Reset	Signal Description
PF4	Input, output, or disconnected	GPIO disconnected	**Port F4**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF5	Input, output, or disconnected	GPIO disconnected	**Port F5**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF6	Input, output, or disconnected	GPIO disconnected	**Port F6**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF7	Input, output, or disconnected	GPIO disconnected	**Port F7**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF8	Input, output, or disconnected	GPIO disconnected	**Port F8**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF9	Input, output, or disconnected	GPIO disconnected	**Port F9**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*
PF10	Input, output, or disconnected	GPIO disconnected	**Port F10**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *Internal Pull down resistor.* *This input is 5 V tolerant.*

3.12 Timer

Table 12. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to VDD through a pull-up resistor in order to ensure a stable logic level at this input. *Internal Pull down resistor.* *This input is 5 V tolerant.*
TIO1	Input or Output	GPIO Input	**Timer 1 Schmitt-Trigger Input/Output**—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1 control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to Vdd through a pull-up resistor in order to ensure a stable logic level at this input. *Internal Pull down resistor.* *This input is 5 V tolerant.*

3.13 JTAG/OnCE Interface

Table 13. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. *Internal Pull up resistor.* *This input is 5 V tolerant..*

Table 13. JTAG/OnCE Interface (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. *Internal Pull up resistor.* *This input is 5 V tolerant.*
TDO	Output	Tri-state	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. *Internal Pull up resistor.* *This input is 5 V tolerant.*

4 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{DD}). The suggested value for a pullup or pulldown resistor is 10 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 14. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	−0.3 to + 1.6	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	−0.3 to + 4.0	V

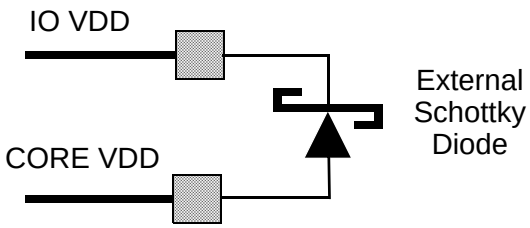
Table 14. Maximum Ratings (Continued)

Rating[1]	Symbol	Value[1, 2]	Unit
All “5.0V tolerant” input voltages	V_{IN}	GND — 0.3 to 5.5V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
SCK_SCL	I_{SCK}	16	mA
ACI_PD0,ADO_PD1	I_{DAX}	24	mA
TDO	Ijtag	24	mA
Operating temperature range[3]	T_J	-40 to +115	°C
Storage temperature	T_{STG}	—55 to +125	°C

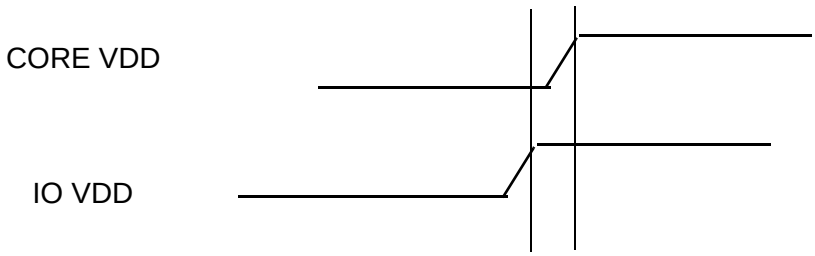
Notes:
1. GND = 0 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL = 50PF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Operating temperature qualified for automotive applications.

5 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, the connection shown below is recommended to be made between the DSP56371 IO_VDD and CORE_VDD power pins.



To prevent a high current condition upon power up, the IOVDD must be applied ahead of the CORE VDD as shown below if the external Schottcky is not used.



6 Thermal Characteristics

Table 15. Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	$R_{\theta JA}$ or θ_{JA}	39	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	18.25	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

7 DC Electrical Characteristics

Table 16. DC ELECTRICAL CHARACTERISTICS[4]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (core_vdd) • PLL (plld_vdd)	V_{DD}	1.2	1.25	1.3[1]	V
Supply voltages • Vio_vdd • PLL (pllp_vdd) • PLL (plla_vdd)	V_{DDIO}	3.14	3.3	3.46[1]	V
Input high voltage • All pins	V_{IH}	2.0	—	V_{IO_VDD}+2V	V
Note: All 3.3 volt supplies must rise prior to the rise of the 1.25 volt supplies to avoid a high current condition and possible system damage.					
Input low voltage • All pins	V_{IL}	–0.3	—	0.8	V
Input leakage current (All pins)	I_{IN}	—	—	84	µA
Clock pin Input Capacitance (EXTAL)	C_{IN}		3.749		pF
High impedance (off-state) input current (@ 3.46 V)	I_{TSI}	–84	—	84	µA
Output high voltage I_{OH} = -5 mA	V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 5 mA	V_{OL}	—	—	0.4	V
Internal supply current[1] at internal clock of 181MHz • In Normal mode	I_{CCI}	—	99	200	mA
• In Wait mode	I_{CCW}	—	48	150	mA
• In Stop mode[3]	I_{CCS}	—	2.5	82	mA
IO supply current		—	115	150	mA
Input capacitance[4]	C_{IN}	—	—	10	pF

Notes:
1. The Section 3, *Power Consumption Considerations* section provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.25V, V_{DD_IO} = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.30V, $V_{IO\_VDD)}$ = 3.46V at T_J = 115°C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
3. Periodically sampled and not 100% tested
4. T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL=50pF

8 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56371 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 1.0V and 1.8V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz (PLL bypassed), the device AC test conditions are 5 MHz and rated speed.

9 Internal Clocks

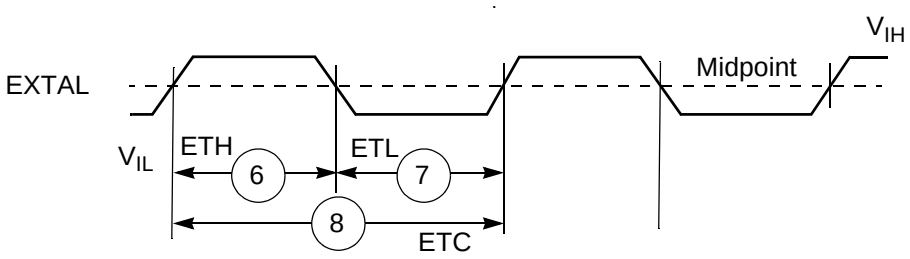
Table 17. INTERNAL CLOCKS

No.	Characteristics	Symbol	Min	Typ	Max	UNIT	Condition
1	Comparison Frequency	Fref[1]	5	--	20	MHZ	Fref = FN/NR
2	Input Clock Frequency	FIN	Fref*NR				NR is input divider value
3	Output clock Frequency (with PLL enabled[2,3]	FOUT	75	(1000/Etc × MF x FM)/ (PDF × DF x OD)	--	MHZ	FOUT=FVCO/NO where NO is output divider value
4	Output clock Frequency (with PLL disabled[2,3]	FOUT	--	1000/Etc	--	MHZ	---
5	Duty Cycle	--	40	50	60	%	FVCO=300MHZ~600MHZ

Notes:
1. See users manual for definition.
2. DF = Division Factor
   Ef = External frequency
   MF = Multiplication Factor
   PDF = Predivision Factor
   FM= Feedback Multiplier
   OD = Output Divider
3. Maximum frequency will vary depending on the ordered part number.

10 External Clock Operation

The DSP56371 system clock is an externally supplied square wave voltage source connected to EXTAL (see Figure 4).



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 4. **External Clock Timing**

Table 18. Clock Operation 150 and 181 MHz Values

No.	Characteristics	Symbol	150 MHz		181 MHz	
			Min	Max	Min	Max
6	EXTAL input high [1,2] (40% to 60% duty cycle)	Eth	3.33ns	100ns	2.75ns	100ns
7	EXTAL input low[1,2] (40% to 60% duty cycle)	Etl	3.33ns	100ns	2.75ns	100ns
8	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	Etc	 6.66ns 6.66ns	 inf 200ns	 5.52ns 5.52ns	 inf 200ns
9	Instruction cycle time= I_{CYC} = T_C[3] • With PLL disabled • With PLL enabled	Icyc	 6.66ns 6.66ns	 inf 13.0ns	 5.52ns 5.52ns	 inf 13.0ns

Notes:
1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3. The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.
4. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

11 Reset, Stop, Mode Select, and Interrupt Timing

Table 19. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all output pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 2 x T_C 2 x T_C	 11.1 11.1	 — --	 ns ns
12	Syn reset setup time from RESET • Maximum	 T_C	 —	 5.5	 ns
13	Syn reset de assert delay time • Minimum • Maximum(PLL enabled)	 2× T_C (2xT_C)+T_{LOCK}	 11.1 5.0	 — 	 ns ms
14	Mode select setup time		10.0	—	ns
15	Mode select hold time		10.0	—	ns
16	Minimum edge-triggered interrupt request assertion width	2 xT_C	11.1	—	ns
17	Minimum edge-triggered interrupt request deassertion width	2 xT_C	11.1	—	ns
18	Delay from interrupt trigger to interrupt code execution.	10 xT_C + 5	60.0		ns
19	Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1) • PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0) • PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	 9+(128K× T_C) 25× T_C 9+(128KxT_C)+T_{lock} (25 x T_C)+T_{lock}	 704 138 5.7 5	 — — 	 us ns ms ms
20	• Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	10 x T_C + 3.0		59.0	ns

Table 19. Reset, Stop, Mode Select, and Interrupt Timing (Continued)

No.	Characteristics	Expression	Min	Max	Unit
21	Interrupt Requests Rate				
	• ESAI, ESAI_1, SHI, DAX, Timer	12 x T_C	—	—	ns
	• DMA	8 x T_C	—	—	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	8 x T_C	—	—	ns
	• $\overline{IRQ}$ (level trigger)	12 c T_C	—	—	ns
22	DMA Requests Rate				
	• Data read from ESAI, ESAI_1, SHI, DAX	6 x T_C	—	—	ns
	• Data write to ESAI, ESAI_1, SHI, DAX	7 x T_C	—	—	ns
	• Timer	2 x T_C	—	—	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	3 x T_C	—	—	ns

Notes:
1. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, using external clock (PCTL Bit 13 = 0), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.

   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.
3. Periodically sampled and not 100% tested
4. $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other "required $\overline{RESET}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

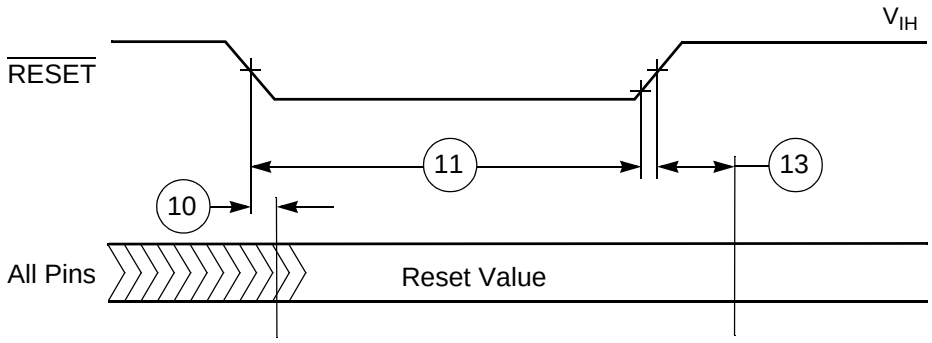


Figure 5. **Reset Timing**

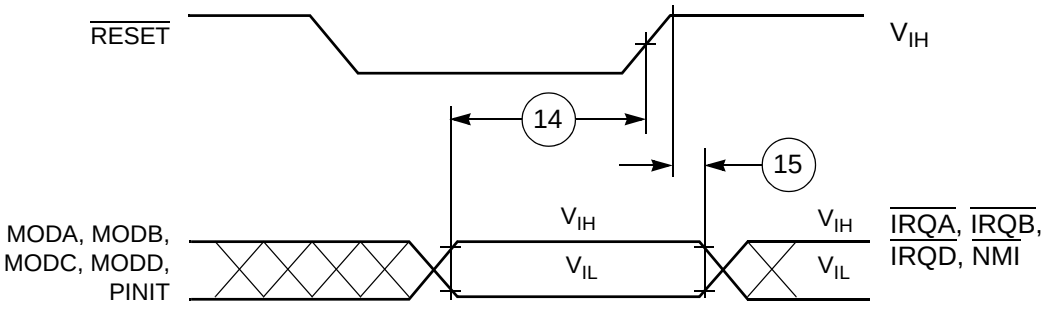


Figure 6. **Recovery from Stop State Using IRQA Interrupt Service**

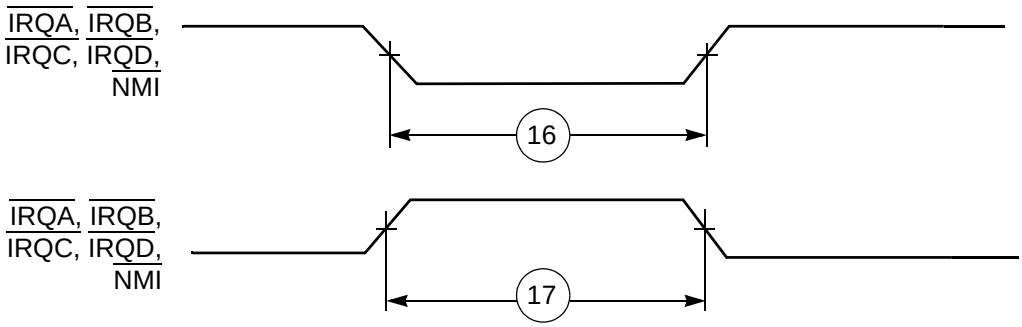
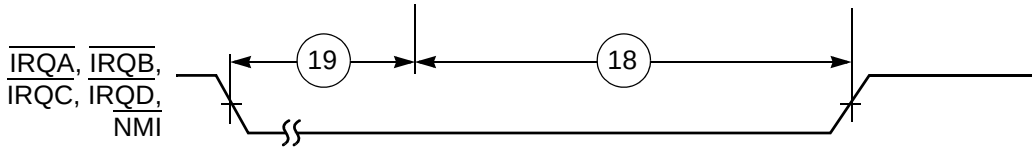
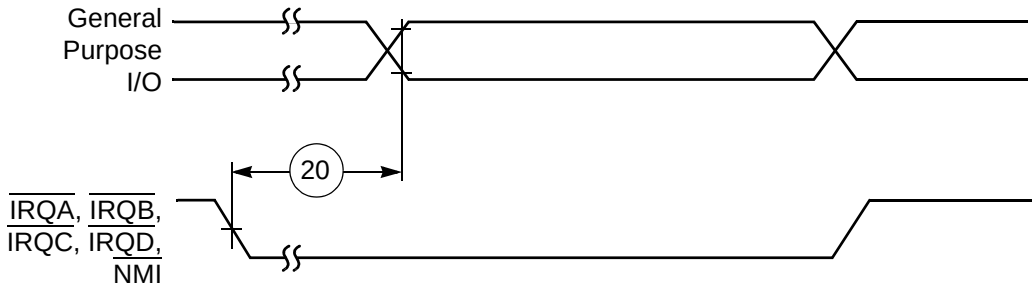


Figure 7. **External Interrupt Timing (Negative Edge-Triggered)**



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 8. **External Fast Interrupt Timing**

12 Serial Host Interface SPI Protocol Timing

Table 20. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1]	Mode	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	79.0	—	ns
24	Serial clock high period	Master	29.5	—	ns
		Slave	25.8	—	ns
25	Serial clock low period	Master	29.5	—	ns
		Slave	25.8	—	ns
26	Serial clock rise/fall time	Master	—	10	ns
		Slave	—	10	ns
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	34.4	—	ns
	CPHA = 1	Slave	10	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	12	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master/Slave	0	—	ns
30	SCK last sampling edge to data input not valid	Master/Slave	22.4	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master/Slave	—	100	ns
34	SCK edge to data out not valid (data out hold time)	Master/Slave	21.4	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	15.0	ns
36	First SCK sampling edge to HREQ output deassertion	Slave	50	—	ns
37	Last SCK sampling edge to HREQ output not deasserted (CPHA = 1)	Slave	52.2	—	ns
38	SS deassertion to HREQ output not deasserted (CPHA = 0)	Slave	46.6	—	ns
39	SS deassertion pulse width (CPHA = 0)	Slave	12.7	—	ns
40	HREQ in assertion to first SCK edge	Master	—	—	ns
41	HREQ in deassertion to last SCK sampling edge (HREQ in set-up time) (CPHA = 1)	Master	0	—	ns
42	First SCK edge to HREQ in not asserted (HREQ in hold time)	Master	0	—	ns
43	HREQ assertion width	Master			ns

Notes:
1. V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. Periodically sampled, not 100% tested

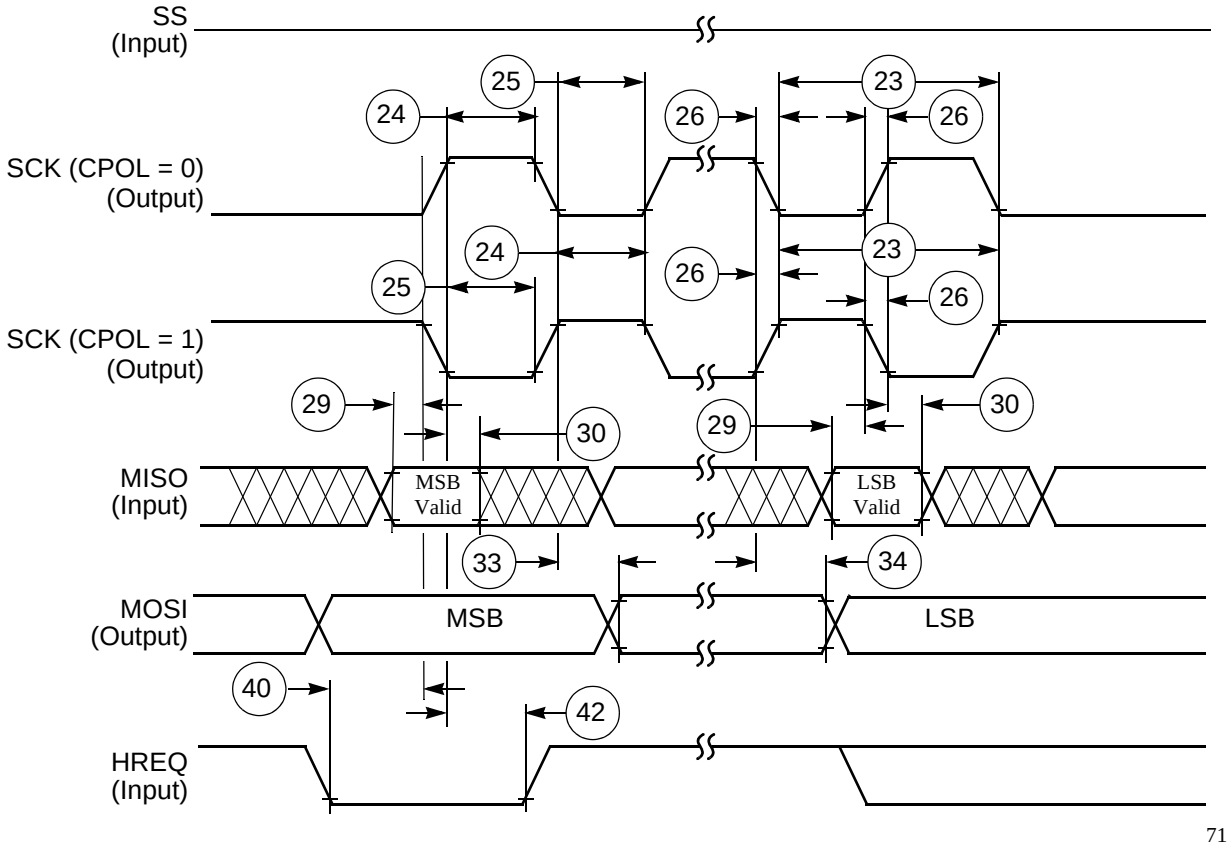


Figure 9. **SPI Master Timing (CPHA = 0)**

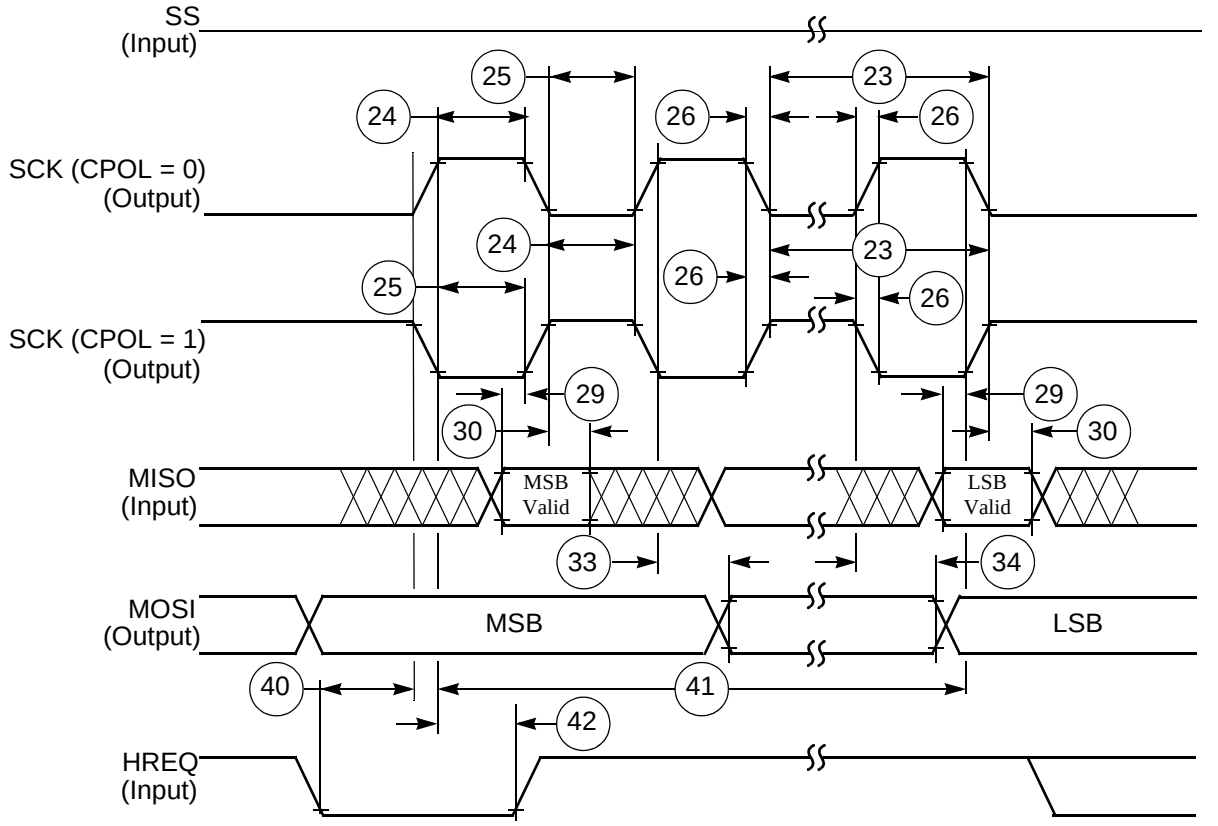


Figure 10. **SPI Master Timing (CPHA = 1)**

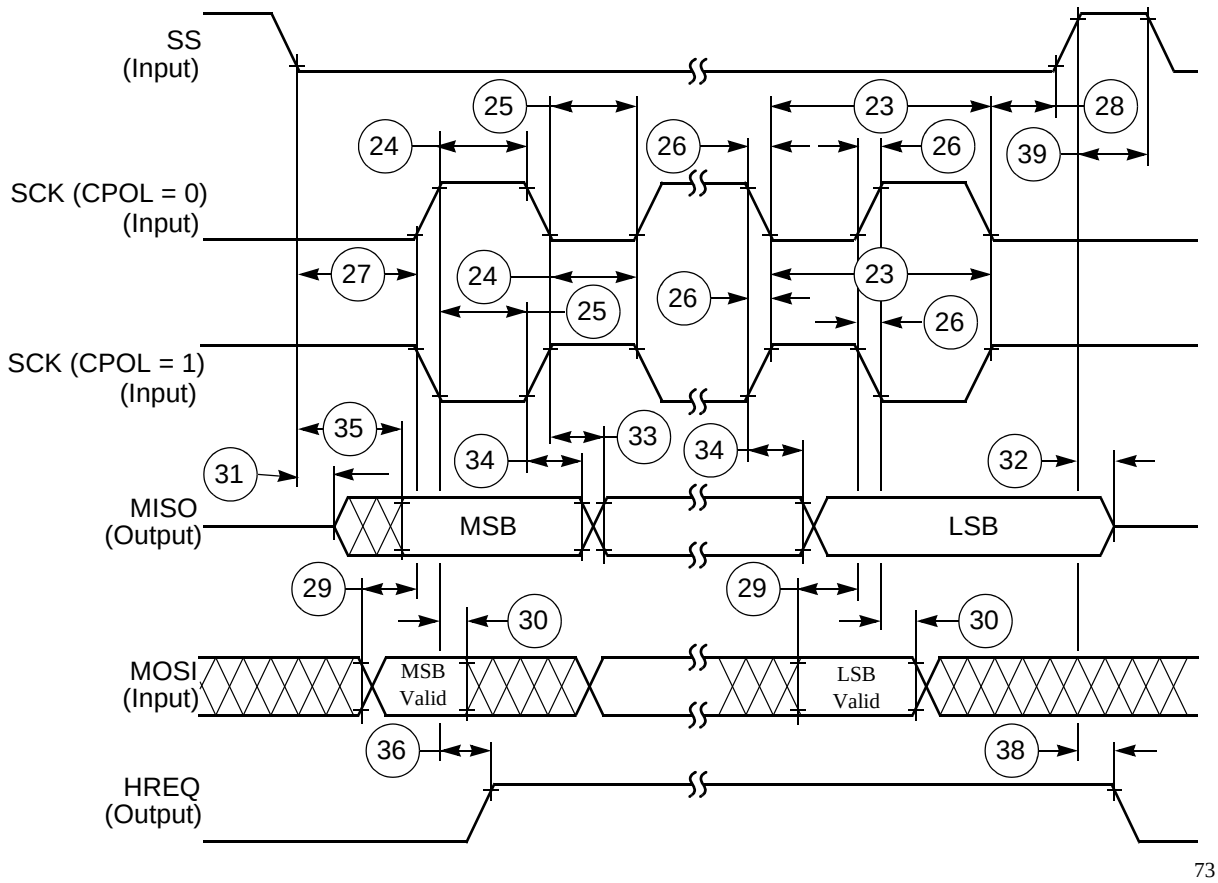


Figure 11. **SPI Slave Timing (CPHA = 0)**

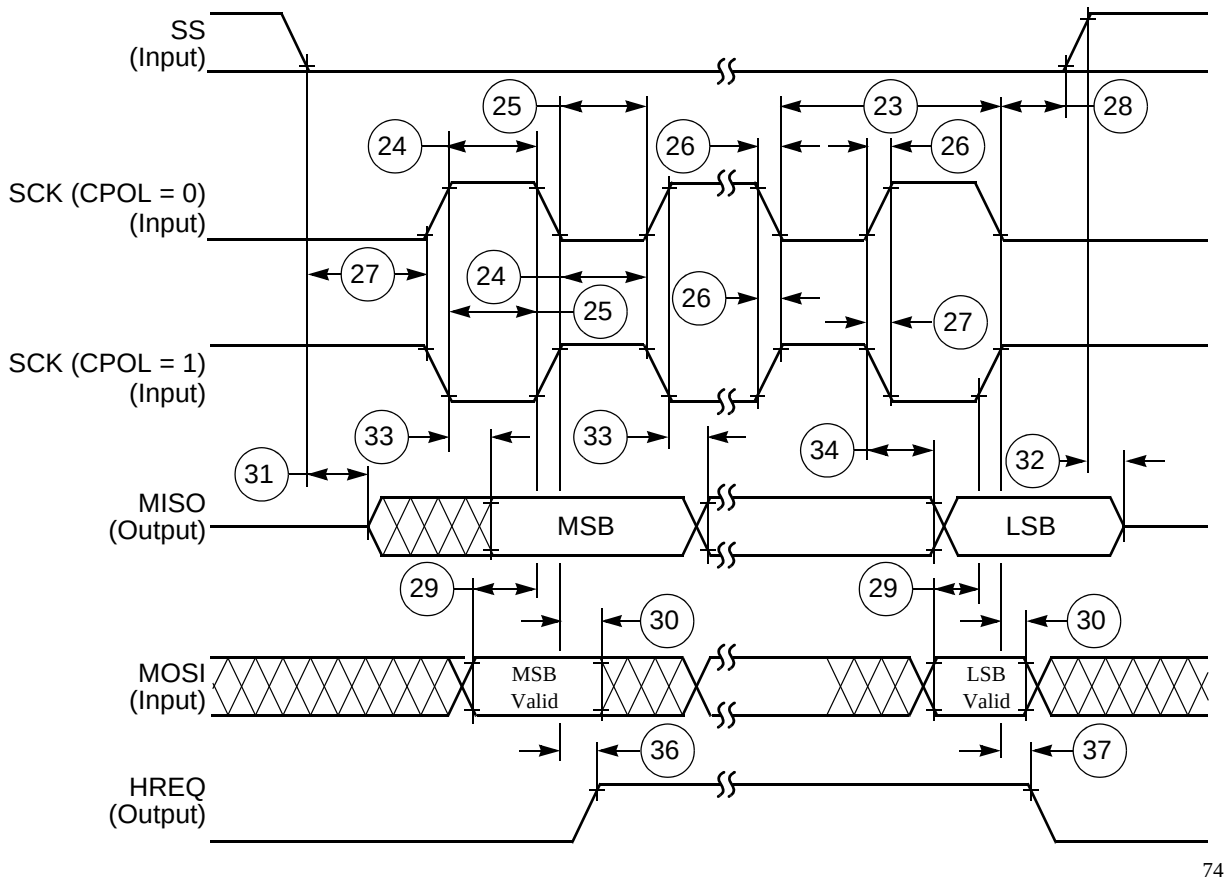


Figure 12. **SPI Slave Timing (CPHA = 1)**

13 Serial Host Interface (SHI) I²C Protocol Timing

Table 21. SHI I²C Protocol Timing

Standard I²C*							
No.	Characteristics[1]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time	T_R	—	5	—	5	ns
51	SCL and SDA fall time	T_F	—	5	—	5	ns
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency	F_{OSC}	10.6	—	28.5	—	MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion	$T_{NG;RQO}$ $4 \times T_C + 30$	—	—	—	—	ns
59	Last SCL edge to HREQ output not deasserted	$T_{AS;RQO}$ $2 \times T_C + 30$	50	—	50	—	ns
60	HREQ in assertion to first SCL edge	$T_{AS;RQI}$ $0.5 \times T_I2_{CCP}$ $-0.5 \times T_C - 21$	4327	—	927	—	ns
61	First SCL edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Note: 1. VCORE_VDD = 1.2 5 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL = 50 pF

13.1 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

— HRS is the pre-scaler rate select bit. When HRS is cleared, the fixed divide-by-eight pre-scaler is operational. When HRS is set, the pre-scaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I^2C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad \text{(if HDM[7:0] = \$02 and HRS = 1)}$$

to

$$4096 \times T_C \quad \text{(if HDM[7:0] = \$FF and HRS = 0)}$$

The programmed serial clock cycle (T_{I^2CCP}), SCL rise time (T_R), should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 22.

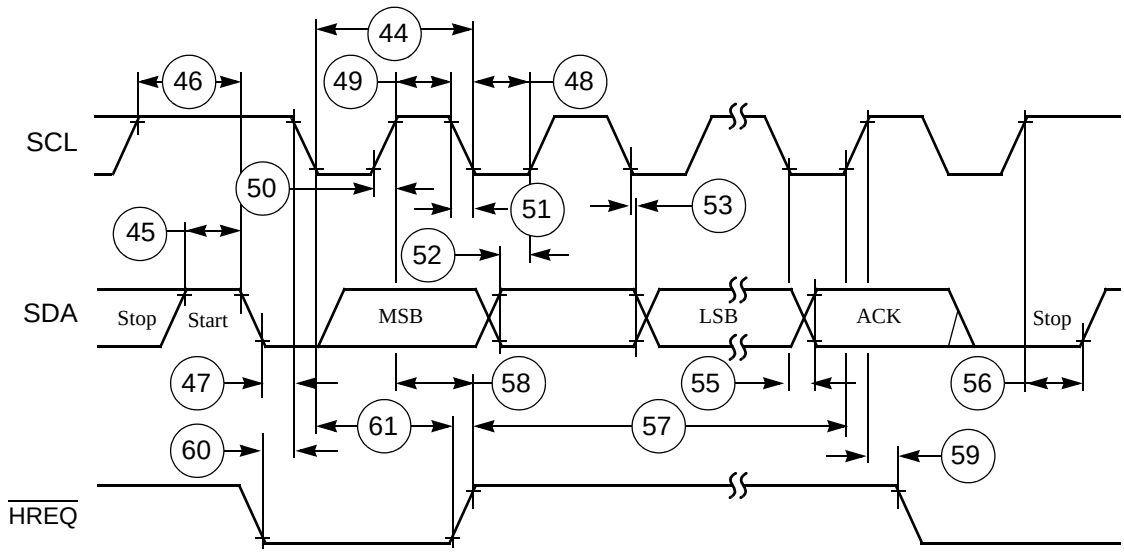


Figure 13. **I^2C Timing**

14 Enhanced Serial Audio Interface Timing

Table 22. Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$	22.3	—	i ck	ns
			$4 \times T_C$	22.3	—	x ck	
			SCKT:max[(3*T_C) or t87]	26.5	—	x ck	
63	Clock high period • For internal clock • For external clock	—	$2 \times T_C - 10.0$ $2 \times T_C$	3.4 10.0	— —		ns
64	Clock low period • For internal clock • For external clock	—	$2 \times T_C - 10.0$ $2 \times T_C$	3.4 10.0	— —		ns
65	SCKR rising edge to FSR out (bl) high	—	—	— —	37.0 22.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	—	—	0.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	—	—	5.0 3.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge [6]	—	—	1.0 23.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	—	—	1.0 23.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	—	—	3.0 0.0	— —	x ck i ck a	ns
76	Flags input setup before SCKR falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns

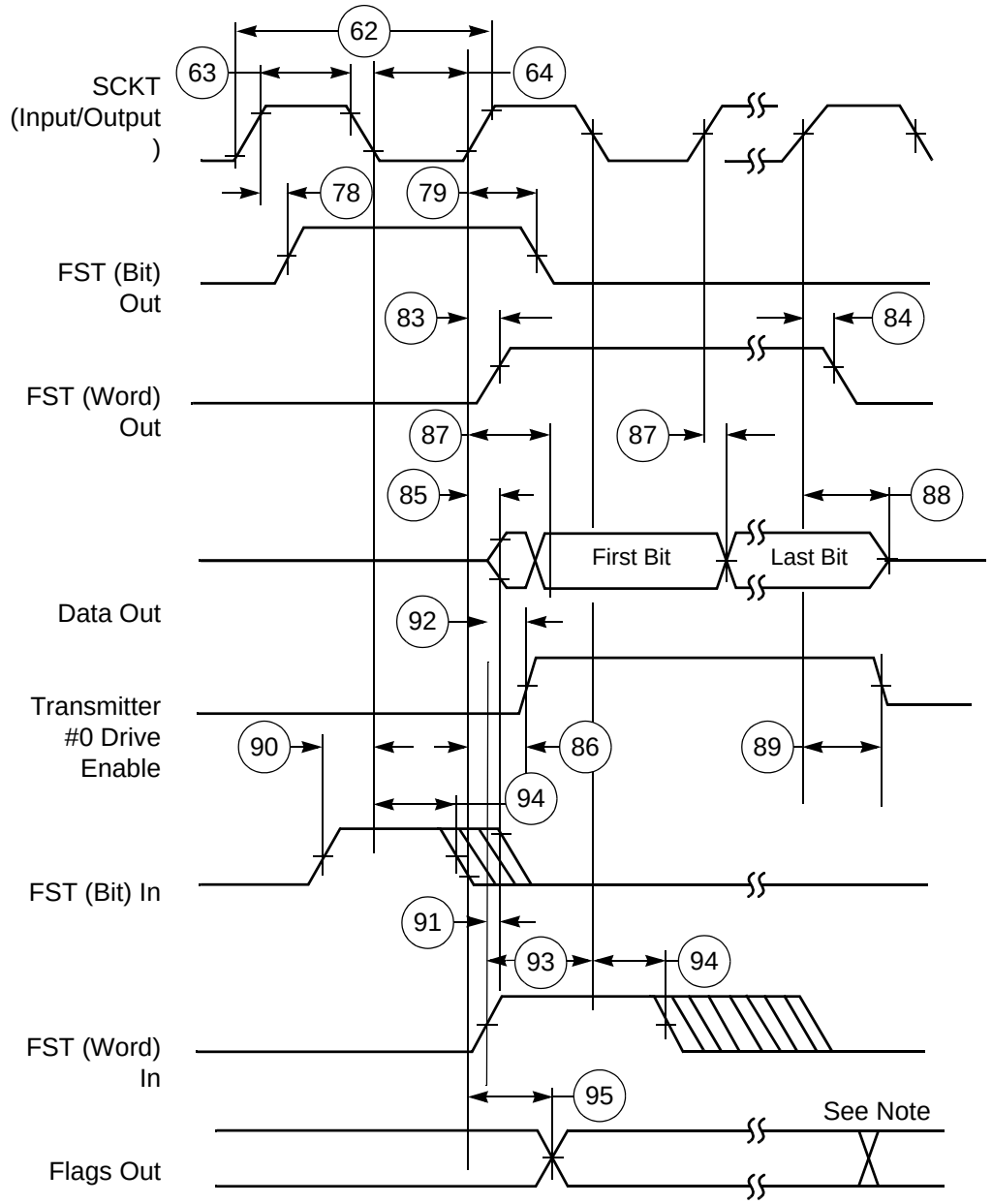
Table 22. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit
78	SCKT rising edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
82	SCKT rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
84	SCKT rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
85	SCKT rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
86	SCKT rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
87	SCKT rising edge to data out valid	—	—	— —	26.5 21.0	x ck i ck	ns
88	SCKT rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns
89	SCKT rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
90	FST input (bl, wr) setup time before SCKT falling edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns
91	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
92	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	ns
93	FST input (wl) setup time before SCKT falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
94	FST input hold time after SCKT falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
95	Flag output valid after SCKT rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
96	HCKR/HCKT clock cycle	—	$2 \times T_C$	40.0	—		ns
97	HCKT input rising edge to SCKT output	—	—	—	18.0		ns
98	HCKR input rising edge to SCKR output	—	—	—	18.0		ns

Table 22. Enhanced Serial Audio Interface Timing (Continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression[3]	Min	Max	Condition[4]	Unit

Notes:
1. V_{CORE_VDD} = 1.25 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (asynchronous implies that SCKT and SCKR are two different clocks)
   i ck s = internal clock, synchronous mode
   (synchronous implies that SCKT and SCKR are the same clock)
3. bl = bit length
   wl = word length
   wr = word length relative
4. SCKT(SCKT pin) = transmit clock
   SCKR(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high frequency clock
   HCKR(HCKR pin) = receive high frequency clock
5. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested
8. ESAI_1 specs match those of ESAI_0



Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

Figure 14. **ESAI Transmitter Timing**

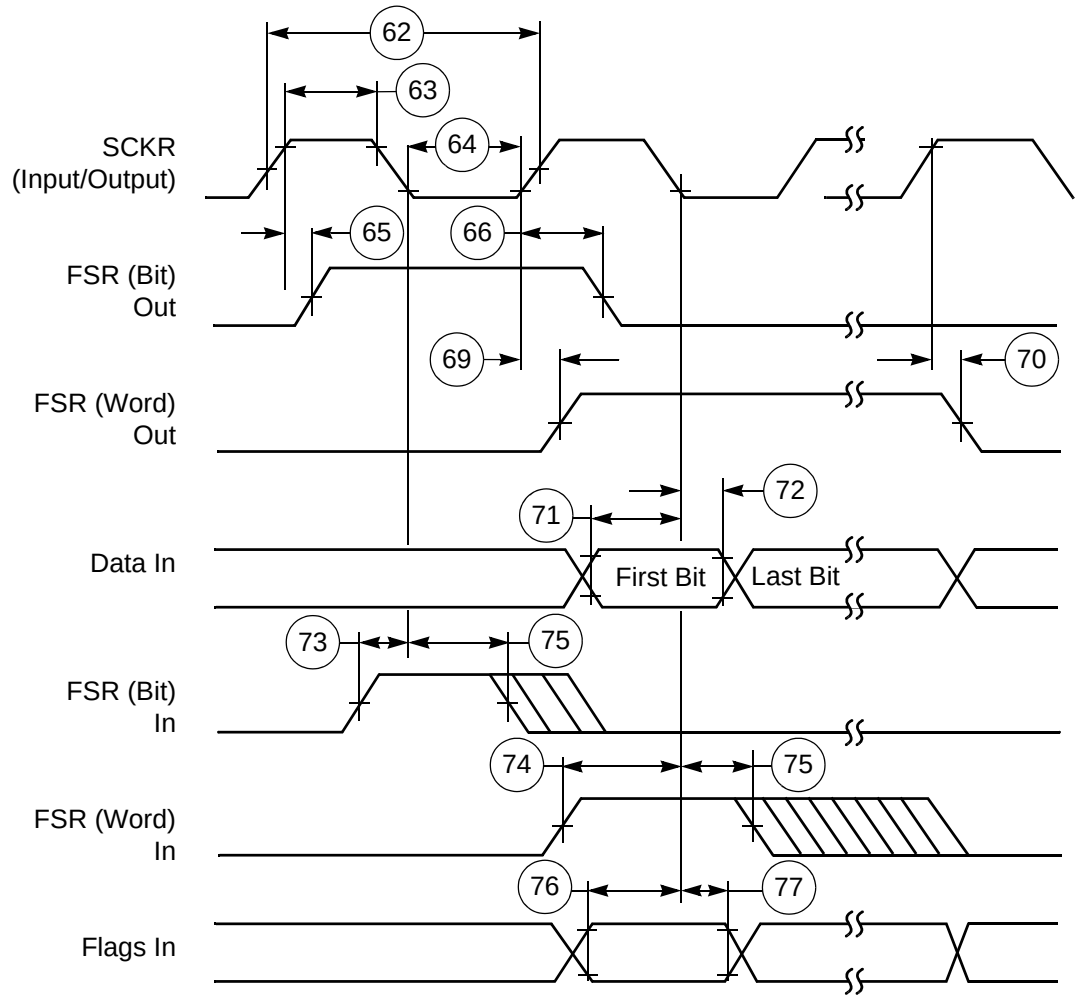


Figure 15. **ESAI Receiver Timing**

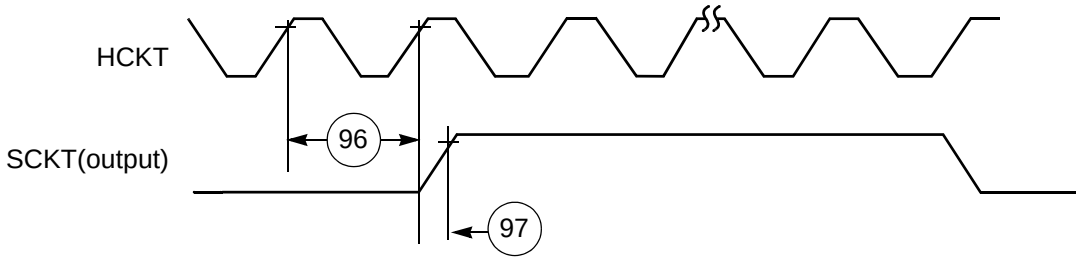


Figure 16. **ESAI HCKT Timing**

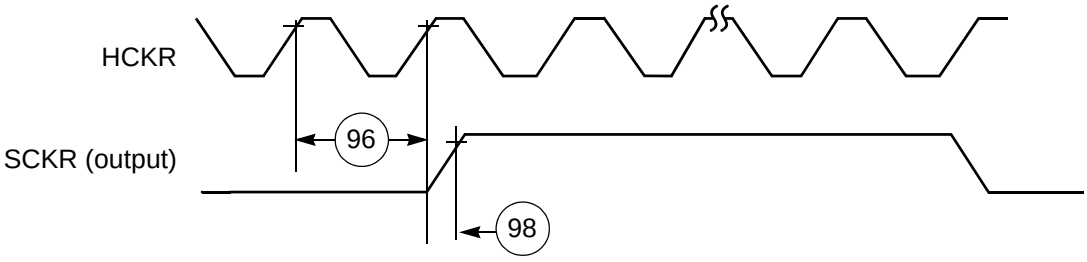


Figure 17. **ESAI HCKR Timing**

15 Digital Audio Transmitter Timing

Table 23. Digital Audio Transmitter Timing

No.	Characteristic	Expression	181 MHz		Unit
			Min	Max	
99	ACI frequency (see note)	$1 / (2 \times T_C)$	—	90	MHz
100	ACI period	$2 \times T_C$	11.1	—	ns
101	ACI high duration	$0.5 \times T_C$	2.8	—	ns
102	ACI low duration	$0.5 \times T_C$	2.8	—	ns
103	ACI rising edge to ADO valid	$1.5 \times T_C$	—	8.3	ns

Note: 1. In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of theDSP56371 internal clock frequency. For example, if the DSP56371 is running at 181 MHz internally, the ACI frequency should be less than 90MHz.

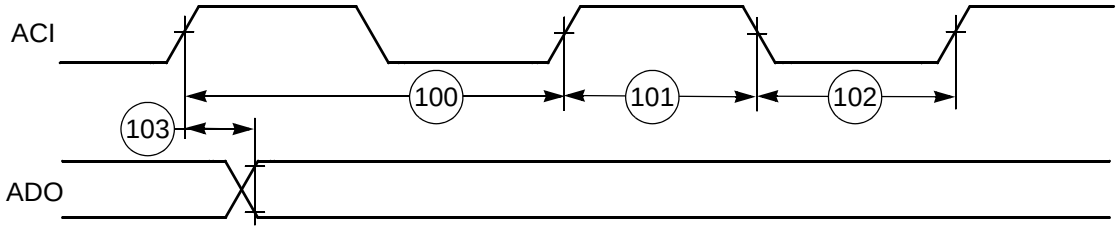


Figure 18. **Digital Audio Transmitter Timing**

16 Timer Timing

Table 24. Timer Timing

No.	Characteristics	Expression	181 MHz		Unit
			Min	Max	
104	TIO Low	$2 \times T_C + 2.0$	13	—	ns
105	TIO High	$2 \times T_C + 2.0$	13	—	ns

Note: 1. $V_{CORE\_VDD} = 1.25\ V \pm 0.05$ V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF

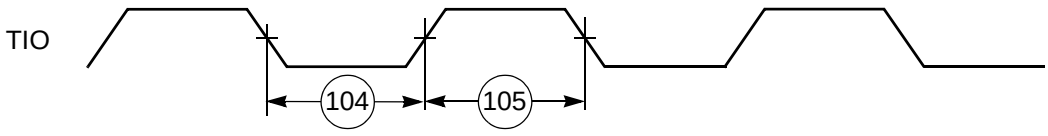


Figure 19. **TIO Timer Event Input Restrictions**

17 GPIO Timing

Table 25. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
106	FOSC edge to GPIO out valid (GPIO out delay time)		—	7	ns
107	FOSC edge to GPIO out not valid (GPIO out hold time)		----	7	ns
108	FOSC In valid to EXTAL edge (GPIO in set-up time)		2	---	ns
109	FOSC edge to GPIO in not valid (GPIO in hold time)		0	---	ns
110	Minimum GPIO pulse high width (except Port F)	2 x T_C	11.1	—	ns
111	Minimum GPIO pulse low width (except Port F)	2 x T_C	11.1		ns
112	Minimum GPIO pulse low width (Port F)	6 x T_C	33.3		ns
113	Minimum GPIO pulse high width (Port F)	6 x T_C	33.3		ns
114	GPIO out rise time	—	—	13	ns
115	GPIO out fall time	—	—	13	ns

Note: 1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF

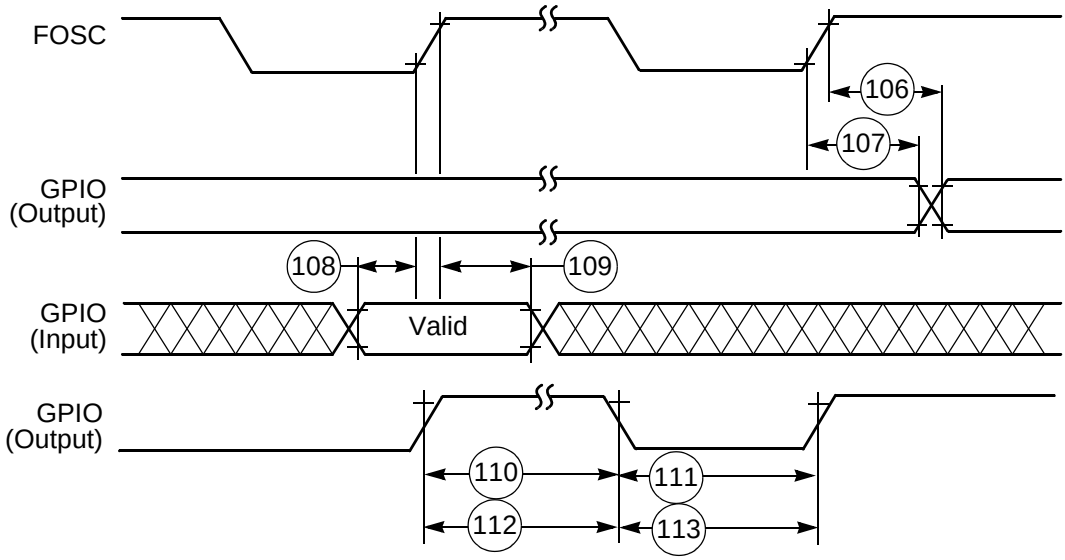


Figure 20. **GPIO Timing**

18 JTAG Timing

Table 26. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
116	TCK frequency of operation (1/($T_C \times 6$); maximum 22 MHz)	0.0	22.0	MHz
117	TCK cycle time	45.0	—	ns
118	TCK clock pulse width	20.0	—	ns
119	TCK rise and fall times	0.0	10.0	ns
120	TCK low to output data valid	0.0	40.0	ns
121	TCK low to output high impedance	0.0	40.0	ns
122	TMS, TDI data setup time	5.0	—	ns
123	TMS, TDI data hold time	25.0	—	ns
124	TCK low to TDO data valid	0.0	44.0	ns
125	TCK low to TDO high impedance	0.0	44.0	ns

Note: 1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

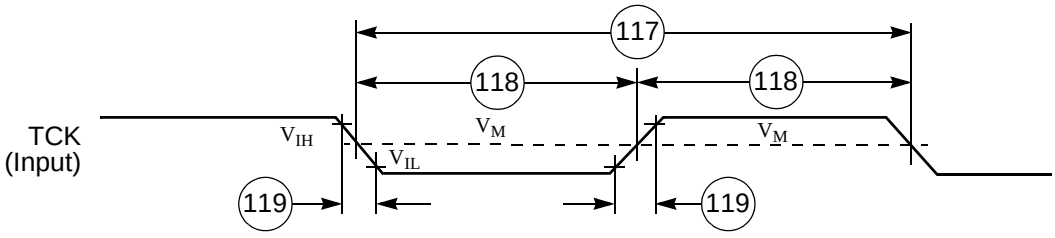


Figure 21. **Test Clock Input Timing Diagram**

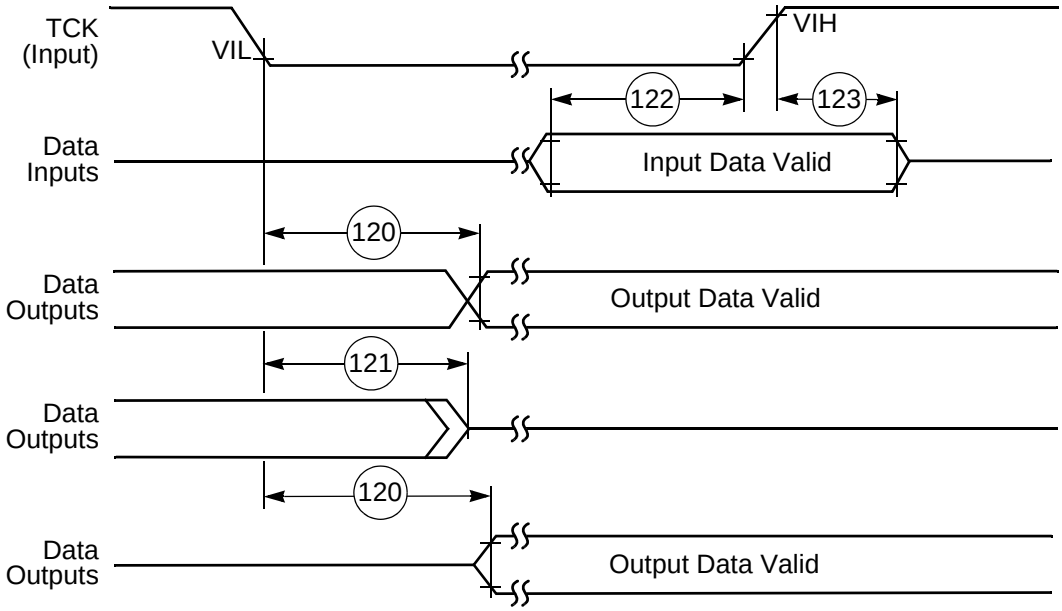


Figure 22. **Debugger Port Timing Diagram**

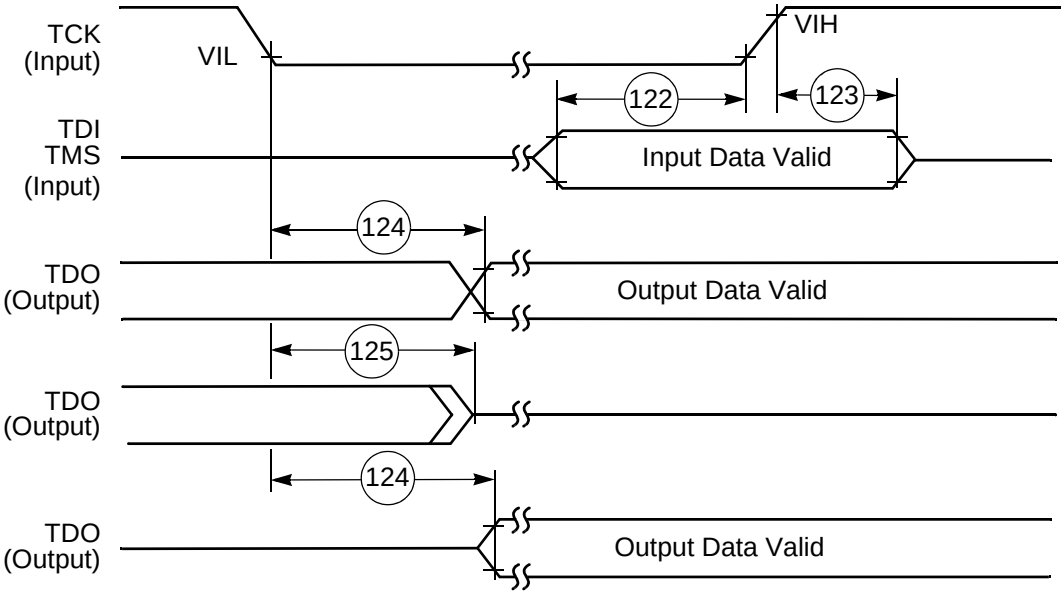


Figure 23. **Test Access Port Timing Diagram**

19 Package Information

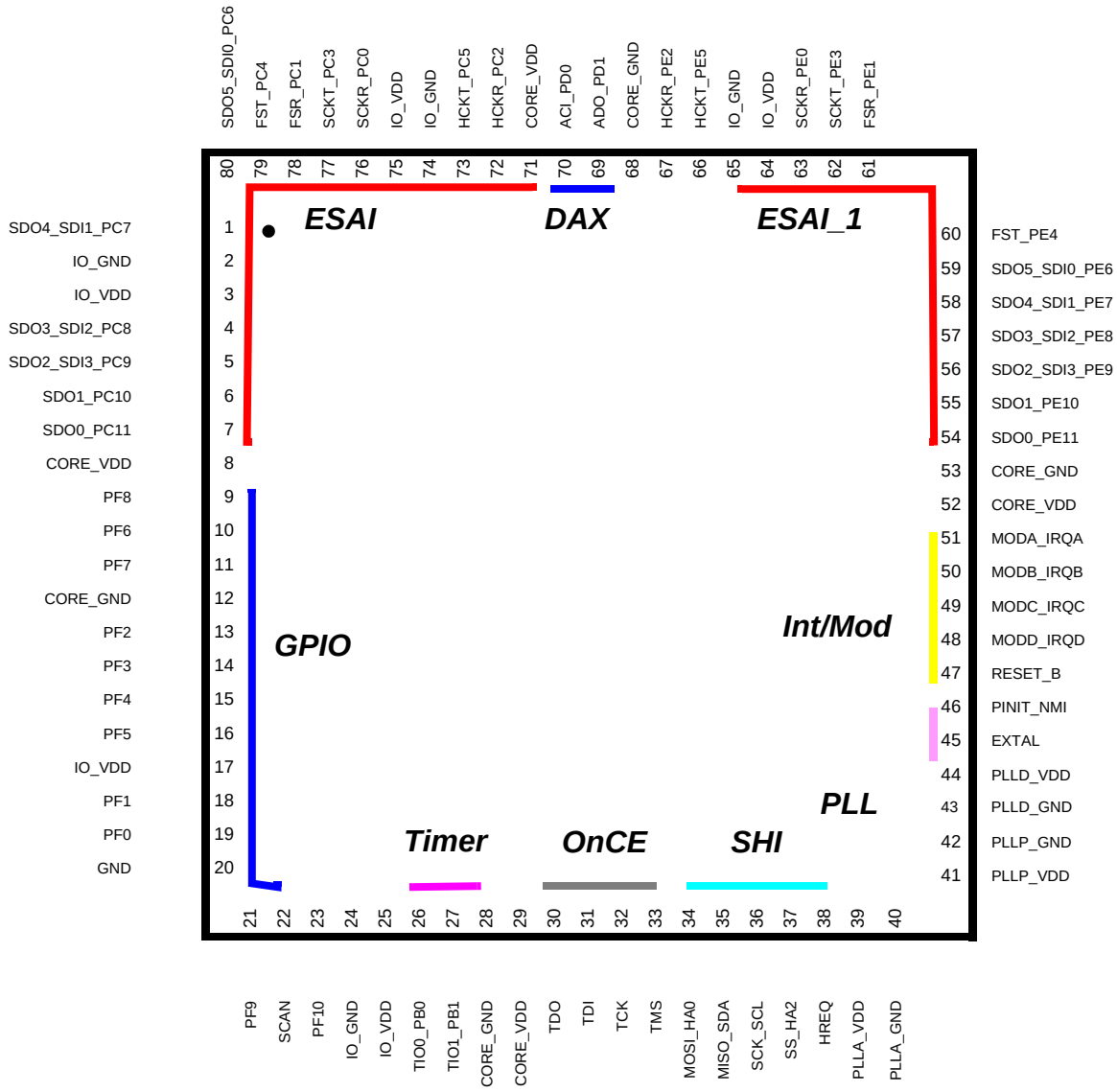


Figure 24. **DSP56371 Pinout**

Table 27. Signal Identification by Pin Number

Pin No.	Signal Name	Pin No	Signal Name	Pin No	Signal Name	Pin No	Signal Name
1	SDO4_SDI1_PC7	21	PF9	41	PLLP_VDD	61	FSR_PE1
2	IO_GND	22	SCAN	42	PLLP_GND	62	SCKT_PE3
3	IO_VDD	23	PF10	43	PLLD_GND	63	SCKR_PE0
4	SDO3_SDI2_PC8	24	IO_GND	44	PLLD_VDD	64	IO_VDD
5	SDO2_SDI3_PC9	25	IO_VDD	45	EXTAL	65	IO_GND
6	SDO1_PC10	26	TI0_PB0	46	PINIT_NMI	66	HCKT_PE5
7	SDO0_PC11	27	TI0_PB1	47	RESET_B	67	HCKR_PE2
8	CORE_VDD	28	CORE_GND	48	MODD_IRQD	68	CORE_GND
9	PF8	29	CORE_VDD	49	MODC_IRQC	69	ADO_PD1
10	PF6	30	TDO	50	MODB_IRQB	70	ADI_PD0
11	PF7	31	TDI	51	MODA_IRQA	71	CORE_VDD
12	CORE_GND	32	TCK	52	CORE_VDD	72	HCKR_PC2
13	PF2	33	TMS	53	CORE_GND	73	HCKT2_PC5
14	PF3	34	MOSI_HA0	54	SDO0_PE11	74	IO_GND
15	PF4	35	MISO_SDA	55	SDO1_PE10	75	IO_VDD
16	PF5	36	SCK_SCL	56	SDO2_SDI3_PE9	76	SCKR_PC0
17	IO_VDD	37	SS_HA2	57	SDO3_SDI2_PE8	77	SCKT_PC3
18	PF1	38	HREQ	58	SDO4_SDI1_PE7	78	FSR_PC1
19	PF0	39	PLLA_VDD	59	SDO5_SD10_PE6	79	FST_PC4
20	GND	40	PLLA_GND	60	FST_PE4	80	SDO5_SDI10_PC6

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MECHANICAL OUTLINES DICTIONARY

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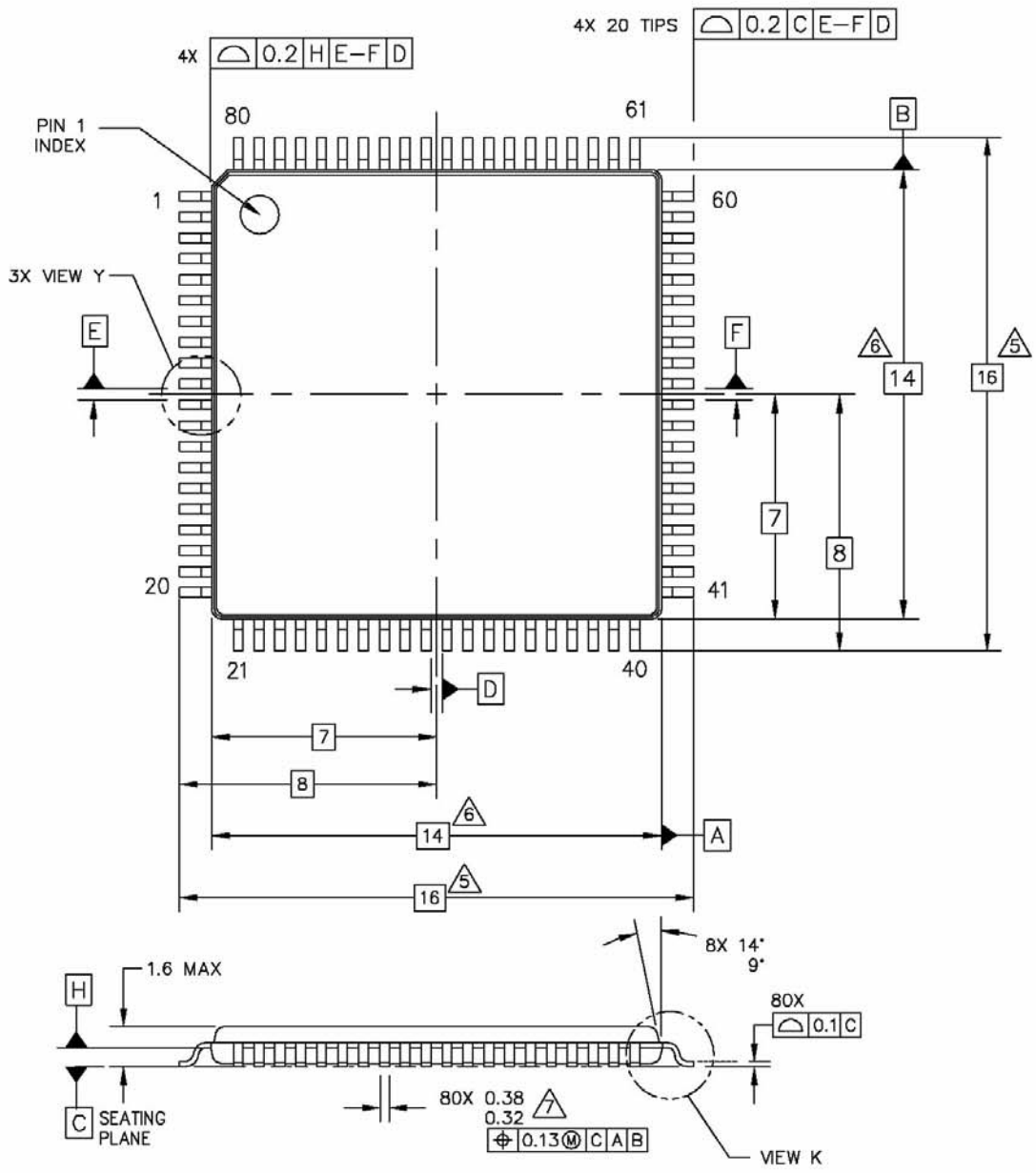

TITLE:
80 LD LQFP, 14 X 14 PKG,
0.65 MM PITCH, 1.4 THICK

CASE NUMBER: 917A–03

STANDARD: FREESCALE

PACKAGE CODE: 8258

SHEET: 1 OF 4

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	PAGE: 917A
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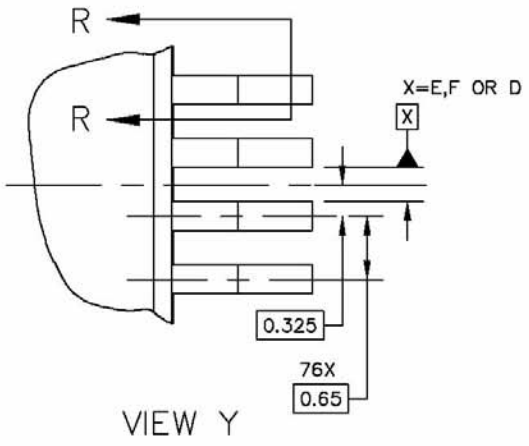

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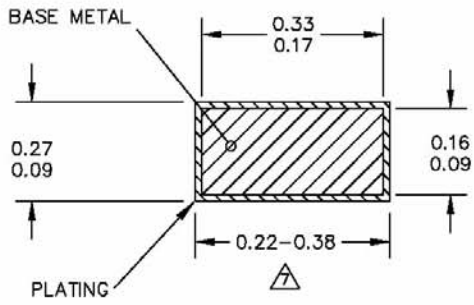

SECTION R–R
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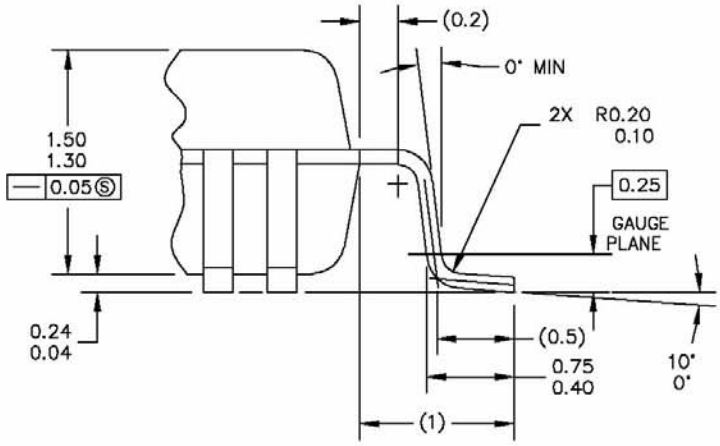

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TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 4

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		PAGE: 917A
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE:	CASE NUMBER: 917A–03	
80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

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REVISION HISTORY

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LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
0	-----	RELEASED FOR PRODUCTION	-----	-----
A	-----	-----	-----	-----
B	-----	-----	-----	-----
C	-----	-----	-----	-----
D	GARY JOHNSON	REFORMAT DOCUMENT. DELETED DUAL DIMENSIONS (INCH). CHANGED DOCUMENT TITLE FROM TQFP TO LQFP.	AZHAR A.	11 MAR 2004
E	PATRICE L.	UPDATED DRAWINGS PER FREESCALE FORMAT.	KL CHIN	7 OCT 2004

TITLE:
80 LQFP, 14 X 14 PKG,
0.65 MM PITCH, 1.4 THICK

CASE NUMBER: 917A-03
STANDARD: FREESCALE
PACKAGE CODE: 8258
SHEET: 4 OF 4

20 Design Considerations

20.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where: T_A = ambient temperature °C
R_{qJA} = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where: $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation
  $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

20.2 Electrical Design Considerations

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 k ohm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Route the DVDD pin carefully to minimize noise.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56371 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 3.3 V tolerant pins and the chip V_{CC} never exceeds a 3.00 V.

20.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

Power Consumption Example

For a GPIO address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 150 MHz clock, toggling at its maximum possible rate (75 MHz), the current consumption is

$$I = 50x10^{-12}x3.3x75x10^{6} = 12.375mA$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$$

where :I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

21 Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation.

```
;*********************************;*******************************

;* ;* CHECKS Typical Power Consumption
;*****************************************************************

ORG P:$000800
move #$000000,r1
move #$000000,r0
do #1024,ldmem
move r1,p:(r0)
move r1,y:(r0)+
ldmem nop



move #0,b1

;jmp $FF2AE0
;org P:$FF2AE0
move b1,y:>$100
```

```
move #$FF,B
move #>$AF080,X0
move #>$FF2AD6,r0
move #$0,r1
dor #6,loop1

move p:(r0)+,x1
move x0,p:(r1)+
move x1,p:(r1)+
nop
loop1
move #$0,vba
move #$0,sp
move #$0,sc
reset
move #$FFFFFF,m0
move m0,m1
move m0,m2
move m0,m3
move m0,m4
move m0,m5
move m0,m6
move m0,m7
move #>$102,ep
move #>$18,sz
move #>$110000,omr
move #$300,sr
movep #>$F02000,X:$FFFFFF
movep #$187,X:$FFFFFE
;then sets up BCR and AAR registers
;then sets up PORTB and HDI08 PORT
andi #$FC,mr
;start running ROM intialisation stage
;jsr $FF1C7E
; Set green HLX zone table
jsr $FF1D64
; Run GPIONil function
jsr $FF2F82
; Initialise Green HLX
jsr $FF1FA1
; Disable DAX
move #>$15F,x1
move x1,P:$FF0D7F
; Run Green HLX
jmp $FF1FDB

nop
nop
nop
nop
nop
nop
```

```
dor forever,endprog
nop
nop
endprog nop
```

22 IBIS Model

[IBIS ver] 2.1

[File name] tpz013g3.ibs

[File Rev] 1.0

[Date] 07/30/2002

[Source] Made By 0.13uu HSPICE model.

[Disclaimer] This information is for modeling purposes only and is not guaranteed.

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|***

| Component tpz013g3

|***

(Pin)	signal_name	model_name
1	SDO4_SDI1_PC7	PRD12DGZ
2	IO_GND	PVSS3DGZ
3	IO_VDD	PVDD2DGZ
4	SDO3_SDI2_PC8	PRD12DGZ
5	SDO2_SDI3_PC9	PRD12DGZ
6	SDO1_PC10	PRD12DGZ
7	SDO0_PC11	PRD12DGZ
8	CORE_VDD	PVDD1DGZ
9	PF8	PRD12DGZ
10	PF6	PRD12DGZ
11	PF7	PRD12DGZ
12	CORE_GND	PVSS3DGZ
13	PF2	PRD12DGZ
14	PF3	PRD12DGZ
15	PF4	PRD12DGZ
16	PF5	PRD12DGZ
17	IO_VDD	PVDD2DGZ
18	PF1	PRD12DGZ
19	PF0	PRD12DGZ

20	GND	PVSS2DGZ
21	PF9	PRD12DGZ
22	SCAN	PDDDGZ
23	PF10	PRD12DGZ
24	IO_GND	PVSS3DGZ
25	IO_VDD	PVDD2DGZ
26	TI0_PB0	PVDD2DGZ
27	TI1_PB1	PVDD2DGZ
28	CORE_GND	PVSS3DGZ
29	CORE_VDD	PVDD1DGZ
30	TDO	PRT24DGZ
31	TDI	PDUDGZ
32	TCK	PDUDGZ
33	TMS	PDUDGZ
34	MOSI_HA0	PRD12DGZ
35	MISO_SDA	PRD12DGZ
36	SCK_SCL	PRD16DGZ
37	SS_HA2	PDUSDGZ
38	HREQ	PRD12DGZ
39	PLLA_VDD	PVDD1P
40	PLLA_GND	PVSS1P
41	PLLP_VDD	PVDD2DGZ
42	PLLP_GND	PVSS2P
43	PLLD_GND	PVSS1P
44a	PLLD_VDD	PVDD1PC
44b	PLLD_VDD	PVDD1DGZ
45	EXTAL	PDIDGZ
46	PINIT_NMI	PDUSDGZ
47	RESET_B	PDUSDGZ
48	MODD_IRQD	PDUSDGZ
49	MODC_IRQC	PDUSDGZ
50	MODB_IRQB	PDUSDGZ
51	MODA_IRQA	PDUSDGZ

52	CORE_VDD	PVDD1DGZ
53	CORE_GND	PVSS3DGZ
54	SDO0_PE11	PRD12DGZ
55	SDO1_PE10	PRD12DGZ
56	SDO2_SDI3_PE9	PRD12DGZ
57	SDO3_SDI2_PE8	PRD12DGZ
58	SDO4_SDI1_PE7	PRD12DGZ
59	SDO5_SDI0_PE6	PRD12DGZ
60	FST_PE4	PRD12DGZ
61	FSR_PE1	PRD12DGZ
62	SCKT_PE4	PRD12DGZ
63	SCKR_PE0	PRD12DGZ
64	IO_VDD	PVDD2DGZ
65	IO_GND	PVSS3DGZ
66	HCKT_PE5	PRD12DGZ
67	HCKR_PE2	PRD12DGZ
68	CORE_GND	PVSS3DGZ
69	ADO_PD1	PRD24DGZ
70	ADI_PD2	PRD24DGZ
71	CORE_VDD	PVDD1DGZ
72	HCKR_PC2	PRD12DGZ
73	HCKT_PC5	PRD12DGZ
74	IO_GND	PVSS3DGZ
75	IO_VDD	PVDD2DGZ
76	SCKR_PC0	PRD12DGZ
77	SCKT_PC4	PRD12DGZ
78	FSR_PC1	PRD12DGZ
79	FST_PC4	PRD12DGZ
80	SDO5_SDI0_PC6	PRD12DGZ

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|*****************************************************************************
|                        Model prd12dgz
|*****************************************************************************
|
```

[Model] prd12dgz

Model_type I/O

Polarity Non-Inverting

Enable Active-Low

Vinl = 0.80V

Vinh = 2.00V

Vmeas = 1.50V
Cref = 50.00pF
Rref = 1.00M
Vref = 0.000V

C_comp	4.17pF	3.75pF	4.58pF
|			
|			
[Temperature Range]	25.00	0.12k	0.000
[Pullup Reference]	3.30V	3.00V	3.60V
[Pulldown Reference]	0.000V	0.000V	0.000V
[POWER Clamp Reference]	5.00V	4.50V	5.50V
[GND Clamp Reference]	0.000V	0.000V	0.000V

[Pulldown]

| voltage	I(typ)	I(min)	I(max)
|			
-3.30	0.000A	0.000A	0.000A
-3.10	0.000A	0.000A	-10.00mA
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	-10.00mA	0.000A
-2.30	-10.00mA	0.000A	-10.00mA
-2.10	0.000A	-10.00mA	0.000A
-1.90	0.000A	0.000A	-10.00mA
-1.70	0.000A	0.000A	-10.00mA
-1.50	-10.00mA	0.000A	-10.00mA
-1.00	-11.00mA	-5.00mA	-13.00mA
-0.90	-12.00mA	-5.00mA	-15.00mA
-0.80	-24.00mA	-7.00mA	-32.51mA
-0.70	-29.14mA	-8.00mA	-32.35mA
-0.60	-26.47mA	-13.80mA	-29.35mA
-0.50	-22.61mA	-14.54mA	-25.54mA
-0.40	-18.32mA	-12.17mA	-20.93mA
-0.30	-13.87mA	-9.16mA	-15.91mA
-0.20	-9.33mA	-6.10mA	-10.74mA
-0.10	-4.70mA	-3.05mA	-5.43mA
-0.00	2.86nA	7.25nA	11.72nA
0.10	4.61mA	2.94mA	5.36mA
0.20	8.96mA	5.69mA	10.49mA
0.30	13.07mA	8.26mA	15.36mA
0.40	16.92mA	10.65mA	20.00mA
0.50	20.53mA	12.86mA	24.40mA
0.60	23.91mA	14.90mA	28.55mA

0.70	27.04mA	16.76mA	32.48mA
0.80	29.95mA	18.46mA	36.18mA
0.90	32.61mA	19.99mA	39.64mA
1.00	35.06mA	21.37mA	42.87mA
1.10	37.27mA	22.58mA	45.87mA
1.20	39.27mA	23.64mA	48.64mA
1.30	41.04mA	24.55mA	51.19mA
1.40	42.60mA	25.32mA	53.50mA
1.50	43.95mA	25.95mA	55.60mA
1.60	45.08mA	26.44mA	57.46mA
1.70	46.00mA	26.80mA	59.11mA
1.80	46.70mA	27.07mA	60.53mA
1.90	47.20mA	27.26mA	61.71mA
2.00	47.55mA	27.41mA	62.63mA
2.10	47.81mA	27.53mA	63.31mA
2.20	48.01mA	27.63mA	63.79mA
2.30	48.17mA	27.71mA	64.15mA
2.40	48.31mA	27.78mA	64.43mA
2.50	48.42mA	27.85mA	64.65mA
2.60	48.53mA	27.90mA	64.84mA
2.70	48.62mA	27.96mA	65.00mA
2.80	48.70mA	28.01mA	65.14mA
2.90	48.78mA	28.05mA	65.27mA
3.00	48.85mA	28.09mA	65.38mA
3.10	48.92mA	28.14mA	65.49mA
3.20	48.99mA	28.18mA	65.59mA
3.30	49.05mA	28.23mA	65.68mA
3.40	49.12mA	28.42mA	65.77mA
3.50	49.20mA	28.97mA	65.86mA
3.60	49.24mA	29.74mA	65.95mA
3.70	49.31mA	30.57mA	66.04mA
3.80	49.40mA	31.13mA	66.12mA
3.90	49.61mA	28.60mA	66.22mA
4.00	50.41mA	28.66mA	66.33mA
4.10	51.65mA	28.72mA	66.49mA
4.20	52.87mA	28.80mA	66.72mA
4.30	50.78mA	28.89mA	67.28mA
4.50	50.67mA	29.12mA	70.40mA
4.70	51.17mA	29.42mA	73.03mA
4.90	51.85mA	29.83mA	69.12mA
5.10	52.75mA	30.37mA	70.18mA
5.30	53.86mA	31.02mA	71.45mA
5.50	55.21mA	31.82mA	73.05mA
5.70	56.82mA	32.77mA	74.98mA
5.90	58.68mA	33.86mA	77.25mA
6.10	60.78mA	35.10mA	79.83mA
6.60	66.91mA	38.73mA	87.50mA

|

[Pullup]

| voltage | I(typ) | I(min) | I(max)

|

-3.30	0.11A	82.01mA	0.13A
-3.10	0.11A	79.25mA	0.13A
-2.90	0.10A	76.07mA	0.12A
-2.70	97.60mA	72.55mA	0.11A
-2.50	92.41mA	68.70mA	0.11A
-2.30	87.04mA	64.55mA	0.10A
-2.10	81.44mA	60.13mA	94.69mA
-1.90	75.56mA	55.45mA	87.72mA
-1.70	69.36mA	50.52mA	80.48mA
-1.50	62.83mA	45.36mA	73.03mA
-1.00	48.46mA	31.37mA	56.75mA
-0.90	43.82mA	28.63mA	50.74mA
-0.80	38.59mA	28.69mA	44.61mA
-0.70	33.28mA	24.97mA	38.60mA
-0.60	28.26mA	21.04mA	33.20mA
-0.50	23.64mA	17.11mA	27.91mA
-0.40	19.01mA	13.34mA	22.52mA
-0.30	14.32mA	9.87mA	17.03mA
-0.20	9.58mA	6.53mA	11.45mA
-0.10	4.80mA	3.23mA	5.78mA
0.00	34.08uA	11.20uA	71.92uA
0.10	-4.58mA	-3.08mA	-5.50mA
0.20	-8.94mA	-5.98mA	-10.80mA
0.30	-13.04mA	-8.72mA	-15.82mA
0.40	-16.89mA	-11.27mA	-20.56mA
0.50	-20.50mA	-13.66mA	-25.04mA
0.60	-23.86mA	-15.87mA	-29.25mA
0.70	-26.98mA	-17.92mA	-33.21mA
0.80	-29.87mA	-19.80mA	-36.91mA
0.90	-32.53mA	-21.51mA	-40.36mA
1.00	-34.96mA	-23.06mA	-43.56mA
1.10	-37.16mA	-24.45mA	-46.52mA
1.20	-39.15mA	-25.68mA	-49.24mA
1.30	-40.92mA	-26.75mA	-51.73mA
1.40	-42.48mA	-27.66mA	-53.98mA
1.50	-43.83mA	-28.43mA	-56.01mA
1.60	-44.98mA	-29.05mA	-57.81mA
1.70	-45.94mA	-29.53mA	-59.40mA
1.80	-46.72mA	-29.90mA	-60.77mA
1.90	-47.35mA	-30.20mA	-61.93mA
2.00	-47.86mA	-30.45mA	-62.90mA
2.10	-48.29mA	-30.66mA	-63.70mA
2.20	-48.65mA	-30.85mA	-64.37mA
2.30	-48.97mA	-31.02mA	-64.93mA
2.40	-49.25mA	-31.17mA	-65.40mA
2.50	-49.50mA	-31.31mA	-65.82mA
2.60	-49.72mA	-31.44mA	-66.18mA
2.70	-49.92mA	-31.56mA	-66.50mA
2.80	-50.11mA	-31.67mA	-66.79mA
2.90	-50.28mA	-31.78mA	-67.05mA
3.00	-50.44mA	-31.88mA	-67.29mA

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  3.10          -50.59mA      -31.98mA      -67.51mA
  3.20          -50.74mA      -32.08mA      -67.72mA
  3.30          -50.88mA      -32.20mA      -67.92mA
  3.40          -51.01mA      -32.75mA      -68.11mA
  3.50          -51.14mA      -40.35mA      -68.29mA
  3.60          -51.27mA      -0.14A        -68.47mA
  3.70          -51.42mA      -0.94A        -68.64mA
  3.80          -51.84mA      -2.69A        -68.80mA
  3.90          -53.78mA      -4.48A        -68.97mA
  4.00          -64.80mA      -6.27A        -69.30mA
  4.10          -0.29A        -8.06A        -70.82mA
  4.20          -1.85A        -9.85A        -75.29mA
  4.30          -3.90A        -11.63A       -83.12mA
  4.50          -8.00A        -15.21A       -1.14A
  4.70          -12.10A       -18.79A       -5.39A
  4.90          -16.20A       -22.36A       -9.64A
  5.10          -20.30A       -25.94A       -13.89A
  5.30          -24.40A       -29.51A       -18.15A
  5.50          -28.50A       -33.09A       -22.41A
  5.70          -32.60A       -36.67A       -26.66A
  5.90          -36.70A       -40.24A       -30.92A
  6.10          -40.80A       -43.82A       -35.17A
  6.60          -51.05A       -52.76A       -45.81A
|
[GND_clamp]
| voltage       I(typ)        I(min)        I(max)
|
  -5.00         -85.83A       -77.78A       -88.32A
  -4.80         -81.73A       -74.20A       -84.06A
  -4.60         -77.63A       -70.62A       -79.80A
  -4.40         -73.53A       -67.04A       -75.54A
  -4.20         -69.43A       -63.46A       -71.28A
  -4.00         -65.33A       -59.88A       -67.02A
  -3.80         -61.23A       -56.30A       -62.76A
  -3.60         -57.13A       -52.72A       -58.50A
  -3.40         -53.03A       -49.14A       -54.24A
  -3.20         -48.93A       -45.56A       -49.98A
  -3.00         -44.84A       -41.99A       -45.73A
  -2.80         -40.74A       -38.42A       -41.48A
  -2.60         -36.64A       -34.84A       -37.22A
  -2.40         -32.54A       -31.27A       -32.97A
  -2.20         -28.45A       -27.69A       -28.72A
  -2.00         -24.35A       -24.12A       -24.46A
  -1.80         -20.25A       -20.54A       -20.21A
  -1.60         -16.15A       -16.97A       -15.95A
  -1.40         -12.05A       -13.39A       -11.70A
  -1.20         -7.95A        -9.82A        -7.44A
  -1.00         -3.85A        -6.24A        -3.19A
  -0.80         -0.23A        -2.66A        -70.99mA
  -0.60         -2.25mA       -0.10A        -5.98mA
  -0.40         -89.81uA      -0.52mA       -0.26mA
```

-0.20	-27.92uA	-14.70uA	-42.92uA
-0.00	-87.63nA	-89.05nA	-0.10uA
0.20	18.71uA	7.31uA	32.27uA
0.40	29.19uA	10.25uA	54.12uA
0.60	32.49uA	10.67uA	65.78uA
0.80	33.07uA	10.78uA	69.33uA
1.00	33.30uA	10.86uA	70.17uA
1.20	33.45uA	10.92uA	70.55uA
1.40	33.57uA	10.97uA	70.80uA
1.60	33.68uA	11.02uA	70.99uA
1.80	33.77uA	11.07uA	71.16uA
2.00	33.87uA	11.11uA	71.32uA
2.20	33.96uA	11.14uA	71.46uA
2.40	34.01uA	11.15uA	71.61uA
2.60	34.03uA	11.16uA	71.76uA
2.80	34.05uA	11.17uA	71.84uA
3.00	34.06uA	11.19uA	71.86uA
3.20	34.07uA	11.51uA	71.88uA
3.40	34.07uA	10.95uA	71.90uA
3.60	34.07uA	10.39uA	71.92uA
3.80	34.07uA	9.83uA	71.94uA
4.00	34.07uA	9.27uA	71.96uA
4.20	34.07uA	8.71uA	71.98uA
4.40	34.07uA	8.15uA	72.00uA
4.60	34.07uA	7.59uA	72.02uA
4.80	34.07uA	7.03uA	72.04uA
5.00	34.07uA	6.47uA	72.06uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	48.57uA	16.33uA	95.57uA
-4.90	48.24uA	16.21uA	95.07uA
-4.80	47.91uA	16.09uA	94.57uA
-4.70	47.58uA	15.97uA	94.07uA
-4.60	47.25uA	15.85uA	93.57uA
-4.50	46.92uA	15.73uA	93.07uA
-4.40	46.59uA	15.61uA	92.57uA
-4.30	46.26uA	15.49uA	92.07uA
-4.20	45.93uA	15.37uA	91.57uA
-4.10	45.60uA	15.25uA	91.07uA
-4.00	45.27uA	15.13uA	90.57uA
-3.90	44.94uA	15.01uA	90.07uA
-3.80	4.61uA	14.89uA	89.57uA
-3.70	44.28uA	14.77uA	89.07uA
-3.60	43.95uA	14.65uA	88.57uA
-3.50	43.62uA	14.53uA	88.07uA
-3.40	43.29uA	14.41uA	87.57uA
-3.30	42.96uA	14.29uA	87.07uA
-3.20	42.63uA	14.17uA	86.57uA
-3.10	42.30uA	14.05uA	86.07uA

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  -3.00         41.97uA         13.93uA         85.57uA
  -2.90         41.64uA         13.81uA         85.07uA
  -2.80         41.31uA         13.69uA         84.57uA
  -2.70         40.98uA         13.57uA         84.07uA
  -2.60         40.65uA         13.45uA         83.57uA
  -2.50         40.32uA         13.33uA         83.07uA
  -2.40         39.99uA         13.21uA         82.57uA
  -2.30         39.66uA         13.09uA         82.07uA
  -2.20         39.33uA         12.97uA         81.57uA
  -2.10         39.00uA         12.85uA         81.07uA
  -2.00         38.67uA         12.73uA         80.57uA
  -1.90         38.34uA         12.61uA         80.07uA
  -1.80         38.01uA         12.49uA         79.57uA
  -1.70         37.68uA         12.37uA         79.07uA
  -1.60         37.35uA         12.25uA         78.57uA
  -1.50         37.02uA         12.15uA         78.07uA
  -1.40         36.71uA         12.05uA         77.57uA
  -1.30         36.42uA         11.95uA         77.07uA
  -1.20         36.15uA         11.87uA         76.57uA
  -1.10         35.89uA         11.79uA         76.07uA
  -1.00         35.66uA         11.72uA         75.57uA
  -0.90         35.45uA         11.66uA         75.10uA
  -0.80         35.26uA         11.60uA         74.67uA
  -0.70         35.09uA         11.55uA         74.28uA
  -0.60         34.93uA         11.51uA         73.93uA
  -0.50         34.80uA         11.47uA         73.61uA
  0.40          34.68uA         11.43uA         73.34uA
  -0.30         34.59uA         11.41uA         73.10uA
  -0.20         34.50uA         11.38uA         72.89uA
  -0.10         34.43uA         11.36uA         72.72uA

  0.00          34.37uA         11.34uA          72.57uA
|
[Ramp]
| variable      typ             min             max
  dV/dt_r       1.21/2.06n      0.85/2.62n      1.45/1.82n
  dV/dt_f       1.22/2.51n      0.78/3.11n      1.45/2.14n
R_load = 50.00
|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F
| time          V(typ)          V(min)          V(max)
|
  0.000S        1.26uV          1.62uV          1.22uV
  0.20nS        1.04uV          1.45uV          0.74uV
  0.40nS        -5.64uV         -1.36uV         11.59uV
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0.60nS	-0.29mV	-5.13uV	-3.27mV
0.80nS	-3.54mV	25.94uV	-9.17mV
1.00nS	-3.50mV	-4.79uV	56.24mV
1.20nS	33.86mV	-0.86mV	0.13V
1.40nS	79.34mV	-3.75mV	0.19V
1.60nS	0.14V	-8.09mV	0.27V
1.80nS	0.20V	3.52mV	0.36V
2.00nS	0.28V	38.97mV	0.47V
2.20nS	0.36V	82.84mV	0.59V
2.40nS	0.47V	0.13V	0.74V
2.60nS	0.60V	0.18V	0.90V
2.80nS	0.77V	0.27V	1.12V
3.00nS	0.92V	0.34V	1.32V
3.20nS	1.03V	0.40V	1.46V
3.40nS	1.16V	0.50V	1.63V
3.60nS	1.29V	0.59V	1.78V
3.80nS	1.39V	0.67V	1.91V
4.00nS	1.49V	0.75V	2.01V
4.20nS	1.58V	0.84V	2.11V
4.40nS	1.65V	0.91V	2.18V
4.60nS	1.69V	0.95V	2.21V
4.80nS	1.72V	0.99V	2.23V
5.00nS	1.76V	1.03V	2.27V
5.20nS	1.80V	1.07V	2.29V
5.40nS	1.83V	1.12V	2.31V
5.60nS	1.86V	1.16V	2.33V
5.80nS	1.88V	1.18V	2.34V
6.00nS	1.89V	1.20V	2.34V
6.20nS	1.91V	1.23V	2.35V
6.40nS	1.92V	1.25V	2.36V
6.60nS	1.93V	1.27V	2.37V
6.80nS	1.94V	1.28V	2.38V
7.00nS	1.95V	1.30V	2.38V
7.20nS	1.96V	1.31V	2.39V
7.40nS	1.97V	1.33V	2.39V
7.60nS	1.98V	1.34V	2.39V
7.80nS	1.98V	1.35V	2.40V
8.00nS	1.98V	1.36V	2.40V
8.20nS	1.99V	1.37V	2.40V
8.40nS	1.99V	1.37V	2.40V
8.60nS	1.99V	1.38V	2.41V
8.80nS	2.00V	1.39V	2.41V
9.00nS	2.00V	1.39V	2.41V
9.20nS	2.00V	1.40V	2.41V
9.40nS	2.01V	1.40V	2.41V
9.60nS	2.01V	1.41V	2.42V
9.80nS	2.01V	1.41V	2.42V
10.00nS	2.01V	1.41V	2.42V

|

[Rising Waveform]

R_fixture = 50.00

V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	1.27V	1.66V	1.18V
0.20nS	1.27V	1.66V	1.18V
0.40nS	1.27V	1.66V	1.18V
0.60nS	1.27V	1.66V	1.19V
0.80nS	1.28V	1.66V	1.24V
1.00nS	1.40V	1.66V	1.47V
1.20nS	1.60V	1.67V	1.71V
1.40nS	1.77V	1.69V	1.88V
1.60nS	1.99V	1.80V	2.12V
1.80nS	2.24V	1.95V	2.41V
2.00nS	2.50V	2.13V	2.70V
2.20nS	2.74V	2.32V	2.99V
2.40nS	2.94V	2.49V	3.21V
2.60nS	3.09V	2.63V	3.34V
2.80nS	3.18V	2.79V	3.44V
3.00nS	3.24V	2.87V	3.49V
3.20nS	3.26V	2.91V	3.52V
3.40nS	3.27V	2.96V	3.55V
3.60nS	3.29V	2.98V	3.57V
3.80nS	3.29V	2.99V	3.59V
4.00nS	3.30V	2.99V	3.59V
4.20nS	3.30V	3.00V	3.60V
4.40nS	3.30V	3.00V	3.60V
4.60nS	3.30V	3.00V	3.60V
4.80nS	3.30V	3.00V	3.60V
5.00nS	3.30V	3.00V	3.60V
5.20nS	3.30V	3.00V	3.60V
5.40nS	3.30V	3.00V	3.60V
5.60nS	3.30V	3.00V	3.60V
5.80nS	3.30V	3.00V	3.60V
6.00nS	3.30V	3.00V	3.60V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V

8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|
[Falling Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F

Itime	V(typ)	V(min)	V(max)
0.000S	2.02V	1.44V	2.43V
0.20nS	2.02V	1.44V	2.43V
0.40nS	2.02V	1.44V	2.43V
0.60nS	2.02V	1.44V	2.38V
0.80nS	1.97V	1.44V	2.13V
1.00nS	1.73V	1.44V	1.82V
1.20nS	1.45V	1.42V	1.49V
1.40nS	1.24V	1.38V	1.24V
1.60nS	0.96V	1.29V	0.92V
1.80nS	0.70V	1.12V	0.67V
2.00nS	0.50V	0.92V	0.50V
2.20nS	0.36V	0.73V	0.38V
2.40nS	0.27V	0.55V	0.30V
2.60nS	0.20V	0.40V	0.24V
2.80nS	0.14V	0.27V	0.17V
3.00nS	99.16mV	0.20V	0.13V
3.20nS	79.41mV	0.16V	0.11V
3.40nS	53.08mV	0.11V	78.74mV
3.60nS	36.21mV	75.26mV	59.16mV
3.80nS	23.36mV	51.00mV	39.59mV
4.00nS	12.42mV	31.87mV	27.31mV
4.20nS	6.73mV	18.57mV	15.01mV
4.40nS	2.10mV	8.15mV	7.54mV
4.60nS	1.57mV	5.93mV	4.99mV
4.80nS	1.14mV	3.71mV	2.45mV
5.00nS	0.68mV	1.71mV	1.29mV
5.20nS	0.62mV	1.31mV	0.88mV
5.40nS	0.54mV	0.89mV	0.54mV
5.60nS	0.46mV	0.73mV	0.46mV
5.80nS	0.41mV	0.65mV	0.42mV
6.00nS	0.37mV	0.59mV	0.38mV
6.20nS	0.34mV	0.53mV	0.34mV
6.40nS	0.32mV	0.48mV	0.29mV
6.60nS	0.27mV	0.43mV	0.26mV

6.80nS	0.22mV	0.38mV	0.22mV
7.00nS	0.18mV	0.34mV	0.20mV
7.20nS	0.18mV	0.30mV	0.18mV
7.40nS	0.18mV	0.26mV	0.15mV
7.60nS	0.15mV	0.23mV	0.13mV
7.80nS	0.12mV	0.22mV	0.12mV
8.00nS	0.11mV	0.20mV	0.11mV
8.20nS	0.11mV	0.18mV	0.10mV
8.40nS	0.12mV	0.17mV	92.36uV
8.60nS	97.87uV	0.16mV	78.53uV
8.80nS	59.73uV	0.15mV	64.71uV
9.00nS	36.18uV	0.14mV	61.02uV
9.20nS	61.23uV	0.12mV	60.74uV
9.40nS	87.87uV	0.10mV	58.12uV
9.60nS	67.13uV	0.10mV	46.02uV
9.80nS	29.42uV	0.10mV	39.81uV
10.00nS	71.42uV	84.83uV	50.29uV

|

[Falling Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.48V
1.00nS	3.22V	3.00V	3.36V
1.20nS	3.12V	3.00V	3.25V
1.40nS	3.06V	3.00V	3.16V
1.60nS	2.96V	3.00V	3.04V
1.80nS	2.86V	2.95V	2.90V
2.00nS	2.75V	2.89V	2.76V
2.20nS	2.64V	2.83V	2.61V
2.40nS	2.52V	2.77V	2.48V
2.60nS	2.40V	2.70V	2.34V
2.80nS	2.26V	2.61V	2.18V
3.00nS	2.16V	2.54V	2.04V
3.20nS	2.10V	2.48V	1.93V
3.40nS	2.01V	2.41V	1.79V
3.60nS	1.93V	2.35V	1.68V
3.80nS	1.86V	2.30V	1.57V
4.00nS	1.78V	2.25V	1.49V
4.20nS	1.68V	2.19V	1.41V
4.40nS	1.58V	2.13V	1.34V
4.60nS	1.53V	2.10V	1.31V

```
  4.80nS      1.49V          2.08V          1.29V
  5.00nS      1.43V          2.04V          1.26V
  5.20nS      1.39V          2.01V          1.24V
  5.40nS      1.35V          1.98V          1.22V
  5.60nS      1.32V          1.95V          1.21V
  5.80nS      1.31V          1.94V          1.20V
  6.00nS      1.30V          1.93V          1.20V
  6.20nS      1.29V          1.91V          1.19V
  6.40nS      1.29V          1.90V          1.19V
  6.60nS      1.29V          1.88V          1.19V
  6.80nS      1.28V          1.87V          1.19V
  7.00nS      1.28V          1.85V          1.19V
  7.20nS      1.28V          1.84V          1.19V
  7.40nS      1.28V          1.83V          1.19V
  7.60nS      1.28V          1.82V          1.19V
  7.80nS      1.28V          1.81V          1.19V
  8.00nS      1.28V          1.81V          1.19V
  8.20nS      1.28V          1.80V          1.19V
  8.40nS      1.27V          1.79V          1.19V
  8.60nS      1.27V          1.79V          1.19V
  8.80nS      1.27V          1.78V          1.19V
  9.00nS      1.27V          1.77V          1.19V
  9.20nS      1.27V          1.76V          1.19V
  9.40nS      1.27V          1.75V          1.19V
  9.60nS      1.27V          1.73V          1.18V
  9.80nS      1.27V          1.72V          1.18V
  10.00nS     1.27V          1.71V          1.18V
|
| End [Model] prd12dgz
|
|********************************************************************************
|                          Model prd16dgz
|********************************************************************************
|
[Model]          prd16dgz
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-Low
Vinl =   0.80V
Vinh =   2.00V
Vmeas =   1.50V
Cref =  50.00pF
Rref =   1.00M
Vref =  0.000V
C_comp                          3.86pF          3.48pF          4.25pF
|
|
[Temperature Range]          25.00           0.12k           0.000
[Pullup Reference]           3.30V           3.00V           3.60V
[Pulldown Reference]         0.000V          0.000V          0.000V
[POWER Clamp Reference] 5.00V                4.50V            5.50V
```

[GND Clamp Reference] 0.000V 0.000V 0.000V
[Pulldown]
| voltage I(typ) I(min) I(max)
|

-3.30	-10.00mA	0.000A	0.000A
-3.10	0.000A	0.000A	0.000A
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	0.000A	0.000A
-2.30	0.000A	0.000A	0.000A
-2.10	-10.00mA	0.000A	0.000A
-1.90	0.000A	0.000A	-10.00mA
-1.70	-10.00mA	0.000A	-10.00mA
-1.50	-10.00mA	0.000A	-20.00mA
-1.00	-16.00mA	-6.00mA	-18.00mA
-0.90	-16.00mA	-8.00mA	-21.00mA
-0.80	-32.00mA	-8.00mA	-43.34mA
-0.70	-38.86mA	-10.60mA	-43.13mA
-0.60	-35.29mA	-18.40mA	-39.13mA
-0.50	-30.14mA	-19.39mA	-34.05mA
-0.40	-24.42mA	-16.22mA	-27.89mA
-0.30	-18.49mA	-12.22mA	-21.21mA
-0.20	-12.44mA	-8.14mA	-14.32mA
-0.10	-6.27mA	-4.06mA	-7.24mA
-0.00	4.09nA	6.98nA	10.67nA
0.10	6.14mA	3.92mA	7.15mA
0.20	11.95mA	7.59mA	13.98mA
0.30	17.42mA	11.01mA	20.48mA
0.40	22.56mA	14.20mA	26.67mA
0.50	27.38mA	17.14mA	32.53mA
0.60	31.88mA	19.86mA	38.07mA
0.70	36.06mA	22.35mA	43.31mA
0.80	39.93mA	24.61mA	48.24mA
0.90	43.49mA	26.66mA	52.85mA
1.00	46.74mA	28.49mA	57.16mA
1.10	49.69mA	30.11mA	61.16mA
1.20	52.35mA	31.52mA	64.86mA
1.30	54.72mA	32.74mA	68.25mA
1.40	56.80mA	33.76mA	71.34mA
1.50	58.59mA	34.59mA	74.13mA
1.60	60.11mA	35.25mA	76.62mA
1.70	61.33mA	35.74mA	78.81mA
1.80	62.26mA	36.09mA	80.70mA
1.90	62.93mA	36.35mA	82.27mA
2.00	63.40mA	36.55mA	83.51mA
2.10	63.75mA	36.71mA	84.41mA
2.20	64.01mA	36.84mA	85.06mA
2.30	64.23mA	36.95mA	85.54mA
2.40	64.41mA	37.04mA	85.91mA
2.50	64.56mA	37.13mA	86.20mA
2.60	64.70mA	37.21mA	86.45mA

2.70	64.82mA	37.28mA	86.66mA
2.80	64.94mA	37.34mA	86.85mA
2.90	65.04mA	37.40mA	87.02mA
3.00	65.14mA	37.46mA	87.17mA
3.10	65.23mA	37.51mA	87.32mA
3.20	65.32mA	37.57mA	87.45mA
3.30	65.40mA	37.63mA	87.58mA
3.40	65.49mA	37.81mA	87.70mA
3.50	65.59mA	38.34mA	87.82mA
3.60	65.66mA	39.10mA	87.93mA
3.70	65.75mA	39.94mA	88.05mA
3.80	65.86mA	40.42mA	88.16mA
3.90	66.08mA	38.09mA	88.29mA
4.00	66.86mA	38.16mA	88.44mA
4.10	68.11mA	38.25mA	88.63mA
4.20	69.36mA	38.35mA	88.90mA
4.30	67.34mA	38.47mA	89.46mA
4.50	67.43mA	38.78mA	92.67mA
4.70	68.10mA	39.19mA	95.47mA
4.90	69.00mA	39.73mA	91.91mA
5.10	70.20mA	40.44mA	93.29mA
5.30	71.67mA	41.32mA	95.00mA
5.50	73.47mA	42.38mA	97.12mA
5.70	75.61mA	43.64mA	99.69mA
5.90	78.09mA	45.10mA	0.10A
6.10	80.89mA	46.75mA	0.11A
6.60	89.06mA	51.59mA	0.12A

|

[Pullup]

voltage	I(typ)	I(min)	I(max)
-3.30	0.16A	0.12A	0.19A
-3.10	0.16A	0.12A	0.18A
-2.90	0.15A	0.11A	0.17A
-2.70	0.14A	0.11A	0.16A
-2.50	0.14A	0.10A	0.16A
-2.30	0.13A	96.26mA	0.15A
-2.10	0.12A	89.72mA	0.14A
-1.90	0.11A	82.79mA	0.13A
-1.70	0.10A	75.47mA	0.12A
-1.50	93.76mA	67.80mA	0.11A
-1.00	70.54mA	46.98mA	82.43mA
-0.90	63.97mA	42.83mA	74.23mA
-0.80	56.74mA	41.47mA	65.83mA
-0.70	49.39mA	36.27mA	57.50mA
-0.60	42.27mA	30.78mA	49.67mA
-0.50	35.43mA	25.27mA	41.79mA
-0.40	28.50mA	19.90mA	33.74mA
-0.30	21.47mA	14.79mA	25.52mA
-0.20	14.35mA	9.79mA	17.14mA
-0.10	7.19mA	4.85mA	8.64mA

0.00	34.08uA	11.19uA	71.92uA
0.10	-6.89mA	-4.62mA	-8.29mA
0.20	-13.43mA	-8.98mA	-16.24mA
0.30	-19.58mA	-13.08mA	-23.77mA
0.40	-25.36mA	-16.92mA	-30.88mA
0.50	-30.77mA	-20.50mA	-37.60mA
0.60	-35.81mA	-23.82mA	-43.93mA
0.70	-40.49mA	-26.89mA	-49.86mA
0.80	-44.83mA	-29.70mA	-55.41mA
0.90	-48.81mA	-32.27mA	-60.59mA
1.00	-52.46mA	-34.60mA	-65.39mA
1.10	-55.77mA	-36.68mA	-69.83mA
1.20	-58.75mA	-38.52mA	-73.91mA
1.30	-61.41mA	-40.13mA	-77.64mA
1.40	-63.75mA	-41.50mA	-81.02mA
1.50	-65.77mA	-42.65mA	-84.06mA
1.60	-67.50mA	-43.58mA	-86.77mA
1.70	-68.93mA	-44.31mA	-89.14mA
1.80	-70.10mA	-44.87mA	-91.20mA
1.90	-71.04mA	-45.31mA	-92.94mA
2.00	-71.82mA	-45.68mA	-94.40mA
2.10	-72.46mA	-46.00mA	-95.60mA
2.20	-73.01mA	-46.28mA	-96.60mA
2.30	-73.48mA	-46.53mA	-97.44mA
2.40	-73.90mA	-46.76mA	-98.15mA
2.50	-74.27mA	-46.97mA	-98.77mA
2.60	-74.60mA	-47.17mA	-99.31mA
2.70	-74.91mA	-47.35mA	-99.80mA
2.80	-75.18mA	-47.52mA	-0.10A
2.90	-75.44mA	-47.68mA	-0.10A
3.00	-75.68mA	-47.83mA	-0.10A
3.10	-75.90mA	-47.97mA	-0.10A
3.20	-76.12mA	-48.11mA	-0.10A
3.30	-76.32mA	-48.27mA	-0.10A
3.40	-76.52mA	-48.87mA	-0.10A
3.50	-76.71mA	-56.48mA	-0.10A
3.60	-76.89mA	-0.15A	-0.10A
3.70	-77.09mA	-0.95A	-0.10A
3.80	-77.56mA	-2.71A	-0.10A
3.90	-79.54mA	-4.50A	-0.10A
4.00	-90.56mA	-6.29A	-0.10A
4.10	-0.31A	-8.09A	-0.11A
4.20	-1.88A	-9.88A	-0.11A
4.30	-3.93A	-11.66A	-0.12A
4.50	-8.04A	-15.24A	-1.17A
4.70	-12.14A	-18.83A	-5.43A
4.90	-16.25A	-22.41A	-9.69A
5.10	-20.36A	-25.99A	-13.95A
5.30	-24.46A	-29.57A	-18.21A
5.50	-28.57A	-33.15A	-22.48A
5.70	-32.68A	-36.73A	-26.74A

```
  5.90          -36.78A         -40.31A         -31.00A
  6.10          -40.89A         -43.89A         -35.27A
  6.60          -51.16A         -52.84A         -45.93A
|
[GND_clamp]
| voltage       I(typ)          I(min)          I(max)
|
  -5.00         -85.90A         -77.84A         -88.40A
  -4.80         -81.80A         -74.26A         -84.14A
  -4.60         -77.70A         -70.68A         -79.88A
  -4.40         -73.60A         -67.10A         -75.62A
  -4.20         -69.50A         -63.52A         -71.36A
  -4.00         -65.40A         -59.94A         -67.10A
  -3.80         -61.30A         -56.36A         -62.84A
  -3.60         -57.20A         -52.78A         -58.58A
  -3.40         -53.10A         -49.20A         -54.32A
  -3.20         -49.00A         -45.62A         -50.06A
  -3.00         -44.90A         -42.04A         -45.80A
  -2.80         -40.80A         -38.46A         -41.54A
  -2.60         -36.69A         -34.89A         -37.28A
  -2.40         -32.59A         -31.31A         -33.02A
  -2.20         -28.49A         -27.73A         -28.76A
  -2.00         -24.38A         -24.15A         -24.50A
  -1.80         -20.28A         -20.57A         -20.24A
  -1.60         -16.17A         -16.99A         -15.97A
  -1.40         -12.06A         -13.40A         -11.71A
  -1.20         -7.96A          -9.83A          -7.45A
  -1.00         -3.86A          -6.25A          -3.19A
  -0.80         -0.23A          -2.66A          -70.76mA
  -0.60         -2.22mA         -0.10A          -5.90mA
  -0.40         -89.20uA        -0.52mA         -0.26mA
  0.20          -27.89uA        -14.67uA        -42.88uA
  -0.00         -62.88nA        -63.80nA        -74.38nA
  0.20          18.73uA         7.33uA          32.30uA
  0.40          29.21uA         10.27uA         54.14uA
  0.60          32.51uA         10.69uA         65.81uA
  0.80          33.09uA         10.80uA         69.35uA
  1.00          33.31uA         10.87uA         70.19uA
  1.20          33.46uA         10.93uA         70.56uA
  1.40          33.58uA         10.98uA         70.81uA
  1.60          33.69uA         11.03uA         71.00uA
  1.80          33.78uA         11.08uA         71.17uA
  2.00          33.87uA         11.12uA         71.33uA
  2.20          33.96uA         11.14uA         71.47uA
  2.40          34.01uA         11.15uA         71.62uA
  2.60          34.03uA         11.16uA         71.76uA
  2.80          34.04uA         11.17uA         71.84uA
  3.00          34.05uA         11.18uA         71.86uA
  3.20          34.06uA         11.57uA         71.88uA
  3.40          34.08uA         10.87uA         71.90uA
  3.60          34.10uA         10.17uA         71.92uA
```

3.80	34.12uA	9.47uA	71.94uA
4.00	34.14uA	8.77uA	71.96uA
4.20	34.16uA	8.07uA	71.98uA
4.40	34.18uA	7.37uA	72.00uA
4.60	34.20uA	6.67uA	72.02uA
4.80	34.22uA	5.97uA	72.04uA
5.00	34.24uA	5.27uA	72.06uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	48.54uA	16.29uA	95.93uA
-4.90	48.21uA	16.17uA	95.42uA
-4.80	47.88uA	16.05uA	94.91uA
-4.70	47.55uA	15.93uA	94.40uA
-4.60	47.22uA	15.81uA	93.89uA
-4.50	46.89uA	15.69uA	93.38uA
-4.40	46.56uA	15.57uA	92.87uA
-4.30	46.23uA	15.45uA	92.36uA
-4.20	45.90uA	15.33uA	91.85uA
-4.10	45.57uA	15.21uA	91.34uA
-4.00	45.24uA	15.09uA	90.83uA
-3.90	44.91uA	14.97uA	90.32uA
-3.80	44.58uA	14.85uA	89.81uA
-3.70	44.25uA	14.73uA	89.30uA
-3.60	43.92uA	14.61uA	88.79uA
-3.50	43.59uA	14.49uA	88.28uA
-3.40	43.26uA	14.37uA	87.77uA
-3.30	42.93uA	14.25uA	87.26uA
-3.20	42.60uA	14.13uA	86.75uA
-3.10	42.27uA	14.01uA	86.24uA
-3.00	41.94uA	13.89uA	85.73uA
-2.90	41.61uA	13.77uA	85.22uA
-2.80	41.28uA	13.65uA	84.71uA
-2.70	40.95uA	13.53uA	84.20uA
-2.60	40.62uA	13.41uA	83.69uA
2.50	40.29uA	13.29uA	83.18uA
-2.40	39.96uA	13.17uA	82.67uA
-2.30	39.63uA	13.05uA	82.16uA
-2.20	39.30uA	12.93uA	81.65uA
-2.10	38.97uA	12.81uA	81.14uA
-2.00	38.64uA	12.69uA	80.63uA
-1.90	38.31uA	12.57uA	80.12uA
-1.80	37.98uA	12.45uA	79.61uA
-1.70	37.65uA	12.33uA	79.10uA
-1.60	37.32uA	12.22uA	78.59uA
-1.50	36.99uA	12.11uA	78.08uA
-1.40	36.68uA	12.02uA	77.57uA
-1.30	36.39uA	11.92uA	77.06uA
-1.20	36.12uA	11.84uA	76.55uA
-1.10	35.87uA	11.76uA	76.04uA

```
  -1.00          35.63uA        11.69uA        75.53uA
  -0.90          35.42uA        11.63uA        75.06uA
  -0.80           35.23uA       11.58uA        74.64uA
  -0.70          35.06uA        11.53uA        4.25uA
  -0.60          34.91uA        11.48uA        73.90uA
  -0.50          34.78uA        11.44uA        73.58uA
  -0.40          34.66uA        11.41uA        73.31uA
  -0.30           34.56uA       11.38uA        73.07uA
  -0.20          34.48uA        11.36uA        72.87uA
  -0.10          34.41uA        11.34uA        72.69uA
  0.00           34.35uA        11.32uA        72.55uA
|
[Ramp]
| variable      typ            min            max
  dV/dt_r       1.43/2.06n     1.08/2.82n     1.66/1.86n
  dV/dt_f       1.39/2.80n     0.98/4.41n     1.61/2.52n
R_load = 50.00
|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F
| time          V(typ)         V(min)         V(max)

  0.000S        0.71uV         0.94uV         0.68uV
  0.20nS        0.48uV         0.81uV         0.000V
  0.40nS        -6.07uV        -1.89uV        12.38uV
  0.60nS        -0.29mV        -5.66uV        -3.13mV
  0.80nS        -3.39mV        26.90uV        -6.39mV
  1.00nS        -4.34mV        -5.17uV        43.34mV
  1.20nS        25.79mV        -0.87mV        0.11V
  1.40nS        62.40mV        -3.65mV        0.15V
  1.60nS        0.11V          -7.89mV        0.21V
  1.80nS        0.16V          0.71mV         0.28V
  2.00nS        0.22V          29.71mV        0.37V
  2.20nS        0.28V          65.63mV        0.46V
  2.40nS        0.37V          0.10V          0.59V
  2.60nS        0.48V          0.15V          0.71V
  2.80nS        0.63V          0.22V          0.92V
  3.00nS        0.79V          0.28V          1.12V
  3.20nS        0.90V          0.34V          1.28V
  3.40nS        1.07V          0.43V          1.49V
  3.60nS        1.24V          0.53V          1.70V
  3.80nS        1.39V          0.63V          1.89V
  4.00nS        1.55V          0.74V          2.07V
  4.20nS        1.71V          0.86V          2.24V
  4.40nS        1.84V          0.97V          2.37V
  4.60nS        1.90V          1.03V          2.44V
```

4.80nS	1.96V	1.09V	2.50V
5.00nS	2.03V	1.16V	2.54V
5.20nS	2.08V	1.22V	2.59V
5.40nS	2.13V	1.29V	2.62V
5.60nS	2.18V	1.36V	2.65V
5.80nS	2.20V	1.39V	2.66V
6.00nS	2.22V	1.43V	2.67V
6.20nS	2.24V	1.47V	2.68V
6.40nS	2.26V	1.51V	2.69V
6.60nS	2.27V	1.54V	2.70V
6.80nS	2.29V	1.57V	2.71V
7.00nS	2.30V	1.60V	2.72V
7.20nS	2.31V	1.63V	2.72V
7.40nS	2.32V	1.66V	2.73V
7.60nS	2.33V	1.68V	2.74V
7.80nS	2.34V	1.69V	2.74V
8.00nS	2.34V	1.70V	2.74V
8.20nS	2.35V	1.72V	2.75V
8.40nS	2.35V	1.73V	2.75V
8.60nS	2.36V	1.74V	2.75V
8.80nS	2.36V	1.75V	2.76V
9.00nS	2.36V	1.76V	2.76V
9.20nS	2.37V	1.77V	2.76V
9.40nS	2.37V	1.78V	2.76V
9.60nS	2.38V	1.79V	2.77V
9.80nS	2.38V	1.80V	2.77V
10.00nS	2.38V	1.80V	2.77V

|

[Rising Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.98V	1.34V	0.92V
0.20nS	0.98V	1.34V	0.92V
0.40nS	0.98V	1.34V	0.92V
0.60nS	0.98V	1.34V	0.92V
0.80nS	0.99V	1.34V	0.94V
1.00nS	1.05V	1.34V	1.07V
1.20nS	1.18V	1.34V	1.24V
1.40nS	1.31V	1.36V	1.37V
1.60nS	1.49V	1.44V	1.55V
1.80nS	1.69V	1.57V	1.76V
2.00nS	1.92V	1.73V	2.02V
2.20nS	2.18V	1.92V	2.33V
2.40nS	2.46V	2.11V	2.62V
2.60nS	2.73V	2.32V	2.91V

2.80nS	2.97V	2.55V	3.20V
3.00nS	3.09V	2.69V	3.33V
3.20nS	3.15V	2.76V	3.39V
3.40nS	3.20V	2.86V	3.44V
3.60nS	3.24V	2.92V	3.50V
3.80nS	3.26V	2.95V	3.53V
4.00nS	3.28V	2.98V	3.55V
4.20nS	3.29V	2.99V	3.57V
4.40nS	3.29V	2.99V	3.59V
4.60nS	3.30V	3.00V	3.59V
4.80nS	3.30V	3.00V	3.59V
5.00nS	3.30V	3.00V	3.60V
5.20nS	3.30V	3.00V	3.60V
5.40nS	3.30V	3.00V	3.60V
5.60nS	3.30V	3.00V	3.60V
5.80nS	3.30V	3.00V	3.60V
6.00nS	3.30V	3.00V	3.60V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|

[Falling Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.41V	1.87V	2.79V
0.20nS	2.41V	1.87V	2.79V
0.40nS	2.41V	1.87V	2.79V
0.60nS	2.41V	1.87V	2.76V

0.80nS	2.37V	1.87V	2.62V
1.00nS	2.24V	1.86V	2.44V
1.20nS	2.07V	1.85V	2.25V
1.40nS	1.94V	1.82V	2.10V
1.60nS	1.76V	1.75V	1.85V
1.80nS	1.54V	1.65V	1.55V
2.00nS	1.28V	1.51V	1.23V
2.20nS	1.01V	1.36V	0.96V
2.40nS	0.78V	1.18V	0.77V
2.60nS	0.61V	0.99V	0.63V
2.80nS	0.46V	0.76V	0.51V
3.00nS	0.37V	0.59V	0.43V
3.20nS	0.33V	0.49V	0.37V
3.40nS	0.26V	0.39V	0.32V
3.60nS	0.21V	0.31V	0.27V
3.80nS	0.17V	0.25V	0.22V
4.00nS	0.14V	0.19V	0.19V
4.20nS	0.10V	0.15V	0.14V
4.40nS	73.29mV	0.10V	0.11V
4.60nS	60.19mV	87.46mV	93.57mV
4.80nS	48.89mV	70.67mV	8.29mV
5.00nS	34.23mV	50.83mV	61.98mV
5.20nS	24.65mV	38.23mV	46.06mV
5.40nS	14.47mV	23.57mV	32.51mV
5.60nS	8.10mV	14.65mV	20.47mV
5.80nS	5.49mV	9.93mV	15.65mV
6.00nS	3.06mV	6.30mV	11.70mV
6.20nS	1.82mV	4.27mV	6.64mV
6.40nS	1.09mV	2.24mV	4.15mV
6.60nS	0.61mV	1.46mV	2.31mV
6.80nS	0.54mV	1.08mV	1.05mV
7.00nS	0.47mV	0.78mV	0.76mV
7.20nS	0.42mV	0.69mV	0.48mV
7.40nS	0.35mV	0.59mV	0.37mV
7.60nS	0.31mV	0.52mV	0.31mV
7.80nS	0.29mV	0.48mV	0.29mV
8.00nS	0.27mV	0.45mV	0.26mV
8.20nS	0.24mV	0.40mV	0.24mV
8.40nS	0.20mV	0.35mV	0.21mV
8.60nS	0.18mV	0.32mV	0.18mV
8.80nS	0.18mV	0.31mV	0.16mV
9.00nS	0.17mV	0.28mV	0.16mV
9.20nS	0.15mV	0.24mV	0.15mV
9.40nS	0.12mV	0.20mV	0.12mV
9.60nS	0.10mV	0.19mV	93.74uV
9.80nS	0.11mV	0.20mV	90.71uV
10.00nS	0.11mV	0.17mV	97.83uV

|

[Falling Waveform]

R_fixture = 50.00

V_fixture = 3.30

V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.52V
1.00nS	3.25V	3.00V	3.43V
1.20nS	3.17V	3.00V	3.34V
1.40nS	3.12V	3.00V	3.27V
1.60nS	3.05V	3.00V	3.17V
1.80nS	2.97V	2.97V	3.06V
2.00nS	2.87V	2.92V	2.95V
2.20nS	2.78V	2.87V	2.83V
2.40nS	2.68V	2.82V	2.70V
2.60nS	2.58V	2.76V	2.58V
2.80nS	2.45V	2.69V	2.43V
3.00nS	2.34V	2.62V	2.30V
3.20nS	2.26V	2.57V	2.21V
3.40nS	2.17V	2.50V	2.07V
3.60nS	2.07V	2.44V	1.91V
3.80nS	1.98V	2.38V	1.76V
4.00nS	1.89V	2.32V	1.62V
4.20nS	1.76V	2.25V	1.49V
4.40nS	1.63V	2.18V	1.37V
4.60nS	1.55V	2.15V	1.32V
4.80nS	1.48V	2.11V	1.27V
5.00nS	1.40V	2.06V	1.21V
5.20nS	1.32V	2.01V	1.16V
5.40nS	1.25V	1.96V	1.10V
5.60nS	1.19V	1.92V	1.06V
5.80nS	1.15V	1.89V	1.04V
6.00nS	1.13V	1.87V	1.02V
6.20nS	1.10V	1.84V	1.00V
6.40nS	1.07V	1.81V	0.98V
6.60nS	1.05V	1.78V	0.96V
6.80nS	1.03V	1.75V	0.95V
7.00nS	1.02V	1.72V	0.94V
7.20nS	1.01V	1.70V	0.93V
7.40nS	1.00V	1.67V	0.93V
7.60nS	1.00V	1.64V	0.92V
7.80nS	1.00V	1.62V	0.92V
8.00nS	1.00V	1.60V	0.92V
8.20nS	0.99V	1.57V	0.92V
8.40nS	0.99V	1.53V	0.92V
8.60nS	0.99V	1.50V	0.92V
8.80nS	0.99V	1.47V	0.92V

```
  9.00nS      0.99V          1.44V          0.92V
  9.20nS      0.99V          1.42V          0.92V
  9.40nS      0.99V          1.40V          0.92V
  9.60nS      0.99V          1.38V          0.92V
  9.80nS      0.99V          1.37V          0.92V
  10.00nS     0.99V          1.36V          0.92V
|
| End [Model] prd16dgz
|
|*****************************************************************************
|                          Model prd24dgz
|*****************************************************************************
|
[Model]          prd24dgz
Model_type       I/O
Polarity         Non-Inverting
Enable           Active-Low
Vinl =   0.80V
Vinh =   2.00V
Vmeas =   1.50V
Cref =  50.00pF
Rref =   1.00M
Vref =  0.000V
C_comp                        4.15pF          3.73pF          4.56pF
|
|
[Temperature Range]           25.00           0.12k           0.000
[Pullup Reference]            3.30V           3.00V           3.60V
[Pulldown Reference]         0.000V          0.000V          0.000V
[POWER Clamp Reference]      5.00V           4.50V           5.50V
[GND Clamp Reference]        0.000V          0.000V          0.000V
[Pulldown]
|  voltage       I(typ)          I(min)          I(max)
|
  -3.30          -10.00mA        0.000A          0.000A
  -3.10          0.000A          0.000A          -10.00mA
  -2.90          0.000A          0.000A          0.000A
  -2.70          0.000A          0.000A          0.000A
  -2.50          0.000A          0.000A          0.000A
  -2.30          0.000A          0.000A          -10.00mA
  -2.10          -10.00mA        0.000A          -10.00mA
  -1.90          -10.00mA        0.000A          -10.00mA
  -1.70          -10.00mA        -10.00mA        -10.00mA
  -1.50          -10.00mA        -10.00mA        -20.00mA
  -1.00          -19.00mA        -10.00mA        -23.00mA
  -0.90          -21.00mA        -10.00mA        -26.00mA
  -0.80          -41.70mA        -11.00mA        -55.33mA
  -0.70          -50.61mA        -14.60mA        -55.12mA
  -0.60          -46.07mA        -25.10mA        -50.21mA
  -0.50          -39.45mA        -26.37mA        -43.90mA
  -0.40          -32.03mA        -22.06mA        -36.08mA
```

-0.30	-24.29mA	-16.63mA	-27.48mA
-0.20	-16.36mA	-11.11mA	-18.57mA
-0.10	-8.26mA	-5.55mA	-9.40mA
-0.00	3.80nA	7.33nA	12.06nA
0.10	8.11mA	5.36mA	9.30mA
0.20	15.76mA	10.37mA	18.18mA
0.30	22.98mA	15.05mA	26.64mA
0.40	29.76mA	19.40mA	34.69mA
0.50	36.11mA	23.42mA	42.32mA
0.60	42.04mA	27.12mA	49.54mA
0.70	47.55mA	30.50mA	56.36mA
0.80	52.66mA	33.58mA	62.78mA
0.90	57.35mA	36.36mA	68.80mA
1.00	61.65mA	38.84mA	74.42mA
1.10	65.55mA	41.04mA	79.65mA
1.20	69.06mA	42.96mA	84.48mA
1.30	72.19mA	44.61mA	88.92mA
1.40	74.94mA	45.99mA	92.97mA
1.50	77.32mA	47.12mA	96.63mA
1.60	79.33mA	48.01mA	99.91mA
1.70	80.95mA	48.68mA	0.10A
1.80	82.19mA	49.17mA	0.11A
1.90	83.09mA	49.54mA	0.11A
2.00	83.74mA	49.83mA	0.11A
2.10	84.23mA	50.06mA	0.11A
2.20	84.62mA	50.25mA	0.11A
2.30	84.93mA	50.42mA	0.11A
2.40	85.20mA	50.57mA	0.11A
2.50	85.44mA	50.70mA	0.11A
2.60	85.65mA	50.82mA	0.11A
2.70	85.84mA	50.93mA	0.11A
2.80	86.01mA	51.03mA	0.11A
2.90	86.18mA	51.13mA	0.11A
3.00	86.33mA	51.22mA	0.11A
3.10	86.48mA	51.31mA	0.11A
3.20	86.62mA	51.40mA	0.11A
3.30	86.75mA	51.50mA	0.11A
3.40	86.89mA	51.73mA	0.12A
3.50	87.06mA	52.32mA	0.12A
3.60	87.16mA	53.14mA	0.12A
3.70	87.30mA	54.02mA	0.12A
3.80	87.47mA	54.48mA	0.12A
3.90	87.77mA	52.16mA	0.12A
4.00	88.66mA	52.28mA	0.12A
4.10	90.00mA	52.42mA	0.12A
4.20	91.34mA	52.58mA	0.12A
4.30	89.39mA	52.77mA	0.12A
4.50	89.66mA	53.24mA	0.12A
4.70	90.64mA	53.86mA	0.12A
4.90	91.94mA	54.68mA	0.12A
5.10	93.66mA	55.73mA	0.12A

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  5.30          95.77mA       57.03mA       0.13A
  5.50          98.33mA       58.59mA       0.13A
  5.70          0.10A         60.44mA       0.13A
  5.90          0.10A         62.55mA       0.14A
  6.10          0.11A         64.93mA       0.14A
  6.60          0.12A         71.83mA       0.15A
|
[Pullup]
| voltage      I(typ)        I(min)        I(max)
|
  -3.30         0.22A         0.16A         0.25A
  -3.10         0.21A         0.16A         0.24A
  -2.90         0.20A         0.15A         0.23A
   -2.70        0.19A         0.14A         0.22A
  -2.50         0.18A         0.14A         0.21A
  -2.30         0.17A         0.13A         0.20A
  -2.10         0.16A         0.12A         0.19A
  -1.90         0.15A         0.11A         0.17A
  -1.70         0.14A         0.10A         0.16A
  -1.50         0.12A         90.15mA       0.14A
  -1.00         92.80mA       62.50mA       0.11A
  -0.90         84.30mA       57.02mA       97.94mA
  -0.80         75.06mA       54.41mA       87.24mA
  -0.70         65.63mA       47.70mA       76.50mA
  -0.60         56.31mA       40.65mA       66.14mA
  -0.50         47.22mA       33.53mA       55.68mA
  -0.40         38.00mA       26.51mA       44.96mA
  -0.30         28.62mA       19.71mA       34.00mA
  -0.20         19.12mA       13.04mA       22.83mA
  -0.10         9.57mA        6.46mA        11.50mA
  0.00          34.08uA       11.19uA       71.92uA
  0.10          -9.20mA       -6.16mA       -11.08mA
  0.20          -17.92mA      -11.98mA      -21.68mA
  0.30          -26.12mA      -17.45mA      -31.71mA
  0.40          -33.83mA      -22.56mA      -41.21mA
  0.50          -41.04mA      -27.33mA      -50.17mA
  0.60          -47.76mA      -31.76mA      -58.60mA
  0.70          -54.01mA      -35.85mA      -66.51mA
  0.80          -59.78mA      -39.61mA      -73.91mA
  0.90          -65.10mA      -43.04mA      -80.81mA
  1.00          -69.96mA      -46.14mA      -87.22mA
  1.10          -74.37mA      -48.91mA       -93.14mA
  1.20          -78.35mA      -51.37mA      -98.58mA
  1.30          -81.89mA      -53.51mA      -0.10A
  1.40          -85.01mA      -55.34mA      -0.11A
  1.50          -87.72mA      -56.87mA      -0.11A
  1.60           -90.01mA     -58.11mA      -0.12A
  1.70          -91.93mA      -59.08mA      -0.12A
  1.80          -93.48mA      -59.83mA      -0.12A
  1.90          -94.74mA      -60.42mA      -0.12A
  2.00          -95.77mA      -60.91mA      -0.13A
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  2.10          -96.63mA      -61.34mA      -0.13A
  2.20          -97.36mA      -61.71mA      -0.13A
  2.30          -97.99mA      -62.05mA      -0.13A
  2.40          -98.55mA      -62.36mA      -0.13A
  2.50          -99.04mA      -62.64mA      -0.13A
  2.60          -99.49mA      -62.90mA      -0.13A
  2.70           -99.89mA     -63.14mA      -0.13A
  2.80           -0.10A        -63.36mA      -0.13A
  2.90          -0.10A        -63.57mA      -0.13A
  3.00          -0.10A        -63.78mA      -0.13A
  3.10          -0.10A        -63.97mA      -0.14A
  3.20          -0.10A        -64.15mA      -0.14A
  3.30          -0.10A        -64.35mA      -0.14A
  3.40          -0.10A        -64.99mA      -0.14A
  3.50          -0.10A        -72.69mA      -0.14A
  3.60          -0.10A        -0.17A        -0.14A
  3.70          -0.10A        -0.97A        -0.14A
  3.80          -0.10A        -2.72A        -0.14A
  3.90          -0.11A        -4.50A        -0.14A
  4.00          -0.12A        -6.28A        -0.14A
  4.10          -0.34A        -8.06A        -0.14A
  4.20          -1.90A        -9.85A        -0.14A
  4.30          -3.94A        -11.62A       -0.15A
  4.50          -8.02A        -15.19A       -1.21A
  4.70          -12.10A       -18.75A       -5.43A
  4.90          -16.18A       -22.31A       -9.67A
  5.10          -20.27A       -25.88A       -13.90A
  5.30          -24.35A       -29.44A       -18.14A
  5.50          -28.43A       -33.00A       -22.38A
  5.70          -32.51A       -36.56A       -26.62A
  5.90          -36.60A       -40.13A       -30.86A
  6.10          -40.68A       -43.69A       -35.09A
  6.60          -50.89A       -52.59A       -45.69A
|
[GND_clamp]
| voltage       I(typ)        I(min)        I(max)
|
  -5.00         -85.26A       -77.43A       -87.91A
  -4.80         -81.20A       -73.87A       -83.67A
  -4.60         -77.14A       -70.31A       -79.43A
  -4.40         -73.08A       -66.75A       -75.19A
  -4.20         -69.02A       -63.19A       -70.95A
  -4.00          -64.96A      -59.63A       -66.71A
  -3.80         -60.90A       -56.07A       -62.47A
  -3.60         -56.84A       -52.51A       -58.23A
  -3.40          -52.78A      -48.95A       -53.99A
  -3.20         -48.72A       -45.39A       -49.75A
  -3.00         -44.64A       -41.83A       -45.52A
  -2.80         -40.56A       -38.27A       -41.29A
  -2.60         -36.48A       -34.71A       -37.05A
  -2.40          -32.40A      -31.15A       -32.82A
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-2.20	-28.32A	-27.59A	-28.58A
-2.00	-24.24A	-24.03A	-24.35A
-1.80	-20.16A	-20.47A	-20.11A
-1.60	-16.08A	-16.90A	-15.88A
-1.40	-12.00A	-13.34A	-11.64A
-1.20	-7.92A	-9.78A	-7.41A
-1.00	-3.84A	-6.22A	-3.18A
-0.80	-0.23A	-2.66A	-71.67mA
-0.60	-2.33mA	-0.10A	-6.23mA
-0.40	-91.55uA	-0.52mA	-0.28mA
-0.20	-27.91uA	-14.70uA	-42.94uA
-0.00	-75.80nA	-77.03nA	-90.19nA
0.20	18.72uA	7.32uA	32.29uA
0.40	29.20uA	10.26uA	54.13uA
0.60	32.50uA	10.68uA	65.79uA
0.80	33.08uA	10.79uA	69.34uA
1.00	33.30uA	10.86uA	70.18uA
1.20	33.45uA	10.92uA	70.55uA
1.40	33.57uA	10.98uA	70.80uA
1.60	33.68uA	11.03uA	71.00uA
1.80	33.78uA	11.07uA	71.16uA
2.00	33.87uA	11.11uA	71.32uA
2.20	33.96uA	11.14uA	71.47uA
2.40	34.01uA	11.15uA	71.61uA
2.60	34.03uA	11.16uA	71.76uA
2.80	34.04uA	11.17uA	71.84uA
3.00	34.05uA	11.18uA	71.86uA
3.20	34.06uA	11.75uA	71.88uA
3.40	34.08uA	10.69uA	71.90uA
3.60	34.10uA	9.63uA	71.92uA
3.80	34.12uA	8.57uA	71.94uA
4.00	34.14uA	7.51uA	71.96uA
4.20	34.16uA	6.45uA	71.98uA
4.40	34.18uA	5.39uA	72.00uA
4.60	34.20uA	4.33uA	72.02uA
4.80	34.22uA	3.27uA	72.04uA
5.00	34.24uA	2.21uA	72.06uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	48.55uA	16.31uA	95.55uA
-4.90	48.22uA	16.19uA	95.05uA
-4.80	47.89uA	16.07uA	94.55uA
-4.70	47.56uA	15.95uA	94.05uA
-4.60	47.23uA	15.83uA	93.55uA
-4.50	46.90uA	15.71uA	93.05uA
-4.40	46.57uA	15.59uA	92.55uA
-4.30	46.24uA	15.47uA	92.05uA
-4.20	45.91uA	15.35uA	91.55uA
-4.10	45.58uA	15.23uA	91.05uA

-4.00	45.25uA	15.11uA	90.55uA
-3.90	44.92uA	14.99uA	90.05uA
-3.80	44.59uA	14.87uA	89.55uA
-3.70	44.26uA	14.75uA	89.05uA
-3.60	43.93uA	14.63uA	88.55uA
-3.50	43.60uA	14.51uA	88.05uA
-3.40	43.27uA	14.39uA	87.55uA
-3.30	42.94uA	14.27uA	87.05uA
-3.20	42.61uA	14.15uA	86.55uA
-3.10	42.28uA	14.03uA	86.05uA
-3.00	41.95uA	13.91uA	85.55uA
-2.90	41.62uA	13.79uA	85.05uA
-2.80	41.29uA	13.67uA	84.55uA
-2.70	40.96uA	13.55uA	84.05uA
-2.60	40.63uA	13.43uA	83.55uA
-2.50	40.30uA	13.31uA	83.05uA
-2.40	39.97uA	13.19uA	82.55uA
-2.30	39.64uA	13.07uA	82.05uA
-2.20	39.31uA	12.95uA	81.55uA
-2.10	38.98uA	12.83uA	81.05uA
-2.00	38.65uA	12.71uA	80.55uA
-1.90	38.32uA	12.59uA	80.05uA
-1.80	37.99uA	12.47uA	79.55uA
-1.70	37.66uA	12.35uA	79.05uA
-1.60	37.33uA	12.23uA	78.55uA
-1.50	37.00uA	12.13uA	78.05uA
-1.40	36.69uA	12.03uA	77.55uA
-1.30	36.40uA	11.94uA	77.05uA
-1.20	36.13uA	11.85uA	76.55uA
-1.10	35.88uA	11.78uA	76.05uA
-1.00	35.64uA	11.71uA	75.55uA
-0.90	35.43uA	11.64uA	75.08uA
-0.80	35.24uA	11.59uA	74.65uA
-0.70	35.07uA	11.54uA	74.26uA
-0.60	34.92uA	11.49uA	73.91uA
-0.50	34.79uA	11.45uA	73.60uA
-0.40	34.67uA	11.42uA	73.32uA
-0.30	34.57uA	11.39uA	73.08uA
-0.20	34.49uA	11.37uA	72.88uA
-0.10	34.42uA	11.35uA	72.70uA
0.00	34.36uA	11.33uA	72.56uA

|

[Ramp]

variable	typ	min	max
dV/dt_r	1.54/2.22n	1.20/2.88n	1.77/2.15n
dV/dt_f	1.52/3.16n	1.15/4.46n	1.73/3.00n

R_load = 50.00

|

[Rising Waveform]

R_fixture = 50.00

V_fixture = 0.000

V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.70uV	0.92uV	0.68uV
0.20nS	0.45uV	0.77uV	0.000V
0.40nS	-5.49uV	-1.76uV	16.07uV
0.60nS	-0.25mV	-4.97uV	-2.66mV
0.80nS	-2.88mV	24.27uV	-5.55mV
1.00nS	-3.85mV	-5.54uV	32.40mV
1.20nS	18.80mV	-0.76mV	80.52mV
1.40nS	45.63mV	-3.09mV	0.11V
1.60nS	80.05mV	-6.58mV	0.16V
1.80nS	0.11V	-0.18mV	0.21V
2.00nS	0.16V	21.52mV	0.27V
2.20nS	0.20V	48.21mV	0.33V
2.40nS	0.26V	76.15mV	0.41V
2.60nS	0.32V	0.11V	0.48V
2.80nS	0.41V	0.16V	0.61V
3.00nS	0.51V	0.19V	0.73V
3.20nS	0.58V	0.24V	0.82V
3.40nS	0.71V	0.30V	0.97V
3.60nS	0.85V	0.36V	1.16V
3.80nS	1.00V	0.45V	1.35V
4.00nS	1.17V	0.54V	1.55V
4.20nS	1.38V	0.67V	1.80V
4.40nS	1.57V	0.80V	2.03V
4.60nS	1.68V	0.88V	2.15V
4.80nS	1.78V	0.96V	2.26V
5.00nS	1.91V	1.06V	2.39V
5.20nS	2.01V	1.15V	2.51V
5.40nS	2.13V	1.25V	2.61V
5.60nS	2.22V	1.34V	2.70V
5.80nS	2.27V	1.40V	2.74V
6.00nS	2.31V	1.44V	2.77V
6.20nS	2.35V	1.50V	2.80V
6.40nS	2.38V	1.56V	2.82V
6.60nS	2.41V	1.61V	2.84V
6.80nS	2.43V	1.66V	2.86V
7.00nS	2.45V	1.70V	2.87V
7.20nS	2.46V	1.74V	2.88V
7.40nS	2.48V	1.78V	2.89V
7.60nS	2.49V	1.82V	2.90V
7.80nS	2.50V	1.84V	2.91V
8.00nS	2.51V	1.86V	2.91V
8.20nS	2.52V	1.88V	2.92V
8.40nS	2.52V	1.90V	2.92V
8.60nS	2.53V	1.92V	2.92V
8.80nS	2.54V	1.93V	2.93V

9.00nS	2.54V	1.95V	2.93V
9.20nS	2.55V	1.96V	2.94V
9.40nS	2.55V	1.97V	2.94V
9.60nS	2.56V	1.98V	2.94V
9.80nS	2.56V	2.00V	2.95V
10.00nS	2.57V	2.00V	2.95V

|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.76V	1.03V	0.72V
0.20nS	0.76V	1.03V	0.72V
0.40nS	0.76V	1.03V	0.72V
0.60nS	0.76V	1.03V	0.72V
0.80nS	0.77V	1.03V	0.73V
1.00nS	0.81V	1.03V	0.82V
1.20nS	0.90V	1.03V	0.93V
1.40nS	0.98V	1.04V	1.01V
1.60nS	1.09V	1.11V	1.13V
1.80nS	1.22V	1.20V	1.26V
2.00nS	1.35V	1.32V	1.42V
2.20nS	1.51V	1.45V	1.58V
2.40nS	1.69V	1.59V	1.78V
2.60nS	1.91V	1.74V	2.02V
2.80nS	2.22V	1.96V	2.36V
3.00nS	2.47V	2.16V	2.63V
3.20nS	2.65V	2.31V	2.82V
3.40nS	2.85V	2.49V	3.03V
3.60nS	2.97V	2.62V	3.17V
3.80nS	3.08V	2.73V	3.30V
4.00nS	3.14V	2.83V	3.36V
4.20nS	3.19V	2.89V	3.42V
4.40nS	3.23V	2.94V	3.47V
4.60nS	3.25V	2.95V	3.50V
4.80nS	3.27V	2.97V	3.52V
5.00nS	3.28V	2.98V	3.54V
5.20nS	3.29V	2.99V	3.56V
5.40nS	3.29V	2.99V	3.57V
5.60nS	3.30V	3.00V	3.58V
5.80nS	3.30V	3.00V	3.59V
6.00nS	3.30V	3.00V	3.59V
6.20nS	3.30V	3.00V	3.59V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V

7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|
[Falling Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.62V	2.12V	2.99V
0.20nS	2.62V	2.12V	2.99V
0.40nS	2.62V	2.12V	2.99V
0.60nS	2.62V	2.12V	2.96V
0.80nS	2.60V	2.12V	2.85V
1.00nS	2.50V	2.12V	2.72V
1.20nS	2.38V	2.11V	2.59V
1.40nS	2.29V	2.09V	2.50V
1.60nS	2.17V	2.04V	2.36V
1.80nS	2.04V	1.96V	2.20V
2.00nS	1.89V	1.85V	2.00V
2.20nS	1.71V	1.74V	1.76V
2.40nS	1.51V	1.63V	1.49V
2.60nS	1.27V	1.50V	1.23V
2.80nS	0.99V	1.33V	0.98V
3.00nS	0.81V	1.17V	0.83V
3.20nS	0.71V	1.04V	0.75V
3.40nS	0.59V	0.87V	0.66V
3.60nS	0.51V	0.72V	0.57V
3.80nS	0.44V	0.59V	0.50V
4.00nS	0.37V	0.49V	0.45V
4.20nS	0.31V	0.40V	0.38V
4.40nS	0.26V	0.33V	0.32V
4.60nS	0.23V	0.28V	0.29V
4.80nS	0.20V	0.25V	0.26V

5.00nS	0.17V	0.21V	0.23V
5.20nS	0.15V	0.18V	0.20V
5.40nS	0.12V	0.14V	0.17V
5.60nS	92.71mV	0.11V	0.14V
5.80nS	79.46mV	96.17mV	0.12V
6.00nS	67.17mV	83.01mV	0.11V
6.20nS	54.74mV	65.86mV	89.82mV
6.40nS	42.77mV	53.06mV	75.55mV
6.60nS	33.26mV	41.31mV	61.63mV
6.80nS	25.46mV	31.29mV	50.25mV
7.00nS	18.21mV	23.99mV	40.51mV
7.20nS	13.43mV	16.92mV	31.37mV
7.40nS	8.06mV	11.32mV	23.11mV
7.60nS	4.81mV	6.46mV	15.54mV
7.80nS	3.27mV	4.82mV	12.49mV
8.00nS	1.98mV	3.62mV	9.63mV
8.20nS	1.32mV	2.10mV	6.17mV
8.40nS	0.78mV	1.45mV	4.24mV
8.60nS	0.50mV	1.01mV	2.46mV
8.80nS	0.42mV	0.70mV	1.45mV
9.00nS	0.34mV	0.61mV	0.94mV
9.20nS	0.30mV	0.51mV	0.50mV
9.40nS	0.27mV	0.45mV	0.38mV
9.60nS	0.24mV	0.40mV	0.28mV
9.80nS	0.21mV	0.35mV	0.23mV
10.00nS	0.22mV	0.32mV	0.21mV

|

[Falling Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	3.30V	3.00V	3.60V
0.20nS	3.30V	3.00V	3.60V
0.40nS	3.30V	3.00V	3.60V
0.60nS	3.30V	3.00V	3.59V
0.80nS	3.30V	3.00V	3.52V
1.00nS	3.25V	3.00V	3.44V
1.20nS	3.18V	3.00V	3.37V
1.40nS	3.14V	3.00V	3.32V
1.60nS	3.09V	3.00V	3.24V
1.80nS	3.03V	2.97V	3.16V
2.00nS	2.96V	2.92V	3.07V
2.20nS	2.88V	2.88V	2.98V
2.40nS	2.80V	2.84V	2.88V
2.60nS	2.72V	2.80V	2.78V
2.80nS	2.61V	2.74V	2.65V

```
  3.00nS      2.51V          2.68V          2.55V
  3.20nS      2.44V          2.64V          2.47V
  3.40nS      2.34V          2.58V          2.35V
  3.60nS      2.25V          2.52V          2.23V
  3.80nS      2.15V          2.46V          2.09V
  4.00nS      2.06V          2.39V          1.93V
  4.20nS      1.93V          2.32V          1.75V
  4.40nS      1.81V          2.24V          1.58V
  4.60nS      1.73V          2.20V          1.50V
  4.80nS      1.65V          2.15V          1.43V
  5.00nS      1.54V          2.09V          1.34V
  5.20nS      1.44V          2.04V          1.26V
  5.40nS      1.32V          1.97V          1.18V
  5.60nS      1.23V          1.91V          1.11V
  5.80nS      1.18V          1.87V          1.07V
  6.00nS      1.13V          1.84V          1.04V
  6.20nS      1.08V          1.79V          1.00V
  6.40nS      1.04V          1.75V          0.96V
  6.60nS      1.00V          1.71V          0.92V
  6.80nS      0.96V          1.67V          0.89V
  7.00nS      0.93V          1.63V          0.87V
  7.20nS      0.90V          1.59V          0.84V
  7.40nS      0.87V          1.54V          0.82V
  7.60nS      0.85V          1.48V          0.80V
  7.80nS      0.83V          1.44V          0.78V
  8.00nS      0.82V          1.40V          0.78V
  8.20nS      0.81V          1.35V          0.76V
  8.40nS      0.80V          1.31V          0.75V
  8.60nS      0.79V          1.27V          0.75V
  8.80nS      0.78V          1.23V          0.74V
  9.00nS      0.78V          1.20V          0.73V
  9.20nS      0.78V          1.17V          0.73V
  9.40nS      0.77V          1.15V          0.73V
  9.60nS      0.77V          1.12V          0.72V
  9.80nS      0.77V          1.10V          0.72V
  10.00nS     0.77V          1.09V          0.72V
|
| End [Model] prd24dgz
|
|*****************************************************************************
|                          Model prt24dgz
|*****************************************************************************
|
[Model]          prt24dgz
Model_type       3-state
Polarity         Non-Inverting
Enable           Active-Low
Vmeas =   1.50V
Cref =  50.00pF
Rref =   1.00M
Vref =  0.000V
```

C_comp	4.09pF	3.68pF	4.50pF
|			
|			
[Temperature Range]	25.00	0.12k	0.000
[Pullup Reference]	3.30V	3.00V	3.60V
[Pulldown Reference]	0.000V	0.000V	0.000V
[POWER Clamp Reference]	5.00V	4.50V	5.50V
[GND Clamp Reference]	0.000V	0.000V	0.000V
[Pulldown]			
| voltage	I(typ)	I(min)	I(max)
|			
-3.30	-10.00mA	0.000A	0.000A
-3.10	0.000A	0.000A	-10.00mA
-2.90	0.000A	0.000A	0.000A
-2.70	0.000A	0.000A	0.000A
-2.50	0.000A	0.000A	0.000A
-2.30	0.000A	0.000A	-10.00mA
-2.10	-10.00mA	0.000A	-10.00mA
-1.90	-10.00mA	0.000A	-10.00mA
-1.70	-10.00mA	-10.00mA	-10.00mA
-1.50	-10.00mA	-10.00mA	-20.00mA
-1.00	-20.00mA	-10.00mA	-23.00mA
-0.90	-21.00mA	-10.00mA	-26.00mA
-0.80	-41.70mA	-12.00mA	-55.37mA
-0.70	-50.60mA	-14.60mA	-55.11mA
-0.60	-46.07mA	-25.10mA	-50.21mA
-0.50	-39.45mA	-26.38mA	-43.90mA
-0.40	-32.03mA	-22.06mA	-36.09mA
-0.30	-24.30mA	-16.63mA	-27.49mA
-0.20	-16.36mA	-11.10mA	-18.57mA
-0.10	-8.26mA	-5.55mA	-9.40mA
-0.00	3.97nA	7.41nA	12.45nA
0.10	8.11mA	5.36mA	9.30mA
0.20	15.76mA	10.38mA	18.18mA
0.30	22.98mA	15.05mA	26.64mA
0.40	29.76mA	19.40mA	34.68mA
0.50	36.11mA	23.42mA	42.32mA
0.60	42.04mA	27.11mA	49.54mA
0.70	47.55mA	30.50mA	56.36mA
0.80	52.65mA	33.58mA	62.78mA
0.90	57.35mA	36.36mA	68.80mA
1.00	61.64mA	38.84mA	74.42mA
1.10	65.54mA	41.04mA	79.65mA
1.20	69.06mA	42.96mA	84.48mA
1.30	72.18mA	44.61mA	88.92mA
1.40	74.93mA	45.99mA	92.97mA
1.50	77.31mA	47.12mA	96.63mA
1.60	79.32mA	48.01mA	99.91mA
1.70	80.95mA	48.68mA	0.10A
1.80	82.19mA	49.17mA	0.11A
1.90	83.08mA	49.54mA	0.11A

2.00	83.74mA	49.82mA	0.11A
2.10	84.23mA	50.06mA	0.11A
2.20	84.61mA	50.25mA	0.11A
2.30	84.93mA	50.42mA	0.11A
2.40	85.20mA	50.57mA	0.11A
2.50	85.43mA	50.70mA	0.11A
2.60	85.64mA	50.82mA	0.11A
2.70	85.83mA	50.93mA	0.11A
2.80	86.01mA	51.03mA	0.11A
2.90	86.17mA	51.13mA	0.11A
3.00	86.32mA	51.22mA	0.11A
3.10	86.47mA	51.31mA	0.11A
3.20	86.61mA	51.40mA	0.11A
3.30	86.75mA	51.50mA	0.11A
3.40	86.88mA	51.73mA	0.12A
3.50	87.01mA	52.32mA	0.12A
3.60	87.15mA	53.14mA	0.12A
3.70	87.30mA	54.01mA	0.12A
3.80	87.47mA	54.42mA	0.12A
3.90	87.77mA	52.16mA	0.12A
4.00	88.66mA	52.28mA	0.12A
4.10	90.00mA	52.42mA	0.12A
4.20	91.29mA	52.58mA	0.12A
4.30	89.03mA	52.77mA	0.12A
4.50	89.65mA	53.24mA	0.12A
4.70	90.63mA	53.86mA	0.12A
4.90	91.94mA	54.68mA	0.12A
5.10	93.62mA	55.72mA	0.12A
5.30	95.73mA	57.02mA	0.13A
5.50	98.29mA	58.58mA	0.13A
5.70	0.10A	60.42mA	0.13A
5.90	0.10A	62.54mA	0.14A
6.10	0.11A	64.92mA	0.14A
6.60	0.12A	71.81mA	0.15A

|

[Pullup]

voltage	I(typ)	I(min)	I(max)
-3.30	0.22A	0.16A	0.25A
-3.10	0.21A	0.16A	0.24A
-2.90	0.20A	0.15A	0.23A
-2.70	0.19A	0.14A	0.22A
-2.50	0.18A	0.14A	0.21A
-2.30	0.17A	0.13A	0.20A
-2.10	0.16A	0.12A	0.18A
-1.90	0.15A	0.11A	0.17A
-1.70	0.14A	0.10A	0.16A
-1.50	0.12A	90.13mA	0.14A
-1.00	92.59mA	62.48mA	0.11A
-0.90	84.26mA	56.95mA	97.88mA
-0.80	75.03mA	54.36mA	87.19mA

-0.70	65.60mA	47.69mA	76.45mA
-0.60	56.28mA	40.63mA	66.08mA
-0.50	47.19mA	33.52mA	55.62mA
-0.40	37.96mA	26.49mA	44.89mA
-0.30	28.58mA	19.70mA	33.93mA
-0.20	19.09mA	13.03mA	22.76mA
-0.10	9.54mA	6.45mA	11.43mA
0.00	0.17uA	0.16uA	0.19uA
0.10	-9.23mA	-6.17mA	-11.15mA
0.20	-17.95mA	-11.99mA	-21.75mA
0.30	-26.16mA	-17.46mA	-31.79mA
0.40	-33.86mA	-22.57mA	-41.28mA
0.50	-41.07mA	-27.35mA	-50.24mA
0.60	-47.79mA	-31.77mA	-58.67mA
0.70	-54.04mA	-35.86mA	-66.58mA
0.80	-59.82mA	-39.62mA	-73.98mA
0.90	-65.13mA	-43.05mA	-80.88mA
1.00	-69.99mA	-46.15mA	-87.29mA
1.10	-74.41mA	-48.92mA	-93.21mA
1.20	-78.38mA	-51.38mA	-98.65mA
1.30	-81.93mA	-53.52mA	-0.10A
1.40	-85.05mA	-55.36mA	-0.11A
1.50	-87.75mA	-56.88mA	-0.11A
1.60	-90.05mA	-58.12mA	-0.12A
1.70	-91.96mA	-59.09mA	-0.12A
1.80	-93.52mA	-59.84mA	-0.12A
1.90	-94.78mA	-60.43mA	-0.12A
2.00	-95.80mA	-60.92mA	-0.13A
2.10	-96.66mA	-61.35mA	-0.13A
2.20	-97.39mA	-61.72mA	-0.13A
2.30	-98.03mA	-62.06mA	-0.13A
2.40	-98.58mA	-62.37mA	-0.13A
2.50	-99.08mA	-62.65mA	-0.13A
2.60	-99.52mA	-62.91mA	-0.13A
2.70	-99.92mA	-63.15mA	-0.13A
2.80	-0.10A	-63.37mA	-0.13A
2.90	-0.10A	-63.58mA	-0.13A
3.00	-0.10A	-63.78mA	-0.13A
3.10	-0.10A	-63.96mA	-0.14A
3.20	-0.10A	-64.14mA	-0.14A
3.30	-0.10A	-64.33mA	-0.14A
3.40	-0.10A	-64.95mA	-0.14A
3.50	-0.10A	-72.61mA	-0.14A
3.60	-0.10A	-0.17A	-0.14A
3.70	-0.10A	-0.97A	-0.14A
3.80	-0.10A	-2.72A	-0.14A
3.90	-0.11A	-4.50A	-0.14A
4.00	-0.12A	-6.28A	-0.14A
4.10	-0.34A	-8.06A	-0.14A
4.20	-1.90A	-9.85A	-0.14A
4.30	-3.94A	-11.62A	-0.15A

4.50	-8.02A	-15.19A	-1.20A
4.70	-12.10A	-18.75A	-5.43A
4.90	-16.18A	-22.31A	-9.67A
5.10	-20.27A	-25.88A	-13.90A
5.30	-24.35A	-29.44A	-18.14A
5.50	-28.43A	-33.00A	-22.38A
5.70	-32.51A	-36.56A	-26.62A
5.90	-36.60A	-40.13A	-30.86A
6.10	-40.68A	-43.69A	-35.09A
6.60	-50.89A	-52.59A	-45.69A

|
[GND_clamp]

voltage	I(typ)	I(min)	I(max)
-3.30	-50.75A	-47.17A	-51.87A
-3.20	-48.72A	-45.39A	-49.75A
-3.10	-46.68A	-43.61A	-47.63A
-3.00	-44.64A	-41.83A	-45.52A
-2.90	-42.60A	-40.05A	-43.40A
-2.80	-40.56A	-38.27A	-41.29A
-2.70	-38.52A	-36.49A	-39.17A
-2.60	-36.48A	-34.71A	-37.05A
-2.50	-34.44A	-32.93A	-34.94A
-2.40	-32.40A	-31.15A	-32.82A
-2.30	-30.36A	-29.37A	-30.70A
-2.20	-28.32A	-27.59A	-28.58A
-2.10	-26.28A	-25.81A	-26.47A
-2.00	-24.24A	-24.03A	-24.35A
-1.90	-22.20A	-22.25A	-22.23A
-1.80	-20.16A	-20.47A	-20.11A
-1.70	-18.12A	-18.68A	-18.00A
-1.60	-16.08A	-16.90A	-15.88A
-1.50	-14.04A	-15.12A	-13.76A
-1.40	-12.00A	-13.34A	-11.64A
-1.30	-9.96A	-11.56A	-9.53A
-1.20	-7.92A	-9.78A	-7.41A
-1.10	-5.88A	-8.00A	-5.29A
-1.00	-3.84A	-6.22A	-3.18A
-0.90	-1.80A	-4.44A	-1.07A
-0.80	-0.23A	-2.65A	-71.53mA
-0.70	-13.26mA	-0.90A	-13.93mA
-0.60	-2.23mA	-0.10A	-6.08mA
-0.50	-0.34mA	-7.99mA	-1.62mA
-0.40	-28.68uA	-0.48mA	-0.18mA
-0.30	-1.65uA	-27.22uA	-10.18uA
-0.20	-0.15uA	-1.61uA	-0.42uA
-0.10	-86.50nA	-0.17uA	-0.11uA
-0.00	-76.61nA	-77.36nA	-91.73nA
0.10	-68.52nA	-64.82nA	-83.30nA
0.20	-60.47nA	-56.49nA	-75.01nA
0.30	-52.43nA	-48.39nA	-66.73nA

0.40	-44.39nA	-40.30nA	-58.46nA
0.50	-36.35nA	-32.21nA	-50.19nA
0.60	-28.31nA	-24.12nA	-41.93nA
0.70	-20.27nA	-16.03nA	-33.68nA
0.80	-12.24nA	-7.94nA	-25.42nA
0.90	-4.20nA	0.15nA	-17.17nA
1.00	3.83nA	8.23nA	-8.92nA
1.10	11.86nA	16.32nA	-0.67nA
1.20	19.89nA	24.41nA	7.58nA
1.30	27.92nA	32.50nA	15.84nA
1.40	35.95nA	40.59nA	24.10nA
1.50	43.98nA	48.68nA	32.36nA
1.60	52.00nA	56.77nA	40.64nA
1.70	60.02nA	64.85nA	48.92nA
1.80	68.04nA	72.94nA	57.21nA
1.90	76.05nA	81.03nA	65.52nA
2.00	84.05nA	89.12nA	73.85nA
2.10	92.04nA	97.20nA	82.20nA
2.20	100.00nA	0.11uA	90.59nA
2.30	0.11uA	0.11uA	99.01nA
2.40	0.12uA	0.12uA	0.11uA
2.50	0.12uA	0.12uA	0.12uA
2.60	0.13uA	0.13uA	0.12uA
2.70	0.13uA	0.13uA	0.13uA
2.80	0.14uA	0.13uA	0.14uA
2.90	0.14uA	0.14uA	0.15uA
3.00	0.15uA	0.15uA	0.15uA
3.10	0.15uA	0.17uA	0.16uA
3.20	0.15uA	0.56uA	0.16uA
3.30	0.16uA	0.19uA	0.17uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-3.30	0.37uA	0.37uA	0.40uA
-3.20	0.37uA	0.36uA	0.39uA
-3.10	0.36uA	0.36uA	0.39uA
-3.00	0.35uA	0.35uA	0.38uA
-2.90	0.35uA	0.34uA	0.37uA
-2.80	0.34uA	0.34uA	0.37uA
-2.70	0.33uA	0.33uA	0.36uA
-2.60	0.33uA	0.33uA	0.36uA
-2.50	0.32uA	0.32uA	0.35uA
-2.40	0.32uA	0.31uA	0.34uA
-2.30	0.31uA	0.31uA	0.34uA
-2.20	0.30uA	0.30uA	0.33uA
-2.10	0.30uA	0.29uA	0.32uA
-2.00	0.29uA	0.29uA	0.32uA
-1.90	0.28uA	0.28uA	0.31uA
-1.80	0.28uA	0.28uA	0.30uA
-1.70	0.27uA	0.27uA	0.30uA

-1.60	0.27uA	0.26uA	0.29uA
-1.50	0.26uA	0.26uA	0.29uA
-1.40	0.25uA	0.25uA	0.28uA
-1.30	0.25uA	0.25uA	0.27uA
-1.20	0.24uA	0.24uA	0.27uA
-1.10	0.24uA	0.23uA	0.26uA
-1.00	0.23uA	0.23uA	0.25uA
-0.90	0.22uA	0.22uA	0.25uA
-0.80	0.22uA	0.22uA	0.24uA
-0.70	0.21uA	0.21uA	0.24uA
-0.60	0.21uA	0.20uA	0.23uA
-0.50	0.20uA	0.20uA	0.22uA
-0.40	0.20uA	0.19uA	0.22uA
-0.30	0.19uA	0.19uA	0.21uA
-0.20	0.48mA	0.56uA	0.72uA
-0.10	0.16uA	0.17uA	0.18uA
0.00	0.16uA	0.15uA	0.18uA

|
[Ramp]

variable	typ	min	max
dV/dt_r	1.54/2.19n	1.20/2.87n	1.77/2.14n
dV/dt_f	1.52/3.15n	1.15/4.45n	1.73/3.01n

R_load = 50.00
|
[Rising Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.70uV	0.93uV	0.69uV
0.20nS	0.46uV	0.77uV	0.000V
0.40nS	-5.77uV	-1.75uV	11.67uV
0.60nS	-0.27mV	-5.10uV	-2.79mV
0.80nS	-2.96mV	26.03uV	-6.12mV
1.00nS	-3.62mV	-5.61uV	32.64mV
1.20nS	19.35mV	-0.80mV	81.12mV
1.40nS	46.31mV	-3.19mV	0.11V
1.60nS	79.98mV	-6.88mV	0.16V
1.80nS	0.12V	-0.22mV	0.21V
2.00nS	0.16V	21.89mV	0.27V
2.20nS	0.20V	48.68mV	0.33V
2.40nS	0.26V	76.62mV	0.41V
2.60nS	0.32V	0.11V	0.49V
2.80nS	0.42V	0.16V	0.61V
3.00nS	0.51V	0.20V	0.73V
3.20nS	0.58V	0.24V	0.82V

3.40nS	0.71V	0.30V	0.99V
3.60nS	0.85V	0.36V	1.17V
3.80nS	1.01V	0.45V	1.36V
4.00nS	1.18V	0.54V	1.56V
4.20nS	1.38V	0.67V	1.81V
4.40nS	1.57V	0.81V	2.03V
4.60nS	1.69V	0.89V	2.16V
4.80nS	1.79V	0.96V	2.27V
5.00nS	1.91V	1.06V	2.40V
5.20nS	2.03V	1.15V	2.52V
5.40nS	2.14V	1.26V	2.61V
5.60nS	2.24V	1.35V	2.70V
5.80nS	2.28V	1.40V	2.74V
6.00nS	2.31V	1.45V	2.77V
6.20nS	2.36V	1.51V	2.80V
6.40nS	2.39V	1.56V	2.83V
6.60nS	2.41V	1.61V	2.85V
6.80nS	2.43V	1.66V	2.86V
7.00nS	2.45V	1.70V	2.87V
7.20nS	2.46V	1.74V	2.88V
7.40nS	2.48V	1.78V	2.89V
7.60nS	2.49V	1.82V	2.90V
7.80nS	2.50V	1.84V	2.91V
8.00nS	2.51V	1.86V	2.91V
8.20nS	2.52V	1.88V	2.92V
8.40nS	2.52V	1.90V	2.92V
8.60nS	2.53V	1.92V	2.93V
8.80nS	2.54V	1.93V	2.93V
9.00nS	.54V	1.95V	2.93V
9.20nS	2.55V	1.96V	2.94V
9.40nS	2.55V	1.97V	2.94V
9.60nS	2.56V	1.99V	2.94V
9.80nS	2.56V	2.00V	2.95V
10.00nS	2.57V	2.00V	2.95V

|

[Rising Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	0.76V	1.03V	0.72V
0.20nS	0.76V	1.03V	0.72V
0.40nS	0.76V	1.03V	0.72V
0.60nS	0.76V	1.03V	0.72V
0.80nS	0.77V	1.03V	0.73V
1.00nS	0.81V	1.03V	0.82V
1.20nS	0.90V	1.03V	0.93V

1.40nS	0.98V	1.04V	1.02V
1.60nS	1.10V	1.11V	1.13V
1.80nS	1.22V	1.21V	1.26V
2.00nS	1.36V	1.33V	1.42V
2.20nS	1.53V	1.46V	1.58V
2.40nS	1.72V	1.60V	1.80V
2.60nS	1.93V	1.75V	2.04V
2.80nS	2.23V	1.97V	2.36V
3.00nS	2.48V	2.16V	2.62V
3.20nS	2.66V	2.30V	2.82V
3.40nS	2.85V	2.49V	3.04V
3.60nS	2.97V	2.63V	3.19V
3.80nS	3.09V	2.73V	3.29V
4.00nS	3.14V	2.83V	3.36V
4.20nS	3.19V	2.89V	3.42V
4.40nS	3.23V	2.94V	3.47V
4.60nS	3.25V	2.96V	3.50V
4.80nS	3.27V	2.97V	3.52V
5.00nS	3.28V	2.98V	3.54V
5.20nS	.29V	2.99V	3.56V
5.40nS	3.29V	2.99V	3.57V
5.60nS	3.30V	3.00V	3.58V
5.80nS	3.30V	3.00V	3.59V
6.00nS	3.30V	3.00V	3.59V
6.20nS	3.30V	3.00V	3.60V
6.40nS	3.30V	3.00V	3.60V
6.60nS	3.30V	3.00V	3.60V
6.80nS	3.30V	3.00V	3.60V
7.00nS	3.30V	3.00V	3.60V
7.20nS	3.30V	3.00V	3.60V
7.40nS	3.30V	3.00V	3.60V
7.60nS	3.30V	3.00V	3.60V
7.80nS	3.30V	3.00V	3.60V
8.00nS	3.30V	3.00V	3.60V
8.20nS	3.30V	3.00V	3.60V
8.40nS	3.30V	3.00V	3.60V
8.60nS	3.30V	3.00V	3.60V
8.80nS	3.30V	3.00V	3.60V
9.00nS	3.30V	3.00V	3.60V
9.20nS	3.30V	3.00V	3.60V
9.40nS	3.30V	3.00V	3.60V
9.60nS	3.30V	3.00V	3.60V
9.80nS	3.30V	3.00V	3.60V
10.00nS	3.30V	3.00V	3.60V

|

[Falling Waveform]
R_fixture = 50.00
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
L_fixture = 0.000H

C_fixture = 0.000F

time	V(typ)	V(min)	V(max)
0.000S	2.62V	2.12V	2.99V
0.20nS	2.62V	2.12V	2.99V
0.40nS	2.62V	2.12V	2.99V
0.60nS	2.62V	2.12V	2.96V
0.80nS	2.60V	2.12V	2.85V
1.00nS	2.50V	2.12V	2.72V
1.20nS	2.37V	2.11V	2.59V
1.40nS	2.29V	2.09V	2.50V
1.60nS	2.17V	2.04V	2.36V
1.80nS	2.04V	1.96V	2.20V
2.00nS	1.89V	1.85V	2.00V
2.20nS	1.71V	1.74V	1.75V
2.40nS	1.50V	1.63V	1.48V
2.60nS	1.28V	1.50V	1.24V
2.80nS	1.01V	1.33V	1.01V
3.00nS	0.82V	1.17V	0.82V
3.20nS	0.72V	1.04V	0.75V
3.40nS	0.61V	0.87V	0.65V
3.60nS	0.51V	0.72V	0.57V
3.80nS	0.44V	0.60V	0.50V
4.00nS	0.38V	0.49V	0.44V
4.20nS	0.32V	0.40V	0.38V
4.40nS	0.26V	0.32V	0.32V
4.60nS	0.23V	0.28V	0.29V
4.80nS	0.21V	0.25V	0.26V
5.00nS	0.17V	0.21V	0.23V
5.20nS	0.15V	0.18V	0.20V
5.40nS	0.12V	0.14V	0.17V
5.60nS	93.14mV	0.11V	0.14V
5.80nS	80.86mV	94.78mV	0.12V
6.00nS	68.57mV	80.67mV	0.11V
6.20nS	55.24mV	65.96mV	90.13mV
6.40nS	43.92mV	51.39mV	74.96mV
6.60nS	33.33mV	40.71mV	61.03mV
6.80nS	25.91mV	31.19mV	50.31mV
7.00nS	18.81mV	22.83mV	39.65mV
7.20nS	13.52mV	17.13mV	31.61mV
7.40nS	8.40mV	10.61mV	22.62mV
7.60nS	4.73mV	6.73mV	15.75mV
7.80nS	3.46mV	4.67mV	12.43mV
8.00nS	2.19mV	3.16mV	9.14mV
8.20nS	1.26mV	2.23mV	6.37mV
8.40nS	0.84mV	1.32mV	4.12mV
8.60nS	0.49mV	0.95mV	2.29mV
8.80nS	0.41mV	0.74mV	1.55mV
9.00nS	0.35mV	0.58mV	0.81mV
9.20nS	0.31mV	0.51mV	0.53mV
9.40nS	0.28mV	0.45mV	0.39mV

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  9.60nS      0.24mV      0.40mV      0.27mV
  9.80nS      0.22mV      0.36mV      0.24mV
  10.00nS     0.20mV      0.32mV      0.21mV
|
[Falling Waveform]
R_fixture = 50.00
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
L_fixture = 0.000H
C_fixture = 0.000F
|  time       V(typ)      V(min)      V(max)
|
  0.000S      3.30V       3.00V       3.60V
  0.20nS      3.30V       3.00V       3.60V
  0.40nS      3.30V       3.00V       3.60V
  0.60nS      3.30V       3.00V       3.59V
  0.80nS      3.30V       3.00V       3.52V
  1.00nS      3.25V       3.00V       3.44V
  1.20nS      3.18V       3.00V       3.37V
  1.40nS      3.14V       3.00V       3.32V
  1.60nS      3.09V       3.00V       3.24V
  1.80nS      3.03V       2.97V       3.16V
  2.00nS      2.96V       2.92V       3.07V
  2.20nS      2.88V       2.88V       2.98V
  2.40nS      2.80V       2.84V       2.88V
  2.60nS      2.72V       2.80V       2.77V
  2.80nS      2.60V       2.74V       2.64V
  3.00nS      2.51V       2.68V       2.54V
  3.20nS      2.44V       2.64V       2.46V
  3.40nS      2.34V       2.58V       2.34V
  3.60nS      2.25V       2.52V       2.22V
  3.80nS      2.15V       2.46V       2.08V
  4.00nS      2.05V       2.39V       1.92V
  4.20nS      1.93V       2.32V       1.74V
  4.40nS      1.81V       2.24V       1.58V
  4.60nS      1.73V       2.19V       1.50V
  4.80nS      1.65V       2.15V       1.42V
  5.00nS      1.53V       2.09V       1.34V
  5.20nS      1.43V       2.04V       1.26V
  5.40nS      1.32V       1.97V       1.18V
  5.60nS      1.22V       1.91V       1.11V
  5.80nS      1.18V       1.87V       1.07V
  6.00nS      1.13V       1.84V       1.03V
  6.20nS      1.08V       1.79V       0.99V
  6.40nS      1.03V       1.75V       0.95V
  6.60nS      0.99V       1.70V       0.92V
  6.80nS      0.96V       1.66V       0.89V
  7.00nS      0.93V       1.63V       0.87V
  7.20nS      0.90V       1.59V       0.84V
  7.40nS      0.87V       1.53V       0.82V
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  7.60nS      0.84V          1.47V          0.80V
  7.80nS      0.83V          1.44V          0.78V
  8.00nS      0.82V          1.40V          0.78V
  8.20nS      0.81V          1.35V          0.76V
  8.40nS      0.80V          1.30V          0.75V
  8.60nS      0.79V          1.26V          0.75V
  8.80nS      0.78V          1.23V          0.74V
  9.00nS      0.78V          1.19V          0.73V
  9.20nS      0.78V          1.17V          0.73V
  9.40nS      0.77V          1.14V          0.73V
  9.60nS      0.77V          1.12V          0.72V
  9.80nS      0.77V          1.10V          0.72V
  10.00nS     0.77V          1.08V          0.72V
|
| End [Model] prt24dgz
|
|********************************************************************************
|                          Model pdusdgz
|********************************************************************************
|
[Model]          pdusdgz
Model_type       Input
Polarity         Non-Inverting
Vinl =  0.000V
Vinh =   3.30V
C_comp                          5.00pF          5.00pF          5.00pF
|
|
[Temperature Range]             25.00           0.12k           0.000
[Pullup Reference]              3.30V           3.00V           3.60V
[Pulldown Reference]            0.000V          0.000V          0.000V
[POWER Clamp Reference]         5.00V           4.50V           5.50V
[GND Clamp Reference]           0.000V          0.000V          0.000V
[GND_clamp]
|  voltage      I(typ)          I(min)          I(max)
|
  -5.00         -64.63A         -59.13A         -66.41A
  -4.80         -61.55A         -56.41A         -63.21A
  -4.60         -58.47A         -53.69A         -60.01A
  -4.40         -55.39A         -50.97A         -56.81A
  -4.20         -52.31A         -48.25A         -53.61A
  -4.00         -49.23A         -45.53A         -50.41A
  -3.80         -46.15A         -42.81A         -47.21A
  -3.60         -43.07A         -40.09A         -44.01A
  -3.40         -39.99A         -37.37A         -40.81A
  -3.20         -36.91A         -34.65A         -37.61A
  -3.00         -33.82A         -31.94A         -34.41A
  -2.80         -30.73A         -29.22A         -31.22A
  -2.60         -27.64A         -26.51A         -28.02A
  -2.40         -24.56A         -23.79A         -24.82A
  -2.20         -21.47A         -21.08A         -21.62A
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-2.00	-18.38A	-18.36A	-18.42A
-1.80	-15.29A	-15.64A	-15.22A
-1.60	-12.20A	-12.93A	-12.03A
-1.40	-9.12A	-10.21A	-8.83A
-1.20	-6.03A	-7.50A	-5.63A
-1.00	-2.94A	-4.78A	-2.43A
-0.80	-0.20A	-2.07A	-64.17mA
-0.60	-1.85mA	-96.40mA	-4.85mA
-0.40	-83.24uA	-0.50mA	-0.23mA
-0.20	-60.52uA	-36.82uA	-86.29uA
-0.00	-60.40uA	-35.33uA	-85.95uA
0.20	-60.32uA	-35.27uA	-85.85uA
0.40	-60.23uA	-35.20uA	-85.73uA
0.60	-60.11uA	-35.13uA	-85.57uA
0.80	-59.96uA	-35.03uA	-85.37uA
1.00	-59.74uA	-34.91uA	-85.08uA
1.20	-59.32uA	-34.50uA	-84.56uA
1.40	-58.35uA	-33.59uA	-83.44uA
1.60	-56.47uA	-31.92uA	-81.36uA
1.80	-53.57uA	-29.25uA	-78.20uA
2.00	-49.55uA	-7.60uA	-73.89uA
2.20	-43.70uA	-16.78nA	-68.43uA
2.40	-3.73uA	0.10uA	-61.70uA
2.60	0.10uA	0.11uA	-51.99uA
2.80	0.12uA	0.12uA	-2.43uA
3.00	0.13uA	0.13uA	0.13uA
3.20	0.14uA	0.20uA	0.14uA
3.40	0.15uA	0.15uA	0.15uA
3.60	0.16uA	96.30nA	0.16uA
3.80	0.17uA	43.50nA	0.17uA
4.00	0.18uA	-9.30nA	0.18uA
4.20	0.18uA	62.10nA	0.19uA
4.40	0.19uA	-0.11uA	0.20uA
4.60	0.20uA	-0.17uA	0.21uA
4.80	0.21uA	-0.22uA	0.22uA
5.00	0.22uA	-0.27uA	0.23uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	0.61uA	0.59uA	0.65uA
-4.90	0.60uA	0.58uA	0.65uA
-4.80	0.59uA	0.58uA	0.64uA
-4.70	0.59uA	0.57uA	0.63uA
-4.60	0.58uA	0.56uA	0.63uA
-4.50	0.57uA	0.56uA	0.62uA
-4.40	0.56uA	0.55uA	0.61uA
-4.30	0.56uA	0.54uA	0.60uA
-4.20	0.55uA	0.54uA	0.60uA
-4.10	0.54uA	0.53uA	0.59uA
-4.00	0.54uA	0.52uA	0.58uA

-3.90	0.53uA	0.52uA	0.58uA
-3.80	0.52uA	0.51uA	0.57uA
-3.70	0.52uA	0.50uA	0.56uA
-3.60	0.51uA	0.50uA	0.56uA
-3.50	0.50uA	0.49uA	0.55uA
-3.40	0.50uA	0.48uA	0.54uA
-3.30	0.49uA	0.48uA	0.53uA
-3.20	0.48uA	0.47uA	0.53uA
-3.10	0.48uA	0.46uA	0.52uA
-3.00	0.47uA	0.46uA	0.51uA
-2.90	0.46uA	0.45uA	0.51uA
-2.80	0.46uA	0.44uA	0.50uA
-2.70	0.45uA	0.44uA	0.49uA
-2.60	0.44uA	0.43uA	0.49uA
-2.50	0.44uA	0.42uA	0.48uA
-2.40	0.43uA	0.41uA	0.47uA
-2.30	0.42uA	0.41uA	0.46uA
-2.20	0.42uA	0.40uA	0.46uA
-2.10	0.41uA	0.39uA	0.45uA
-2.00	0.40uA	0.39uA	0.44uA
-1.90	0.39uA	0.38uA	0.44uA
-1.80	0.39uA	0.37uA	0.43uA
-1.70	0.38uA	0.37uA	0.42uA
-1.60	0.37uA	0.36uA	0.42uA
-1.50	0.37uA	0.35uA	0.41uA
-1.40	0.36uA	0.35uA	0.40uA
-1.30	0.35uA	0.34uA	0.39uA
-1.20	0.35uA	0.33uA	0.39uA
-1.10	0.34uA	0.33uA	0.38uA
-1.00	0.33uA	0.32uA	0.37uA
-0.90	0.33uA	0.31uA	0.37uA
-0.80	0.32uA	0.31uA	0.36uA
-0.70	0.31uA	0.30uA	0.35uA
-0.60	0.31uA	0.29uA	0.35uA
-0.50	0.30uA	0.29uA	0.34uA
-0.40	0.29uA	0.28uA	0.33uA
-0.30	0.29uA	0.27uA	0.32uA
-0.20	0.28uA	0.27uA	0.32uA
-0.10	0.27uA	0.26uA	0.31uA
0.00	0.27uA	0.25uA	0.30uA

```
|
| End [Model] pdusdgz
|
|*******************************************************************************
|                          Model pdddgz
|*******************************************************************************
|
[Model]          pdddgz
Model_type       Input
Polarity         Non-Inverting
Vinl =  0.000V
```

Vinh = 3.30V

C_comp	5.00pF	5.00pF	5.00pF
|			
|			
[Temperature Range]	25.00	0.12k	0.000
[Pullup Reference]	3.30V	3.00V	3.60V
[Pulldown Reference]	0.000V	0.000V	0.000V
[POWER Clamp Reference]	5.00V	4.50V	5.50V
[GND Clamp Reference] \	0.000V	0.000V	0.000V
[GND_clamp]			
| voltage	I(typ)	I(min)	I(max)
|			
-5.00	-64.63A	-59.13A	-66.41A
-4.80	-61.55A	-56.41A	-63.21A
-4.60	-58.47A	-53.69A	-60.01A
-4.40	-55.39A	-50.97A	-56.81A
-4.20	-52.31A	-48.25A	-53.61A
-4.00	-49.23A	-45.53A	-50.41A
-3.80	-46.15A	-42.81A	-47.21A
-3.60	-43.07A	-40.09A	-44.01A
-3.40	-39.99A	-37.37A	-40.81A
-3.20	-36.91A	-34.65A	-37.61A
-3.00	-33.82A	-31.94A	-34.41A
-2.80	-30.73A	-29.22A	-31.22A
-2.60	-27.64A	-26.51A	-28.02A
-2.40	-24.56A	-23.79A	-24.82A
-2.20	-21.47A	-21.08A	-21.62A
-2.00	-18.38A	-18.36A	-18.42A
-1.80	-15.29A	-15.64A	-15.22A
-1.60	-12.20A	-12.93A	-12.03A
-1.40	-9.12A	-10.21A	-8.83A
-1.20	-6.03A	-7.50A	-5.63A
-1.00	-2.94A	-4.78A	-2.43A
-0.80	-0.20A	-2.07A	-64.21mA
-0.60	-1.89mA	-96.41mA	-4.91mA
-0.40	-85.69uA	-0.50mA	-0.24mA
-0.20	-27.91uA	-14.61uA	-42.88uA
-0.00	-87.50nA	-88.83nA	-0.10uA
0.20	18.71uA	7.31uA	32.27uA
0.40	29.18uA	10.24uA	54.12uA
0.60	32.49uA	10.66uA	65.78uA
0.80	33.06uA	10.78uA	69.33uA
1.00	33.29uA	10.85uA	70.16uA
1.20	33.44uA	10.91uA	70.54uA
1.40	33.56uA	10.96uA	70.78uA
1.60	33.66uA	11.01uA	70.98uA
1.80	33.76uA	11.06uA	71.15uA
2.00	33.85uA	11.10uA	71.30uA
2.20	33.94uA	11.12uA	71.44uA
2.40	33.99uA	11.13uA	71.59uA
2.60	34.01uA	11.14uA	71.74uA

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  2.80          34.02uA        11.15uA        71.82uA
  3.00          34.03uA        11.16uA        71.84uA
  3.20          34.04uA        11.25uA        71.85uA
  3.40          34.06uA        11.17uA        71.87uA
  3.60          34.08uA        11.09uA        71.89uA
  3.80          34.10uA        11.01uA        71.91uA
  4.00          34.12uA        10.93uA        71.93uA
  4.20          34.14uA        10.85uA        71.95uA
  4.40          34.16uA        10.77uA        71.97uA
  4.60          34.18uA        10.69uA        71.99uA
  4.80          34.20uA        10.61uA        72.01uA
  5.00          34.22uA        10.53uA        72.03uA
|
[POWER_clamp]
| voltage       I(typ)          I(min)         I(max)
|
  -5.00         48.19uA        16.29uA        95.53uA
  -4.90         47.87uA        16.17uA        95.03uA
  -4.80         47.55uA          16.05uA          94.53uA
  -4.70         47.23uA          15.93uA          94.03uA
  -4.60         46.91uA          15.81uA          93.53uA
  -4.50         46.59uA          15.69uA          93.03uA
  -4.40         46.27uA          15.57uA          92.53uA
  -4.30         45.95uA          15.45uA          92.03uA
  -4.20         45.63uA          15.33uA          91.53uA
  -4.10         45.31uA          15.21uA          91.03uA
  -4.00         44.99uA          15.09uA          90.53uA
  -3.90         44.67uA          14.97uA          90.03uA
  -3.80         44.35uA          14.85uA          89.53uA
  -3.70         44.03uA          14.73uA          89.03uA
  -3.60         43.71uA          14.61uA          88.53uA
  -3.50         43.39uA          14.49uA          88.03uA
  -3.40         43.07uA          14.37uA          87.53uA
  -3.30         42.75uA          14.25uA          87.03uA
  -3.20         42.43uA          14.13uA          86.53uA
  -3.10         42.11uA          14.01uA          86.03uA
  -3.00         41.79uA          13.89uA          85.53uA
  -2.90         41.47uA          13.77uA          85.03uA
  -2.80         41.15uA          13.65uA          84.53uA
  -2.70         40.83uA          13.53uA          84.03uA
  -2.60         40.51uA          13.41uA          83.53uA
  -2.50         40.19uA          13.29uA          83.03uA
  -2.40         39.87uA          13.17uA          82.53uA
  -2.30         39.55uA          13.05uA          82.03uA
  -2.20         39.23uA          12.93uA          81.53uA
  -2.10         38.91uA          12.81uA          81.03uA
  -2.00         38.59uA          12.69uA          80.53uA
  -1.90         38.27uA          12.57uA          80.03uA
  -1.80         37.95uA          12.45uA          79.53uA
  -1.70         37.63uA          12.33uA          79.03uA
  -1.60         37.31uA          12.22uA          78.53uA
```

```
  -1.50          36.99uA          12.11uA          78.03uA
  -1.40          36.68uA          12.01uA          77.53uA
  -1.30          36.38uA          11.92uA          77.03uA
  -1.20          36.11uA          11.84uA          76.53uA
  -1.10          35.86uA          11.76uA          76.03uA
  -1.00          35.63uA          11.69uA          75.53uA
  -0.90          35.41uA          11.63uA          75.06uA
  -0.80          35.22uA          11.57uA          74.63uA
  -0.70          35.05uA          11.52uA          74.24uA
  -0.60          34.90uA          11.48uA          73.89uA
  -0.50          34.77uA          11.44uA          73.58uA
  -0.40          34.65uA        11.41uA        73.30uA
  -0.30          34.55uA        11.38uA        73.06uA
  -0.20          34.47uA        11.35uA        72.86uA
  -0.10          34.40uA        11.33uA        72.68uA
   0.00          34.34uA        11.31uA        72.54uA
|
| End [Model] pdddgz
|
|********************************************************************************
|                          Model pdudgz
|********************************************************************************
|
[Model]          pdudgz
Model_type       Input
Polarity         Non-Inverting
Vinl =  0.000V
Vinh =   3.30V
C_comp           5.00pF             5.00pF             5.00pF
|
|
[Temperature Range]       25.00              0.12k              0.000
[Pullup Reference]        3.30V              3.00V              3.60V
[Pulldown Reference]      0.000V             0.000V             0.000V
[POWER Clamp Reference]   5.00V              4.50V              5.50V
[GND Clamp Reference]     0.000V             0.000V             0.000V
[GND_clamp]
| voltage        I(typ)             I(min)             I(max)
|
  -5.00          -64.63A            -59.13A            -66.41A
  -4.80          -61.55A            -56.41A            -63.21A
  -4.60          -58.47A            -53.69A            -60.01A
  -4.40          -55.39A            -50.97A            -56.81A
  -4.20          -52.31A            -48.25A            -53.61A
  -4.00          -49.23A            -45.53A            -50.41A
  -3.80          -46.15A            -42.81A            -47.21A
  -3.60          -43.07A            -40.09A            -44.01A
  -3.40          -39.99A            -37.37A            -40.81A
  -3.20          -36.91A            -34.65A            -37.61A
  -3.00          -33.82A            -31.94A            -34.41A
  -2.80          -30.73A            -29.22A            -31.22A
```

-2.60	-27.64A	-26.51A	-28.02A
-2.40	-24.56A	-23.79A	-24.82A
-2.20	-21.47A	-21.08A	-21.62A
-2.00	-18.38A	-18.36A	-18.42A
-1.80	-15.29A	-15.64A	-15.22A
-1.60	-12.20A	-12.93A	-12.03A
-1.40	-9.12A	-10.21A	-8.83A
-1.20	-6.03A	-7.50A	-5.63A
-1.00	-2.94A	-4.78A	-2.43A
-0.80	-0.20A	-2.07A	-64.17mA
-0.60	-1.85mA	-96.40mA	-4.85mA
-0.40	-83.24uA	-0.50mA	-0.23mA
-0.20	-60.52uA	-36.82uA	-86.29uA
-0.00	-60.40uA	-35.33uA	-85.95uA
0.20	-60.32uA	-35.27uA	-85.85uA
0.40	-60.23uA	-35.20uA	-85.73uA
0.60	-60.11uA	-35.13uA	-85.57uA
0.80	-59.96uA	-35.03uA	-85.37uA
1.00	-59.74uA	-34.87uA	-85.08uA
1.20	-59.32uA	-34.50uA	-84.56uA
1.40	-58.35uA	-33.59uA	-83.44uA
1.60	-56.47uA	-31.92uA	-81.36uA
1.80	-53.57uA	-29.25uA	-78.20uA
2.00	-49.55uA	-7.60uA	-73.89uA
2.20	-43.70uA	-16.78nA	-68.43uA
2.40	-3.73uA	0.10uA	61.70uA
2.60	0.10uA	0.11uA	51.99uA
2.80	0.12uA	0.12uA	-2.43uA
3.00	0.13uA	0.13uA	0.13uA
3.20	0.14uA	0.20uA	0.14uA
3.40	0.15uA	0.15uA	0.15uA
3.60	0.16uA	96.30nA	0.16uA
3.80	0.17uA	43.50nA	0.17uA
4.00	0.18uA	-9.30nA	0.18uA
4.20	0.18uA	62.10nA	0.19uA
4.40	0.19uA	-0.11uA	0.20uA
4.60	0.20uA	-0.17uA	0.21uA
4.80	0.21uA	-0.22uA	0.22uA
5.00	0.22uA	-0.27uA	0.23uA

|

[POWER_clamp]

voltage	I(typ)	I(min)	I(max)
-5.00	0.61uA	0.59uA	0.65uA
-4.90	0.60uA	0.58uA	0.65uA
-4.80	0.59uA	0.58uA	0.64uA
-4.70	0.59uA	0.57uA	0.63uA
-4.60	0.58uA	0.56uA	0.63uA
-4.50	0.57uA	0.56uA	0.62uA
-4.40	0.56uA	0.55uA	0.61uA
-4.30	0.56uA	0.54uA	0.60uA

```
 -4.20      0.55uA          0.54uA          0.60uA
 -4.10      0.54uA          0.53uA          0.59uA
 -4.00      0.54uA          0.52uA          0.58uA
 -3.90      0.53uA          0.52uA          0.58uA
 -3.80      0.52uA          0.51uA          0.57uA
 -3.70      0.52uA          0.50uA          0.56uA
 -3.60      0.51uA          0.50uA          0.56uA
 -3.50      0.50uA          0.49uA          0.55uA
 -3.40      0.50uA          0.48uA          0.54uA
 -3.30      0.49uA          0.48uA          0.53uA
 -3.20      0.48uA          0.47uA          0.53uA
 -3.10      0.48uA          0.46uA          0.52uA
 -3.00      0.47uA          0.46uA          0.51uA
 -2.90      0.46uA          0.45uA          0.51uA
 -2.80      0.46uA          0.44uA          0.50uA
 -2.70      0.45uA          0.44uA          0.49uA
 -2.60      0.44uA          0.43uA          0.49uA
 -2.50      0.44uA          0.42uA          0.48uA
 -2.40      0.43uA          0.41uA          0.47uA
 -2.30      0.42uA          0.41uA          0.46uA
 -2.20      0.42uA          0.40uA          0.46uA
 -2.10      0.41uA          0.39uA          0.45uA
 -2.00      0.40uA          0.39uA          0.44uA
 -1.90      0.39uA          0.38uA          0.44uA
 -1.80      0.39uA          0.37uA          0.43uA
 -1.70      0.38uA          0.37uA          0.42uA
 -1.60      0.37uA          0.36uA          0.42uA
 -1.50      0.37uA          0.35uA          0.41uA
 -1.40      0.36uA          0.35uA          0.40uA
 -1.30      0.35uA          0.34uA          0.39uA
 -1.20      0.35uA          0.33uA          0.39uA
 -1.10      0.34uA          0.33uA          0.38uA
 -1.00      0.33uA          0.32uA          0.37uA
 -0.90      0.33uA          0.31uA          0.37uA
 -0.80      0.32uA          0.31uA          0.36uA
 -0.70      0.31uA          0.30uA          0.35uA
 -0.60      0.31uA          0.29uA          0.35uA
 -0.50      0.30uA          0.29uA          0.34uA
 -0.40      0.29uA          0.28uA          0.33uA
 -0.30      0.29uA          0.27uA          0.32uA
 -0.20      0.28uA          0.27uA          0.32uA
 -0.10      0.27uA          0.26uA          0.31uA
  0.00      0.27uA          0.25uA          0.30uA
|
| End [Model] pdudgz
|
|*****************************************************************************
|                          Model pdidgz
|*****************************************************************************
|
[Model]         pdidgz
```

Model_type Input
Polarity Non-Inverting
Vinl = 0.000V
Vinh = 3.30V
C_comp 5.00pF 5.00pF 5.00pF
|
|
[Temperature Range] 25.00 0.12k 0.000
[Pullup Reference] 3.30V 3.00V 3.60V
[Pulldown Reference] 0.000V 0.000V 0.000V
[POWER Clamp Reference] 5.00V 4.50V 5.50V
[GND Clamp Reference] 0.000V 0.000V 0.000V
[GND_clamp]
| voltage I(typ) I(min) I(max)
|
-5.00 -64.63A -59.13A -66.41A
-4.80 -61.55A -56.41A -63.21A
-4.60 -58.47A -53.69A -60.01A
-4.40 -55.39A -50.97A -56.81A
-4.20 -52.31A -48.25A -53.61A
-4.00 -49.23A -45.53A -50.41A
-3.80 -46.15A -42.81A -47.21A
-3.60 -43.07A -40.09A -44.01A
-3.40 -39.99A -37.37A -40.81A
-3.20 -36.91A -34.65A -37.61A
-3.00 -33.82A -31.94A -34.41A
-2.80 -30.73A -29.22A -31.22A
-2.60 -27.64A -26.51A -28.02A
-2.40 -24.56A -23.79A -24.82A
-2.20 -21.47A -21.08A -21.62A
-2.00 -18.38A -18.36A -18.42A
-1.80 -15.29A -15.64A -15.22A
-1.60 -12.20A -12.93A -12.03A
-1.40 -9.12A -10.21A -8.83A
-1.20 -6.03A -7.50A -5.63A
-1.00 -2.94A -4.78A -2.43A
-0.80 -0.20A -2.07A -64.14mA
-0.60 -1.79mA -96.39mA -4.77mA
-0.40 -22.83uA -0.47mA -0.14mA
-0.20 -0.15uA -1.56uA -0.37uA
-0.00 -88.71nA -89.34nA -0.11uA
0.20 -72.38nA -68.50nA -88.30nA
0.40 -56.11nA -52.12nA -71.55nA
0.60 -39.84nA -35.76nA -54.82nA
0.80 -23.57nA -19.40nA -38.12nA
1.00 -7.31nA -3.04nA -21.42nA
1.20 8.94nA 13.32nA -4.73nA
1.40 25.19nA 29.68nA 11.97nA
1.60 41.42nA 46.03nA 28.68nA
1.80 57.64nA 62.39nA 45.42nA
2.00 73.83nA 78.74nA 62.20nA

```
   2.20          89.95nA          94.86nA          79.06nA
   2.40          0.11uA           0.11uA           96.02nA
   2.60          0.12uA           0.12uA           0.11uA
   2.80          0.13uA           0.13uA           0.13uA
   3.00          0.14uA           0.14uA           0.14uA
   3.20          0.15uA           0.21uA           0.15uA
   3.40          0.15uA           0.15uA           0.16uA
   3.60          0.16uA           0.10uA           0.17uA
   3.80          0.17uA           47.20nA          0.18uA
   4.00          0.18uA           -5.80nA          0.18uA
   4.20          0.20uA           -0.11uA          0.20uA
   4.60          0.20uA           -0.16uA          0.21uA
   4.80          0.21uA           -0.22uA          0.22uA
   5.00          0.22uA           -0.27uA          0.23uA
|
[POWER_clamp]
| voltage     I(typ)           I(min)           I(max)
|
  -5.00         0.60uA           0.59uA           0.65uA
  -4.90         0.60uA           0.58uA           0.64uA
  -4.80         0.59uA           0.58uA           0.64uA
  -4.70         0.58uA           0.57uA           0.63uA
  -4.60         0.58uA           0.56uA           0.62uA
  -4.50         0.57uA           0.56uA           0.62uA
  -4.40         0.56uA           0.55uA           0.61uA
  -4.30         0.56uA           0.54uA           0.60uA
  -4.20         0.55uA           0.54uA           0.59uA
  -4.10         0.54uA           0.53uA           0.59uA
  -4.00         0.54uA           0.52uA           0.58uA
  -3.90         0.53uA           0.52uA           0.57uA
  -3.80         0.52uA           0.51uA           0.57uA
  -3.70         0.52uA           0.50uA           0.56uA
  -3.60         0.51uA           0.50uA           0.55uA
  -3.50         0.50uA           0.49uA           0.55uA
  -3.40         0.49uA           0.48uA           0.54uA
  -3.30         0.49uA           0.48uA           0.53uA
  -3.20         0.48uA           0.47uA           0.53uA
  -3.10         0.47uA           0.46uA           0.52uA
  -3.00         0.47uA           0.46uA           0.51uA
  -2.90         0.46uA           0.45uA           0.51uA
  -2.80         0.45uA           0.44uA           0.50uA
  -2.70         0.45uA           0.43uA           0.49uA
  -2.60         0.44uA           0.43uA           0.48uA
  -2.50         0.43uA           0.42uA           0.48uA
  -2.40         0.43uA           0.41uA           0.47uA
  -2.30         0.42uA           0.41uA           0.46uA
  -2.20         0.41uA           0.40uA           0.46uA
  -2.10         0.41uA           0.39uA           0.45uA
  -2.00         0.40uA           0.39uA           0.44uA
  -1.90         0.39uA           0.38uA           0.44uA
  -1.80         0.39uA           0.37uA           0.43uA
```

-1.70	0.38uA	0.37uA	0.42uA
-1.60	0.37uA	0.36uA	0.42uA
-1.50	0.37uA	0.35uA	0.41uA
-1.40	0.36uA	0.35uA	0.40uA
-1.30	0.35uA	0.34uA	0.39uA
-1.20	0.35uA	0.33uA	0.39uA
-1.10	0.34uA	0.33uA	0.38uA
-1.00	0.33uA	0.32uA	0.37uA
-0.90	0.33uA	0.31uA	0.37uA
-0.80	0.32uA	0.31uA	0.36uA
-0.70	0.31uA	0.30uA	0.35uA
-0.60	0.31uA	0.29uA	0.35uA
-0.50	0.30uA	0.29uA	0.34uA
-0.40	0.29uA	0.28uA	0.33uA
-0.30	0.29uA	0.27uA	0.33uA
-0.20	0.28uA	0.27uA	0.32uA
-0.10	0.28uA	0.26uA	0.31uA
0.00	0.27uA	0.26uA	0.31uA

|

| End [Model] pdidgz

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Rev. 3
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