

TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOS V-H)

TPC8037-H

High-Efficiency DC-DC Converter Applications
 Notebook PC Applications
 Portable Equipment Applications

- Small footprint due to a small and thin package
- High-speed switching
- Small gate charge: $Q_{SW} = 5.0 \text{ nC (typ.)}$
- Low drain-source ON-resistance: $R_{DS(ON)} = 7.6 \text{ m}\Omega \text{ (typ.)}$
- High forward transfer admittance: $|Y_{fs}| = 36 \text{ S (typ.)}$
- Low leakage current: $I_{DSS} = 10 \text{ }\mu\text{A (max) (}V_{DS} = 30 \text{ V)}$
- Enhancement mode: $V_{th} = 1.5 \text{ to } 2.5 \text{ V (}V_{DS} = 10 \text{ V, } I_D = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	30	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	30	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	12	A
	Pulsed (Note 1)	I_{DP}	48	
Drain power dissipation (t = 10 s) (Note 2a)		P_D	1.9	W
Drain power dissipation (t = 10 s) (Note 2b)		P_D	1.0	W
Single-pulse avalanche energy (Note 3)		E_{AS}	94	mJ
Avalanche current		I_{AR}	12	A
Repetitive avalanche energy (Note 2a) (Note 4)		E_{AR}	0.18	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	-55 to 150	°C

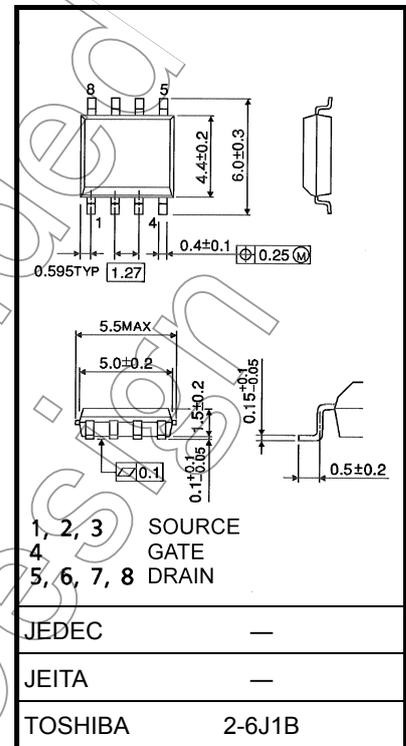
Note: For Notes 1 to 4, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

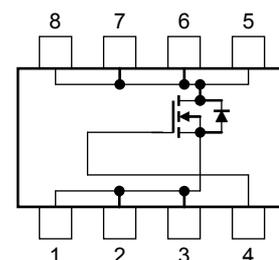
This transistor is an electrostatic-sensitive device. Handle with care.

Unit: mm



Weight: 0.085 g (typ.)

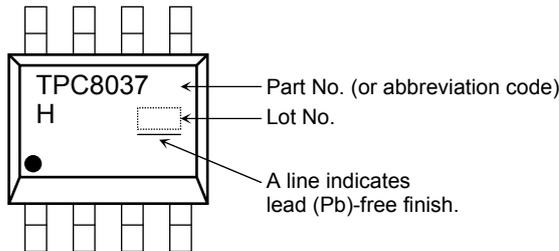
Circuit Configuration



Thermal Characteristics

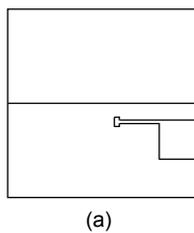
Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	$R_{th(ch-a)}$	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	$R_{th(ch-a)}$	125	°C/W

Marking (Note 5)

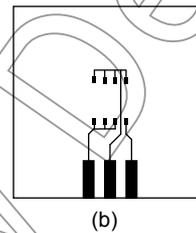


Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: (a) Device mounted on a glass-epoxy board (a) (b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)



FR-4
25.4 × 25.4 × 0.8
(Unit: mm)

Note 3: $V_{DD} = 24\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 500\ \mu\text{H}$, $R_G = 25\ \Omega$, $I_{AR} = 12\ \text{A}$

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: • on lower left of the marking indicates Pin 1.

* Weekly code: (Three digits)

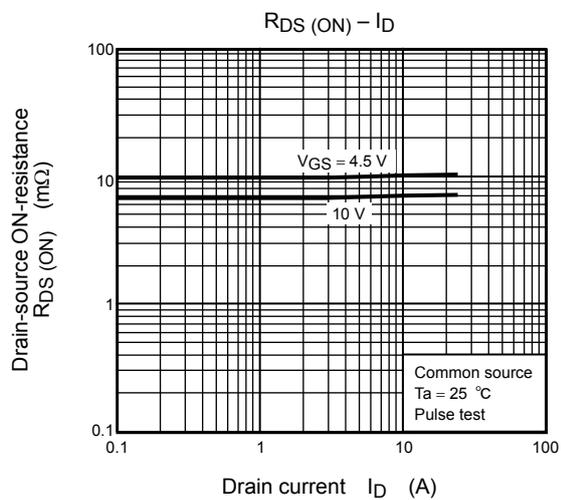
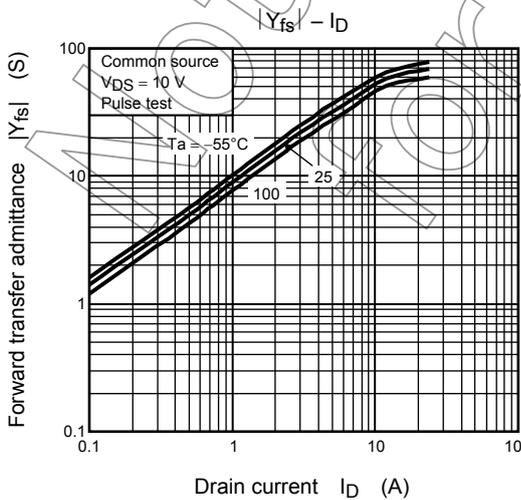
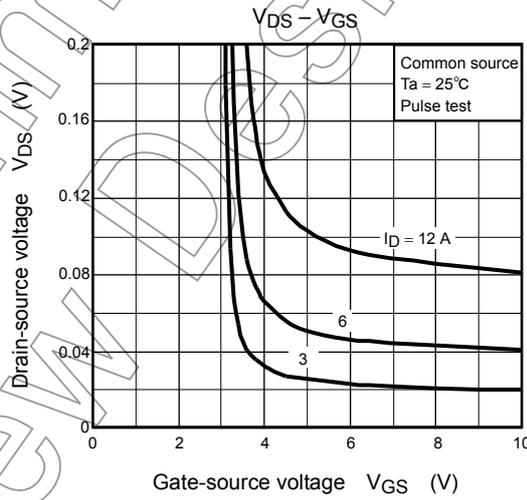
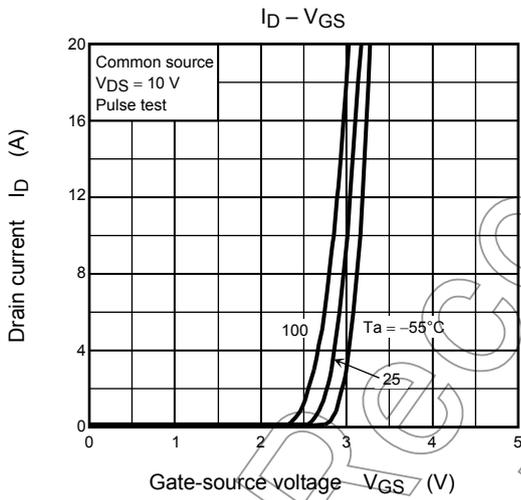
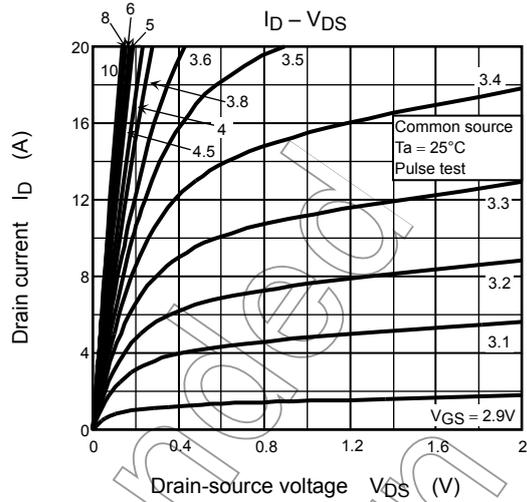
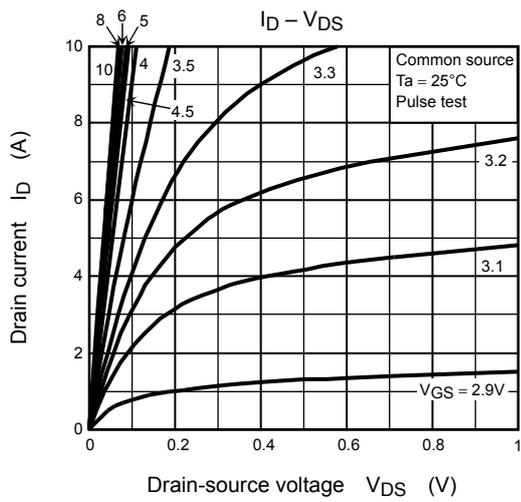


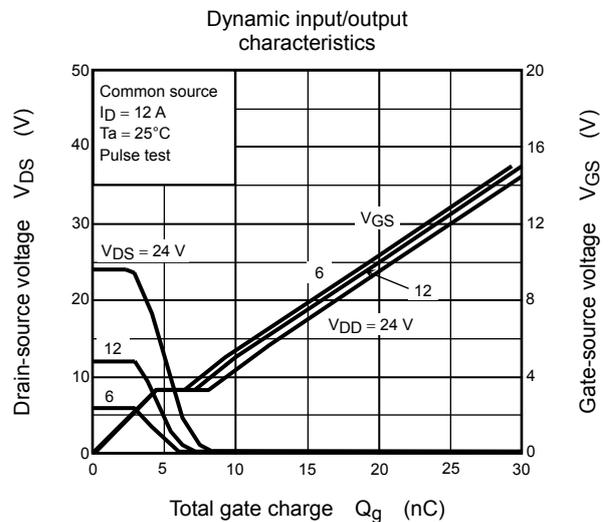
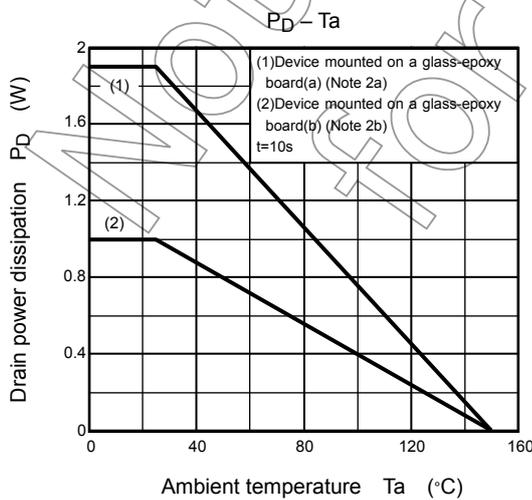
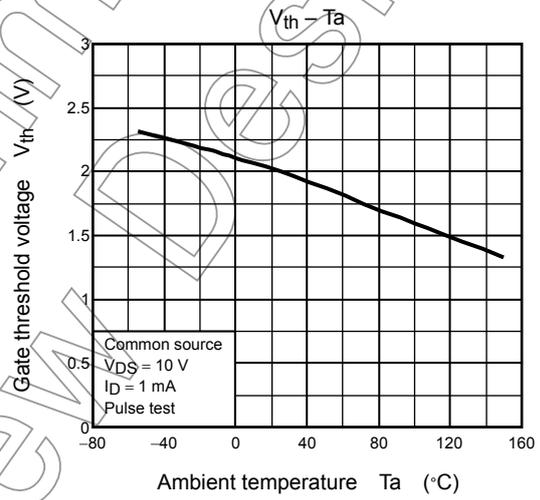
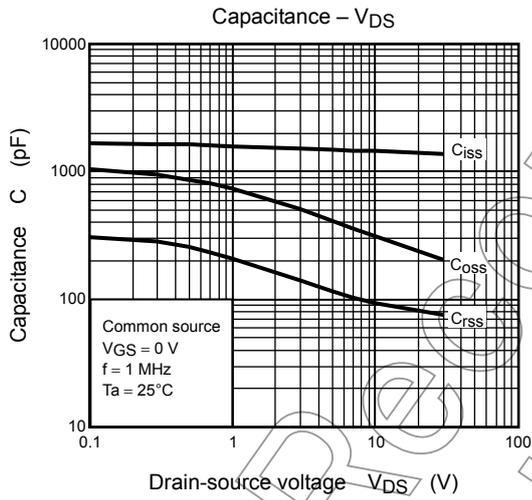
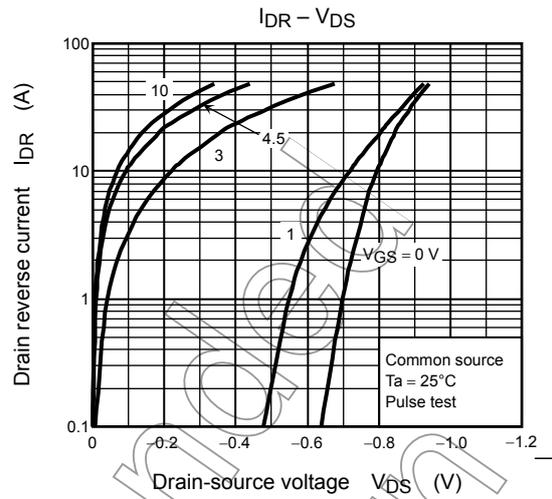
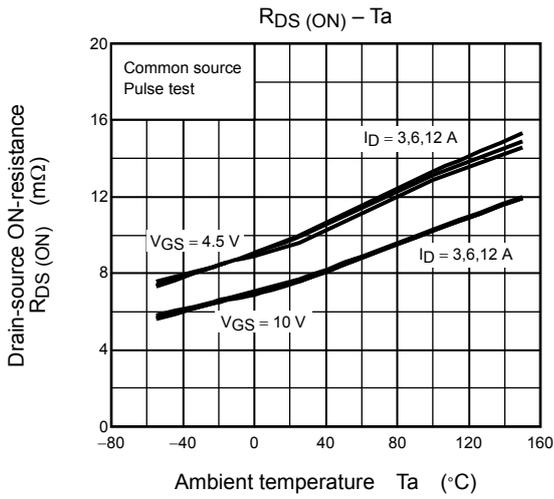
Electrical Characteristics (Ta = 25°C)

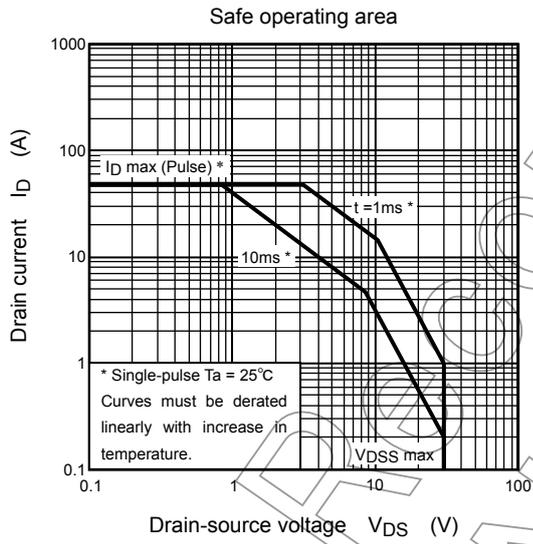
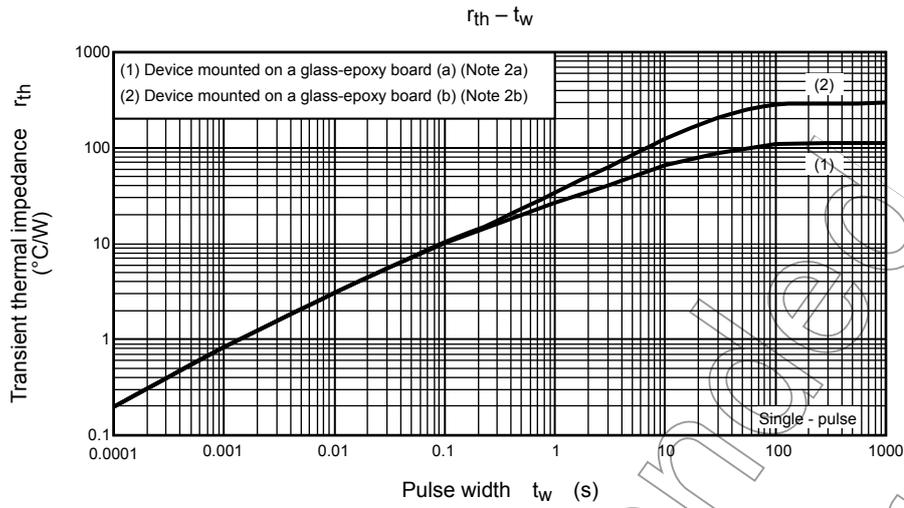
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 100	nA
Drain cutoff current		I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
		$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	15	—	—	
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.5	—	2.5	V
Drain-source ON-resistance		$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}$	—	9.9	13.9	m Ω
			$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	—	7.6	11.4	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 6\text{ A}$	18	36	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1433	2150	pF
Reverse transfer capacitance		C_{rss}		—	83	125	
Output capacitance		C_{oss}		—	303	—	
Gate resistance		R_g	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 5\text{ MHz}$	—	1.0	1.5	Ω
Switching time	Rise time	t_r		—	3	—	ns
	Turn-on time	t_{on}		—	10	—	
	Fall time	t_f		—	3.9	—	
	Turn-off time	t_{off}		Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$	—	23	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	—	21	—	nC
			$V_{DD} \approx 24\text{ V}, V_{GS} = 5\text{ V}, I_D = 12\text{ A}$	—	11	—	
Gate-source charge 1		Q_{gs1}	$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 12\text{ A}$	—	4.4	—	
Gate-drain ("Miller") charge		Q_{gd}		—	3.7	—	
Gate switch charge		Q_{sw}		—	5.0	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	48	A
Forward voltage (diode)		V_{DSF}	$I_{DR} = 12\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V







RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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