TH7111
868/915MHz FSK/FM/ASK Receiver

Features

- Double superhet architecture for high degree of image rejection
- FSK for digital data and FM reception for analog signal transmission
- FM/FSK demodulation either with phase-coincidence or PLL demodulator
- Low current consumption in active mode and very low standby current
- Switchable LNA gain for improved dynamic range
- AFC feature allows wide carrier frequency acceptance range
- RSSI allows signal strength indication and ASK detection
- Surface mount package LQFP44

Ordering Information

Part No.	Temperature Range	Package
TH7111	-40 °C to 85 °C	LQFP44

Application Examples

- General digital and analog 868 MHz or 915 MHz ISM band usage
- Low-power telemetry
- Alarm and security systems
- Keyless car and central locking
- Pagers

Technical Data Overview

- Input frequency range: 800 MHz to 930 MHz
- Power supply range: 2.5 V to 5.5 V for double conversion and 3.3 V to 5.5 V for single conversion
- Temperature range: -40 °C to +85 °C
- Operating current: 7.5 mA at low gain and 9.2 mA at high gain mode
- Standby current: < 100 nA
- Sensitivity: -109 dBm [1)] with 40 kHz second IF filter BW (incl. SAW front-end filter loss)
- Sensitivity: -102 dBm [2)] with 150 kHz second IF filter BW (incl. SAW front-end filter loss)
- Range of first IF: 10 MHz to 80 MHz
- Range of second IF: 455 kHz to 21.4 MHz
- Maximum input level: –10 dBm at ASK and 0 dBm at FSK
- Image rejection: > 65 dB (e.g. with SAW front-end filter and at 10.7 MHz 2nd IF)
- Spurious emission: < -70 dBm
- Input frequency acceptance: ±50 kHz (with AFC option)
- RSSI range: 70 dB
- Frequency deviation range: ±5 kHz to ±120 kHz
- Maximum data rate: 80 kbit/s NRZ
- Maximum analog modulation frequency: 15 kHz

[1)] at ± 8 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation
[2)] at ± 50 kHz FSK deviation, BER = $3 \cdot 10^{-3}$ and phase-coincidence demodulation

General Description

The TH7111 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback dividers DIV_16 and DIV_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
- second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
- IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
- Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering, ASK detection and automatic-frequency control (AFC)
- Bias circuitry for bandgap biasing and circuit shutdown

With the TH7111 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with varactor to create an AFC circuit). In PLL demodulator configuration, the multiplier MIX3 forms a phase comparator. In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier. The second VCO (VCO2) can be used either as the VCO of a PLL demodulator or as the LO2 source of a second external PLL in a multi-channel system. The following table briefly summarizes the various configurations.

	Single-conversion configuration	Double-conversion configuration
FM/FSK	narrow-band RX with ceramic demodulation tank	narrow-band RX with ceramic demodulation tank
FM/FSK	wide-band RX with LC demod. tank and AFC	wide-band RX with LC demod. tank and AFC
FM/FSK	extended sensitivity RX with PLL demodulator	extended sensitivity RX with PLL demodulator
FM/FSK		multi-channel RX with ceramic demodulation tank and external channel synthesizer
ASK	RX with RSSI-based demodulation	RX with RSSI-based demodulation
ASK		RX with RSSI-based demodulation and external channel synthesizer

The preferred superheterodyne configuration is **double conversion** where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a **high degree of image rejection**, achieved in conjunction with an RF front-end filter. Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding a LC filter at the LNA output.

It is also possible to use the TH7111 in **single-conversion** configuration. This can be achieved by switching the LO2 input of MIX2 from the on-chip PLL synthesizer to the pin IN_MIX2 by means of an internal switch (done via pin SW_MIX2). Now MIX2 operates as an amplifier for the IF1 signal if an external pull-down resistor at pin IN_MIX2 is added.

The same setting of MIX2 can be used for **multi-channel applications**. In this situation IN_MIX2 must be driven by an external LO2 signal. This signal can be generated by the VCO2, which is mainly a bipolar transistor that can be configured as a varactor-tuned VCO. Furthermore, a second external PLL for channel selection via LO2 tuning is required. This may be arranged by using a PLL synthesizer chip that can be controlled through a 3-wire bus serial interface. The reference signal for the external PLL synthesizer can be directly taken from the crystal-based reference oscillator RO.

Block Diagram

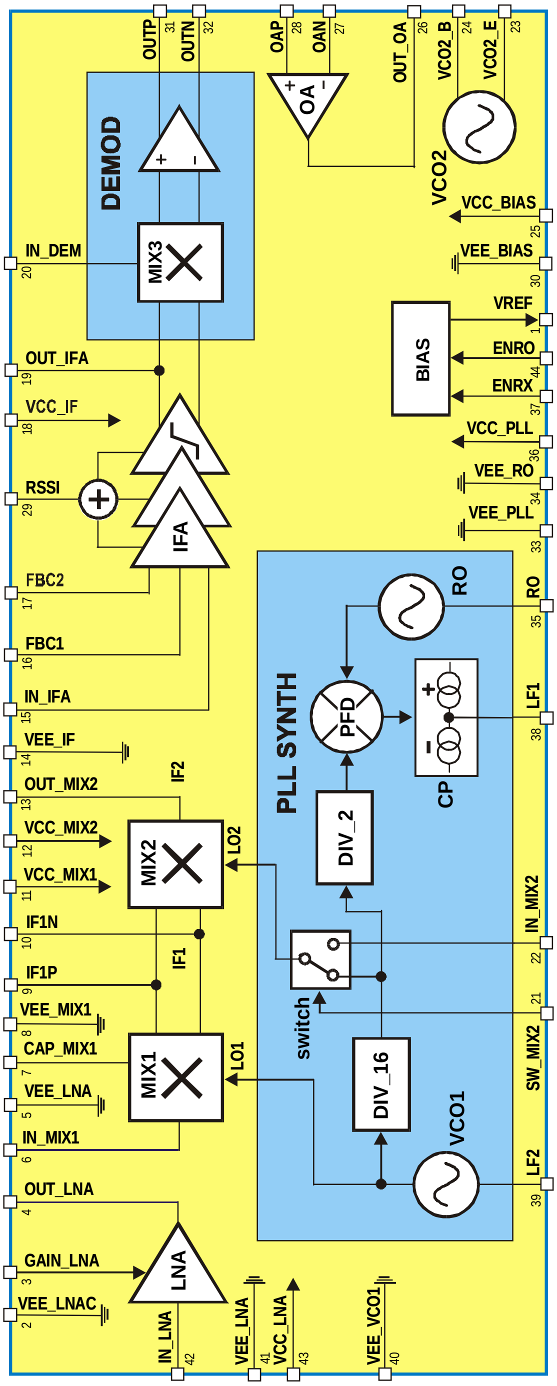


Fig. 1: TH7111 block diagram

Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO1 signal (which is now the one and only LO signal in the receiver).

The receiver's double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH7111 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of N1 = 16 (DIV_16) and N2 = 2 (DIV_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (**low-low**), LO1 low-side and LO2 high-side (**low-high**), LO1 high-side and LO2 low-side (**high-low**) or LO1 and LO2 high-side (**high-high**). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

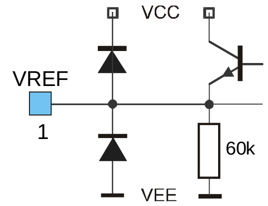
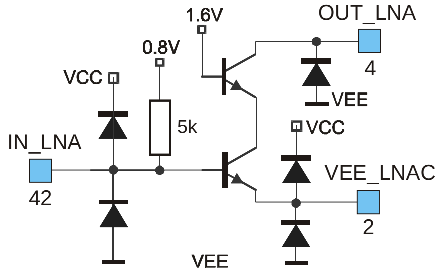
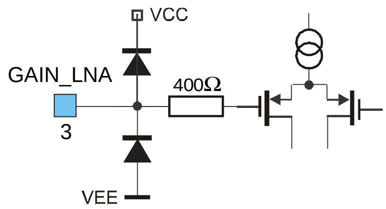
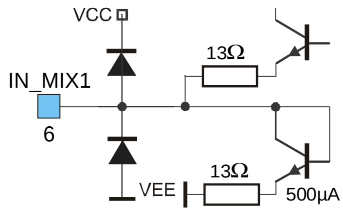
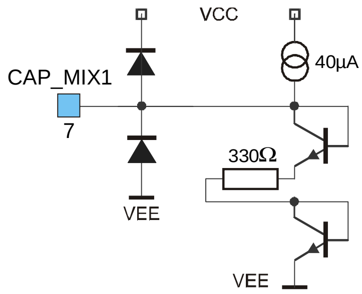
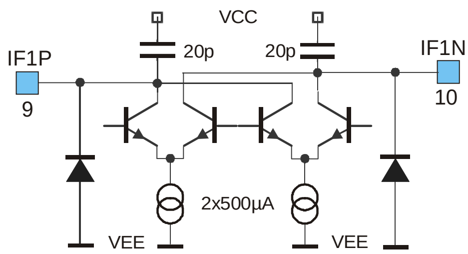
Injection type	high-high	low-low	high-low	low-high
REF	(RF – IF2)/30	(RF – IF2)/34	(RF + IF2)/30	(RF + IF2)/34
LO1	32•REF	32•REF	32•REF	32•REF
IF1	LO1 – RF	RF – LO1	LO1 – RF	RF – LO1
LO2	2•REF	2•REF	2•REF	2•REF
IF2	LO2 – IF1	IF1 – LO2	IF1 – LO2	LO2 – IF1

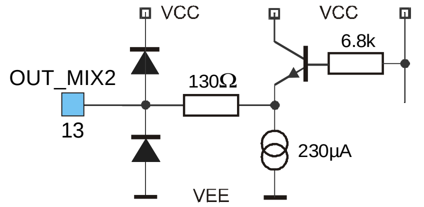
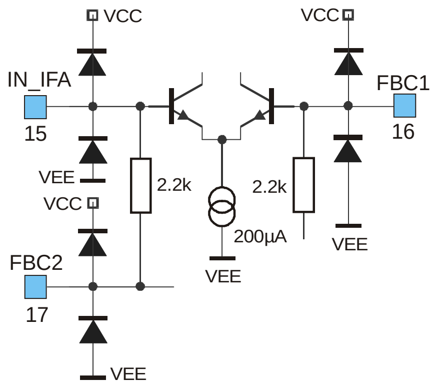
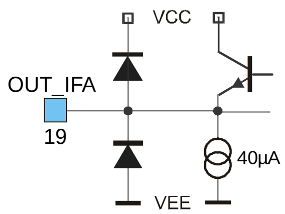
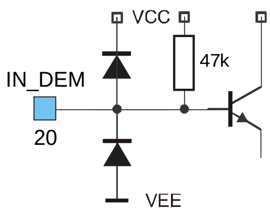
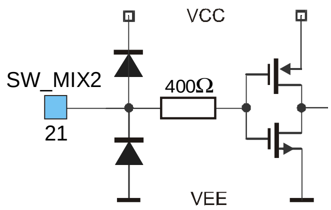
The following table depicts generated, desired, possible images and some undesired signals considering the examples of 868.3 MHz and 915 MHz RF reception at IF2 = 10.7 MHz.

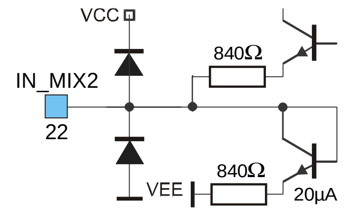
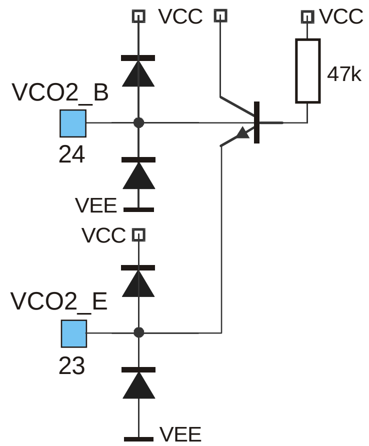
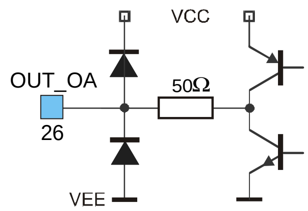
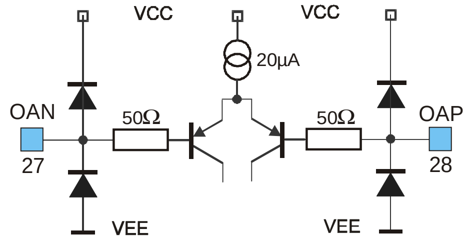
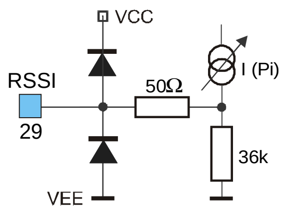
Signal type	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz
Injection type	high-high	**low-low**	high-low	low-high	high-high	**low-low**	high-low	low-high
REF / MHz	28.58667	**25.22353**	29.3	25.85294	30.14333	**26.59706**	30.85667	27.22647
LO1 / MHz	914.77333	**807.15294**	937.6	827.29412	964.58667	**851.10588**	987.41333	871.24706
IF1 / MHz	46.47333	**61.14706**	69.3	41.00588	49.58667	**63.89412**	72.41333	43.75294
LO2 / MHz	57.17333	**50.44706**	58.6	51.70588	60.28667	**53.19412**	61.71333	54.45294
RF image/MHz	961.24667	**746.00588**	1006.9	786.28824	1014.17	**787.21176**	1059.83	827.49412
IF1 image/MHz	67.87333	**39.74706**	47.9	62.40588	70.98667	**42.49412**	51.01333	65.15294

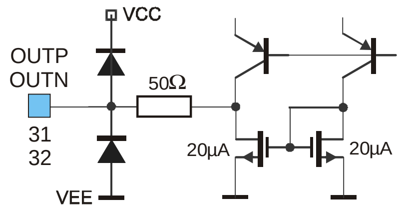
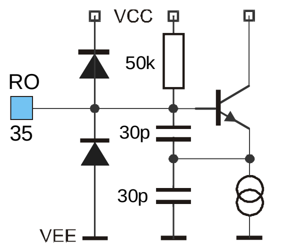
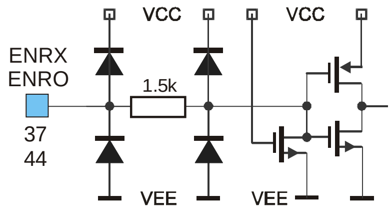
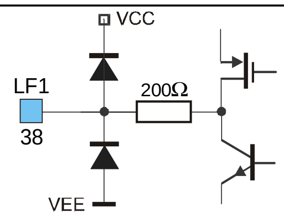
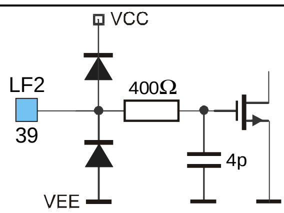
The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 800 MHz to 915 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 868.3 MHz and 915 MHz, respectively.

Pin Definition and Description

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O Type</th><th>Functional Schematic</th><th>Description</th></tr>
<tr><td>1</td><td>VREF</td><td>analog output</td><td>
</td><td>reference voltage output, approx. 1.23V</td></tr>
<tr><td>4</td><td>OUT_LNA</td><td>analog output</td><td rowspan="3">
</td><td>LNA open-collector output, to be connected to external LC tank that resonates at RF</td></tr>
<tr><td>42</td><td>IN_LNA</td><td>analog input</td><td>LNA input, approx. 26Ω single-ended</td></tr>
<tr><td>2</td><td>VEE_LNAC</td><td>ground</td><td>ground of LNA core (cascode)</td></tr>
<tr><td>3</td><td>GAIN_LNA</td><td>analog input</td><td>
</td><td>LNA gain control (CMOS input with hysteresis)</td></tr>
<tr><td>5</td><td>VEE_LNA</td><td>ground</td><td></td><td>LNA biasing ground</td></tr>
<tr><td>6</td><td>IN_MIX1</td><td>analog input</td><td>
</td><td>MIX1 input, approx. 33Ω single-ended</td></tr>
<tr><td>7</td><td>CAP_MIX1</td><td>analog I/O</td><td>
</td><td>connection for MIX1 blocking capacitor</td></tr>
<tr><td>8</td><td>VEE_MIX1</td><td>ground</td><td></td><td>MIX1 ground</td></tr>
<tr><td>9</td><td>IF1P</td><td>analog I/O</td><td rowspan="2">
</td><td>open-collector output, to be connected to external LC tank that resonates at first IF</td></tr>
<tr><td>10</td><td>IF1N</td><td>analog I/O</td><td>open-collector output, to be connected to external LC tank that resonates at first IF</td></tr>
</table>

Pin No.	Name	I/O Type	Functional Schematic	Description
11	VCC_MIX1	supply		MIX1 positive supply
12	VCC_MIX2	supply		MIX2 positive supply
13	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
14	VEE_IF	ground		ground of MIX2, IFA and DEMOD
15	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance
16	FBC1	analog I/O		to be connected to external IFA feedback capacitor
17	FBC2	analog I/O		to be connected to external IFA feedback capacitor
18	VCC_IF	supply		positive supply for IFA, DEMOD and VCO2
19	OUT_IFA	analog I/O		IFA output and MIX3 input (of DEMOD)
20	IN_DEM	analog input		DEMOD input, to MIX3 core
21	SW_MIX2	digital input		input selection for LO2 input port of MIX2

Pin No.	Name	I/O Type	Functional Schematic	Description
22	IN_MIX2	analog input		external LO2 input port of MIX2, approx. 1kΩ single-ended
24	VCO2_B	analog input		VCO2 input, base of a bipolar transistor
23	VCO2_E	analog output		VCO2 output, emitter of a bipolar transistor
25	VCC_BIAS	supply		positive supply of general bias system and OA
26	OUT_OA	analog output		OA output, 40uA current drive capability
27	OAN	analog input		negative OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN
28	OAP	analog input		positive OA input, input voltage limited to approx. 0.7 V_{pp} between pins OAP and OAN
29	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
30	VEE_BIAS	ground		ground for general bias system and OA

Pin No.	Name	I/O Type	Functional Schematic	Description
31	OUTP	analog output		FSK/FM positive output, output impedance of 100kΩ to 300kΩ
32	OUTN	analog output		FSK/FM negative output, output impedance of 100kΩ to 300kΩ
33	VEE_PLL	ground		ground of dividers and PFD
34	VEE_RO	ground		RO ground
35	RO	analog input		RO input, Colpitts type oscillator with internal feed-back capacitors
36	VCC_PLL	supply		positive supply of RO, DIV, PFD and charge pump
37	ENRX	digital input		mode control input (CMOS input)
44	ENRO	digital input		mode control input (CMOS input)
38	LF1	analog output		charge pump output
39	LF2	analog input		VCO1 control input
40	VEE_VCO1	ground		ground of VCO1 and charge pump
41	VEE_LNA	ground		ground of LNA biasing
43	VCC_LNA	supply		positive supply of LNA biasing

Technical Data

Mode Configurations

ENRX	ENRO	Mode	Description
0	0	SBY	standby mode
0	1	RO only	only reference oscillator active
1	0	ON	entire chip active
1	1	ON	entire chip active

Note: ENRX and ENRO are pulled down internally

Second Mixer Input

IN_MIX2V	SW_MIX2	Mode
External LO2	0	double conversion with external LO2
Ext. pull-down res. (15 kΩ)	0	single conversion
N/C	1	double conversion with internal LO2

LNA Gain Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain by voltage at GAIN_LNA
> 1.4 V	LOW GAIN	LNA set to low gain by voltage at GAIN_LNA

Note: hysteresis between gain modes to ensure stability

Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{cc}		0	7.0	V
Input voltage	V_{IN}		- 0.3	V_{CC}+0.3	V
Input RF level	P_{imax}	no damage		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Electrostatic discharge	ESD	human body model, MIL STD 833D method 3015.7, all pins except OUT_IFA pin OUT_IFA	 -500 -500	 +500 +250	 V V

Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage for double conv.	$V_{cc,\,DC}$		2.5	5.5	V
Supply voltage for single conv.	$V_{cc,\,SC}$		3.3	5.5	V
Operating temperature	T_a		-40	+85	ºC
Input frequency	f_i		800	930	MHz
Frequency deviation	Δf	at FM or FSK	±5	±120	kHz
FSK data rate	R_{FSK}	NRZ		40	kbit/s
FM bandwidth	f_m			15	kHz
ASK data rate	R_{ASK}	NRZ		80	kbit/s

DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at $T_a = 23$ °C and $V_{cc} = 3$ V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{SBY}	ENRX=0			100	nA
Total supply current at low gain	$I_{cc,\ low}$	ENRX=1, LNA at LOW GAIN	6.0	7.5	9.0	mA
Total supply current at high gain	$I_{cc,\ high}$	ENRX=1, LNA at HIGH GAIN	7.5	9.2	11.0	mA
Opamp input offset voltage	V_{offs}		-20		20	mV
Opamp input offset current	I_{offs}	$I_{OAP} - I_{OAN}$	-50		50	nA
Opamp input bias current	I_{bias}	$0.5 * (I_{OAP} + I_{OAN})$	-100		100	nA
RSSI voltage at low input level	$V_{RSSI,\ low}$	P_i = -65 dBm, LNA at LOW GAIN	0.5	1.0	1.5	V
RSSI voltage at high input level	$V_{RSSI,\ high}$	P_i = -35 dBm, LNA at LOW GAIN	1.25	1.9	2.45	V

AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
all parameters based on test circuits for FSK (Fig. 2), FM (Fig. 4) and ASK (Fig. 5), respectively;
typical values at $T_a = 23$ °C and $V_{cc} = 3$ V, RF at 868.3MHz, second IF at 10.7 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Start-up time – fast mode FSK/FM	T_{fast}	ENRX from 0 to 1, ENRO = 1, valid data at output			0.4	ms
Start-up time – slow mode FSK/FM	T_{slow}	ENRX from 0 to 1, ENRO = 0, valid data at output			0.9	ms
Start-up time – ASK	T_{ASK}	depends on ASK detector time constant and start-up mode, valid data at output			R3•C13 + T_{fast} (or T_{slow})	ms
Input sensitivity – FSK (narrow band)	$P_{min,\ n}$	B_{IF2} = 40kHz $\Delta f = \pm 15$kHz (FSK/FM) BER $\leq 3 \cdot 10^{-3}$		-109		dBm
Input sensitivity – FSK (wide band)	$P_{min,\ w}$	B_{IF2} = 150kHz $\Delta f = \pm 50$kHz (FSK/FM) BER $\leq 3 \cdot 10^{-3}$		-102		dBm
Input sensitivity – ASK (narrow band)	$P_{minA,\ n}$	B_{IF2} = 40kHz BER $\leq 3 \cdot 10^{-3}$		-108		dBm
Input sensitivity – ASK (wide band)	$P_{minA,\ w}$	B_{IF2} = 150kHz BER $\leq 3 \cdot 10^{-3}$		-104		dBm
Maximum input signal – FSK/FM	$P_{max,\ FM}$	BER $\leq 3 \cdot 10^{-3}$ LNA at LOW GAIN		0		dBm
Maximum input signal – ASK	$P_{max,\ ASK}$	BER $\leq 3 \cdot 10^{-3}$ LNA at LOW GAIN		-10		dBm
Spurious emission	P_{spur}				-70	dBm
Image rejection	ΔP_{imag}			65		dB
Blocking immunity	ΔP_{block}	$\Delta f_{block} > \pm 2$MHz, note 1		57		dB
VCO gain	K_{VCO}			250		MHz/V
Charge pump current	I_{CP}			60		µA

Notes: 1. desired signal with FSK/FM or ASK modulation, CW blocking signal

Test Circuits

FSK Reception

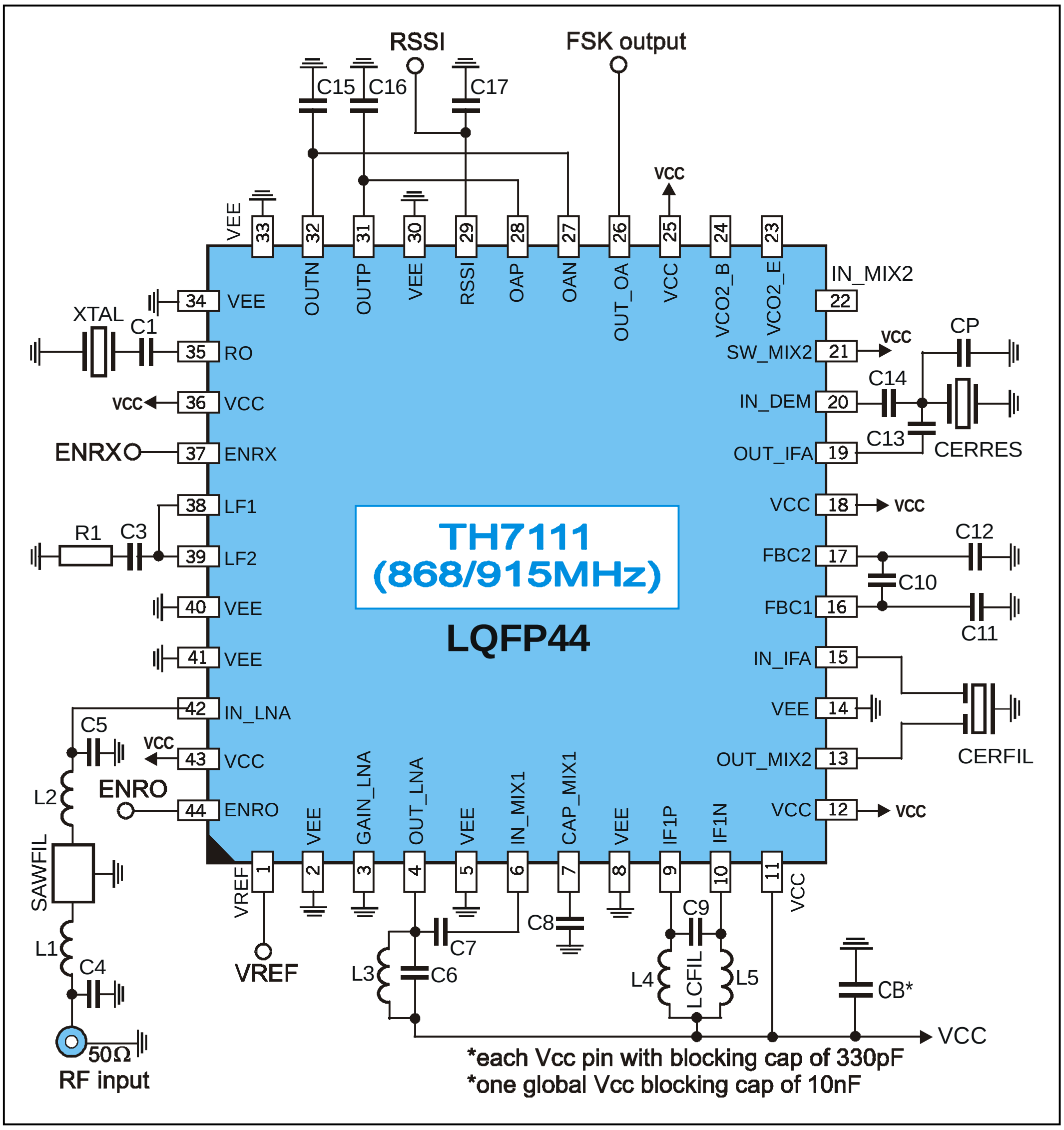


Fig. 2: Test circuit for FSK reception

FSK test circuit component list to Fig. 2

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0603	22 pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C14	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 – 12 pF	±5%	CERRES parallel capacitor
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C17	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
L4	0805	100 nH	±5%	IF1 tank inductor
L5	0805	100 nH	±5%	IF1 tank inductor
XTAL	HC49-SMD	**25.22353 MHz @ RF = 868.3 MHz**	±25ppm calibra-tion ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0, max}$ = 7 pF, $R_{m, max}$ = 50 Ω
SAWFIL	QCC8C	**B3570 @ RF = 868.3 MHz**	B_{3dB} = 1.7 MHz	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

FSK Circuit with AFC and Ceramic Resonator Tolerance Compensation

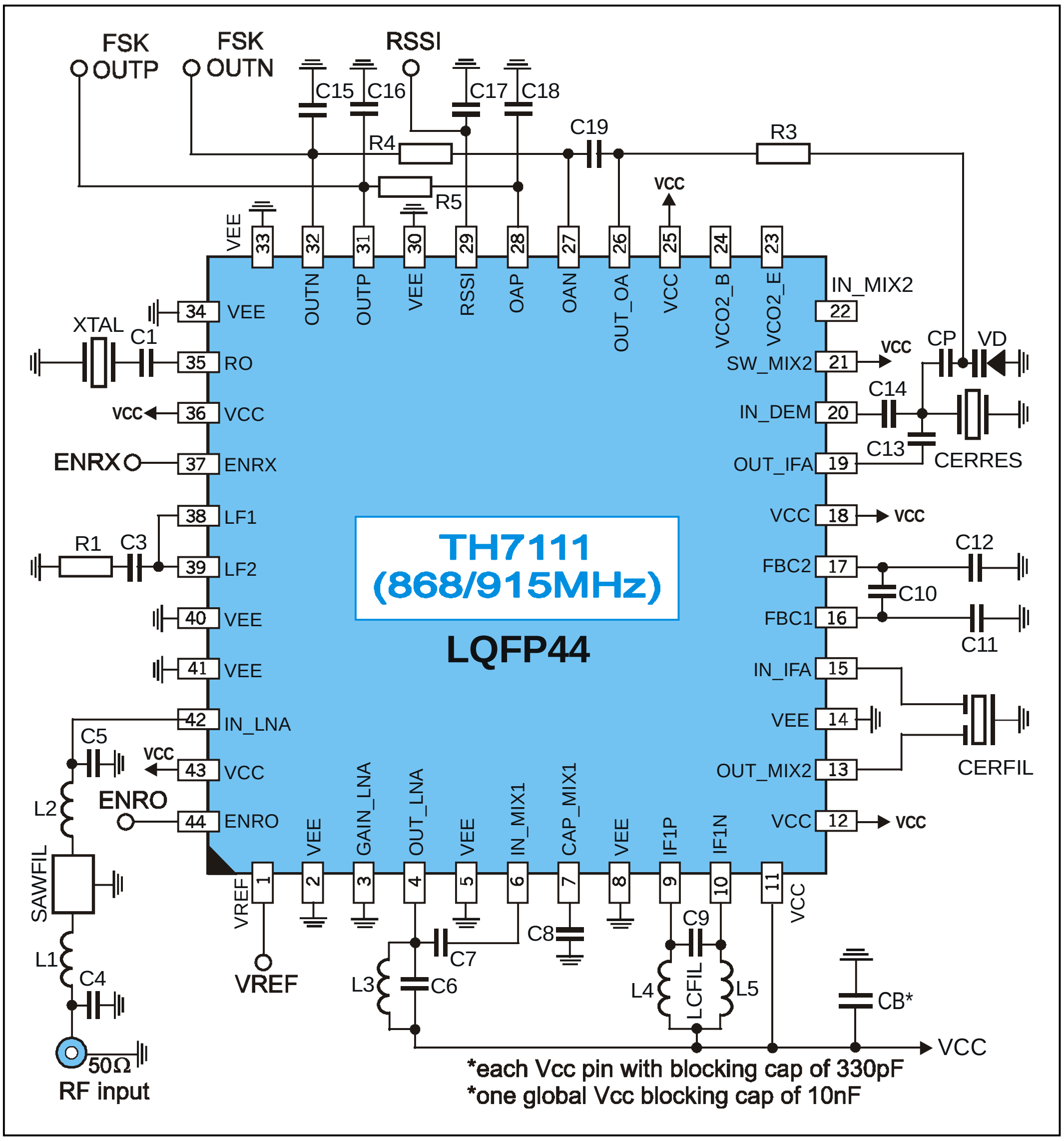


Fig. 3: Test circuit for FSK with AFC and resonator compensation

Circuit Feature

- ❑ Improves input frequency acceptance range up to RF_{nom} ±50 kHz
- ❑ Eliminates calibration tolerances of ceramic resonator
- ❑ Eliminates temperature tolerances of ceramic resonator
- ❑ Non-inverted and inverted CMOS-compatible outputs

FSK test circuit with AFC component list to Fig. 3

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0603	22 pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	1.5 pF	±5%	DEMOD phase-shift capacitor
C14	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	27 pF	±5%	ceramic resonator loading capacitor
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C17	0603	330 pF	±10%	RSSI output low-pass capacitor
C18		33 nF	±10%	integrator capacitor, fixed
C19	0805	33 nF	±10%	integrator capacitor, @ 0.5 to 2 kbit/s NRZ
		10 nF		integrator capacitor, @ 2 to 20 kbit/s NRZ
		1 nF		integrator capacitor, @ 20 to 40 kbit/s NRZ
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0805	100 kΩ	±10%	varactor diode biasing resistor
R4	0805	680 kΩ	±10%	integrator resistor
R5	0805	680 kΩ	±10%	integrator resistor
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
L4	0805	100 nH	±5%	IF1 tank inductor
L5	0805	100 nH	±5%	IF1 tank inductor
VD	SOD-323	BB535		varactor diode from Infineon
XTAL	HC49-SMD	**25.22353 MHz** @ **RF = 868.3 MHz**	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\,max}$ = 7 pF, $R_{m,\,max}$ = 50 Ω
SAWFIL	QCC8C	**B3570** @ **RF = 868.3 MHz**	B_{3dB} = 1.7 MHz	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

FM Reception

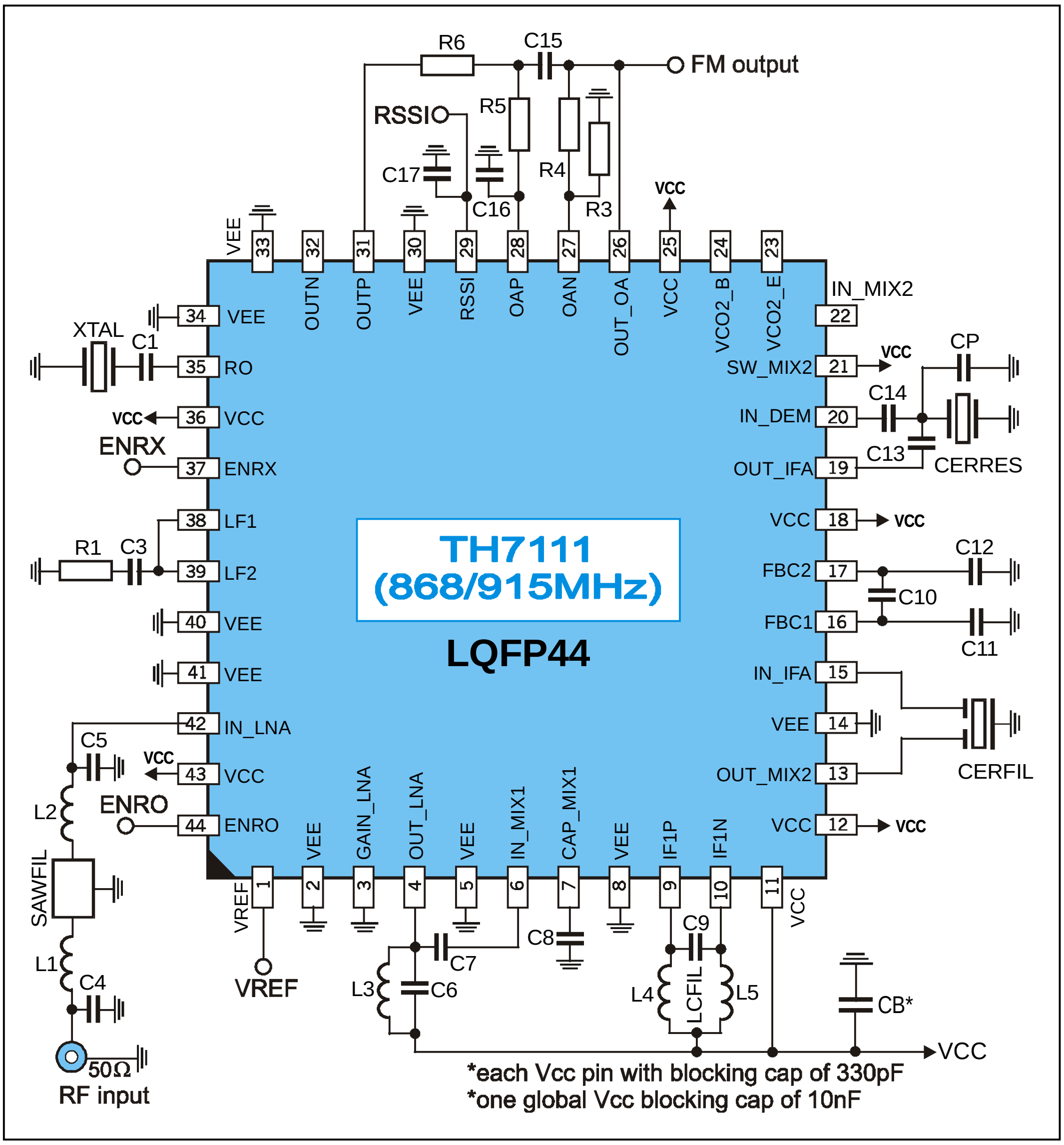


Fig. 4: Test circuit for FM reception

FM test circuit component list to Fig. 4

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0603	22 pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0603	1.5pF	±5%	DEMOD phase-shift capacitor
C14	0603	680 pF	±10%	DEMOD coupling capacitor
CP	0805	10 –12 pF	±5%	CERRES parallel capacitor
C15	0805	100 pF	±5%	sallen-key low-pass filter capacitor, to set cut-off fre- quency
C16	0805	100 pF	±5%	sallen-key low-pass filter capacitor, to set cut-off fre- quency
C17	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0805	12 kΩ	±5%	sallen-key filter resistor, to set desired filter characteristic
R4	0805	6.8 kΩ	±5%	sallen-key filter resistor, to set desired filter characteristic
R5	0805	33 kΩ	±5%	sallen-key filter resistor, to set cut-off frequency
R6	0805	33 kΩ	±5%	sallen-key filter resistor, to set cut-off frequency
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductor
L5	0603	100 nH	±5%	IF1 tank inductor
XTAL	HC49- SMD	**25.22353 MHz** **@ RF = 868.3 MHz**	±25ppm calibra- tion ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 50 Ω
SAWFIL	QCC8C	**B3570** **@ RF = 868.3 MHz**	B_{3dB} = 1.7 MHz	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

ASK Reception

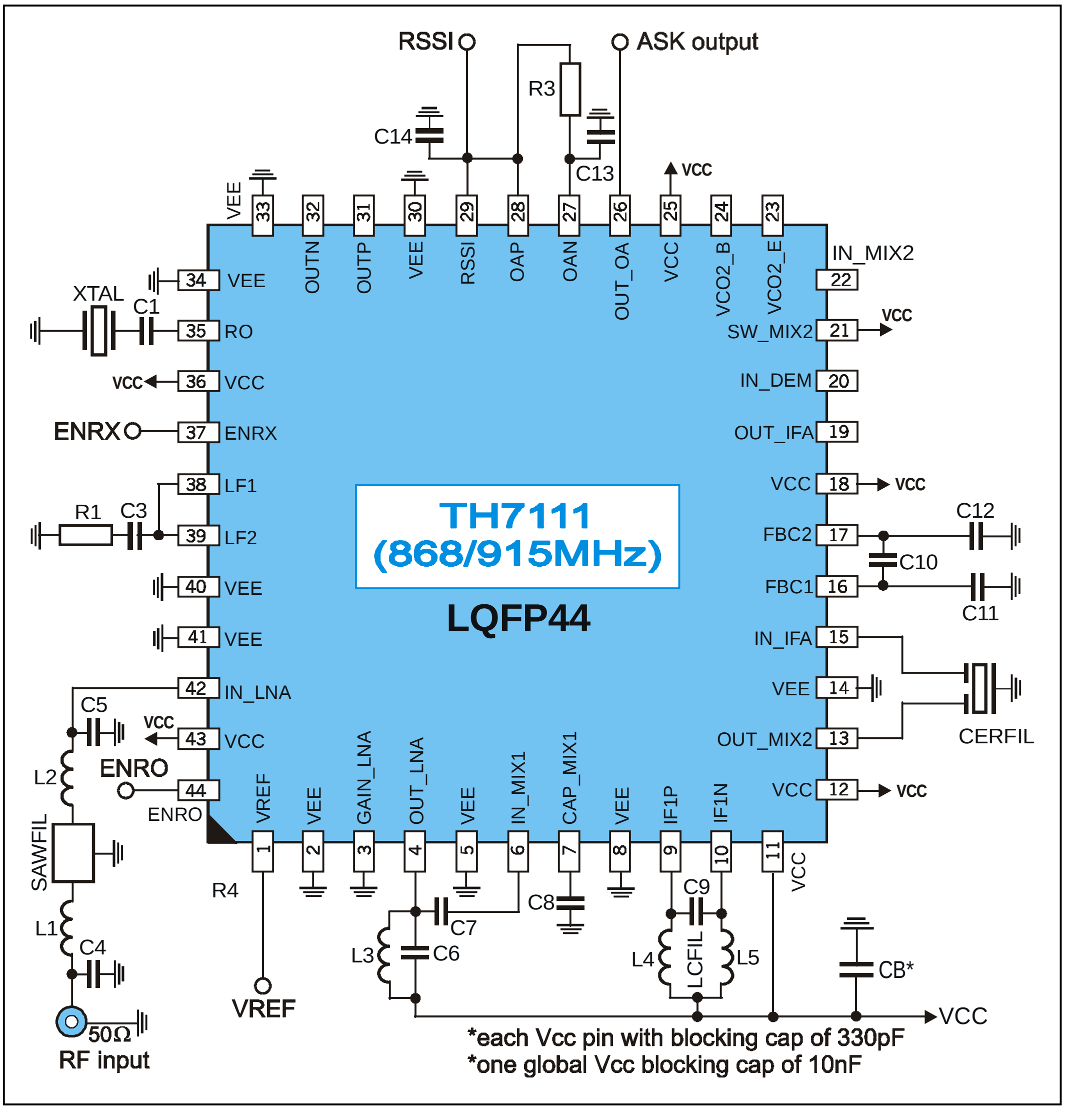


Fig. 5: Test circuit for ASK reception

ASK test circuit component list to Fig. 5

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match to SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match to SAW filter output
C6	0603	NIP	±5%	LNA output tank capacitor
C7	0603	1.2 pF	±5%	MIX1 input matching capacitor
C8	0603	330 pF	±10%	MIX1 blocking capacitor
C9	0805	22 pF	±5%	IF1 tank capacitor
C10	0805	33 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1 nF	±10%	IFA feedback capacitor
C13	0805	1 nF to 10 nF	±10%	ASK data slicer capacitor, depending on data rate
C14	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R3	0603	100 kΩ	±5%	ASK data slicer resistor, depending on data rate
L1	0603	12 nH	±5%	inductor to match SAW filter
L2	0603	12 nH	±5%	inductor to match SAW filter
L3	0603	6.8 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductor
L5	0603	100 nH	±5%	IF1 tank inductor
XTAL	HC49-SMD	**25.22353 MHz** @ **RF = 868.3 MHz**	±25ppm calibra-tion ±30ppm temp.	fundamental-mode crystal, C_{load} = 10 pF to 15pF, $C_{0,\ max}$ = 7 pF, $R_{m,\ max}$ = 50 Ω
SAWFIL	QCC8C	**B3570** @ **RF = 868.3 MHz**	B_{3dB} = 1.7 MHz	low-loss SAW filter from EPCOS
CERFIL	leaded type	SFE10.7MFP @ B_{IF2} = 40 kHz	TBD	ceramic filter from Murata
	SMD type	SFECV10.7MJS-A @ B_{IF2} = 150 kHz	±40 kHz	

NIP – not in place, may be used optionally

Package Dimensions

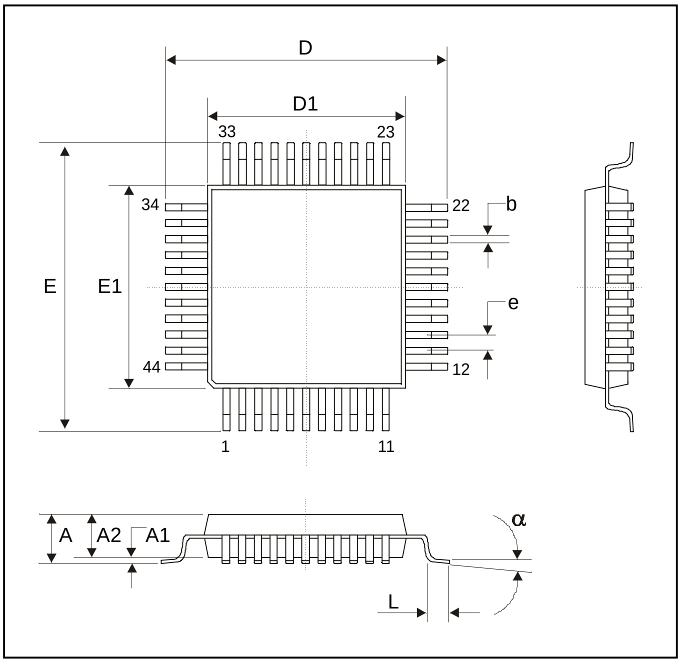


Fig. 6: LQFP44 (Low Quad Flat Package)

All Dimension in mm, coplanaríty < 0.1mm									
	E1, D1	**A**	**A1**	**A2**	**e**	**b**	**L**	**E, D**	**α**
min			0.05	1.35		0.30	0.45		0°
	10.00				0.8			12.00	
max		1.60	0.15	1.45		0.45	0.75		7°
All Dimension in inch, coplanaríty < 0.004”									
min			0.002	0.053		0.012	0.018		0°
	0.394				0.031			0.472	
max		0.630	0.006	0.057		0.018	0.030		7°

Your Notes

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