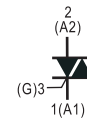
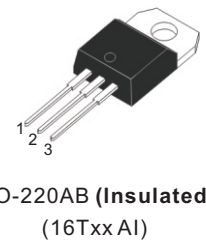
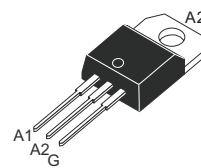
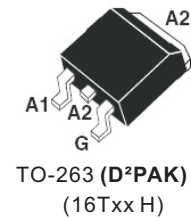


TRIACs, 16A Snubberless, Logic Level and Standard

Features

- Medium current Triac
- Low thermal resistance with clip bonding
- Low thermal resistance insulation ceramic for insulated 16T
- High commutation (4Q) or very high commutation (3Q) capability
- RoHS compliant, UL certified (File NO:E320098)
- Insulated tab (16TxxAI series, rated at 2500 VRMS)



Applications

- Snubberless versions (With Suffix W) especially recommended for use on inductive loads, because of their high commutation performances
- On/off or phase angle function in applications such as static relays, light dimmers and appliance motor speed controllers

Description

Available either in through-hole or surface-mount packages, the 16TxxA and 16TxxAI triacs series are suitable for general purpose mains power AC switching

SYMBOL	VALUE	UNIT
$I_{T(RMS)}$	16	A
V_{DRM}/V_{RRM}	to	V
$I_{GT(Q1)}$	5 to 50	mA

Device summary			
SYMBOL	PARAMETER	16TxxAI ⁽¹⁾	16TxxA
$I_{T(RMS)}$	On-state RMS current	16	16
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage	600/800/1000	600/800/1000
$I_{GT}(\text{Snubberless})$	Triggering gate current	35/50	35/50
$I_{GT}(\text{logic level})$	Triggering gate current	10	10
$I_{GT}(\text{standard})$	Triggering gate current	25/50	25/50

Note 1: Insulated

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current (full sine wave)	$I_{T(RMS)}$	TO-220/TO-263	$T_c = 110^\circ\text{C}$	16	A
		TO-220insulate	$T_c = 86^\circ\text{C}$		
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F = 50 Hz	t = 20 ms	160	A
		F = 60 Hz	t = 16.7 ms	168	
I ² t Value for fusing	I^2t	$t_p = 10$ ms		128	A ² s
Critical rate of rise of on-state current $I_G = 2xI_{GT}$, $t_r \leq 100$ ns	dI/dt	F = 100 Hz	$T_j = 125^\circ\text{C}$	50	A/ μ s
Peak gate current	I_{GM}	$T_p = 20$ μ s	$T_j = 125^\circ\text{C}$	4	A
Average gate power dissipation	$P_{G(AV)}$	$T_j = 125^\circ\text{C}$		1	W
Storage temperature range	T_{stg}			- 40 to + 150	°C
Operating junction temperature range	T_j			- 40 to + 125	

⊙ ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$ unless otherwise specified)

SNUBBERLESS and Logic level (3 quadrants)							
SYMBOL	TEST CONDITIONS	QUADRANT		16Txxxx			Unit
				SW	CW	BW	
$I_{GT}^{(1)}$	$V_D = 12$ V, $R_L = 33\Omega$	I - II - III	MAX.	10	35	50	mA
V_{GT}		I - II - III	MAX.	1.3			V
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3K\Omega$ $T_j = 125^\circ\text{C}$	I - II - III	MIN.	0.2			V
$I_H^{(2)}$	$I_T = 500$ mA		MAX.	15	40	55	mA
I_L	$I_G = 1.2 I_{GT}$	I - III	MAX.	25	50	70	mA
		II		30	60	80	
dV/dt ⁽²⁾	$V_D = 67\% V_{DRM}$, gate open, $T_j = 125^\circ\text{C}$		MIN.	40	500	1000	V/ μ s
(dI/dt) _c ⁽²⁾	(dV/dt) _c = 0.1 V/ μ s	$T_j = 125^\circ\text{C}$	MIN.	8.5	-	-	A/ms
	(dV/dt) _c = 10 V/ μ s	$T_j = 125^\circ\text{C}$		3	-	-	
	Without snubber	$T_j = 125^\circ\text{C}$		-	8.5	14	

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

⊙ ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

Standard (4 quadrants)						
SYMBOL	TEST CONDITIONS	QUADRANT	16Txxxx		UNIT	
			C	B		
I _{GT} ⁽¹⁾	V _D = 12 V, R _L = 33Ω	I - II - III	MAX.	25	50	mA
V _{GT}		IV		50	100	
V _{GD}	V _D = V _{DRM} , R _L = 3.3KΩ, T _j = 125°C	ALL		1.3		V
I _H ⁽²⁾	I _T = 500 mA	ALL	MAX.	25	50	mA
I _L	I _G = 1.2 I _{GT}	I - III - IV	MAX.	40	60	mA
dV/dt ⁽²⁾		II		80	120	
(dV/dt) _c ⁽²⁾	(dI/dt) _c = 7 A/ms, T _j = 125°C		MIN.	200	400	V/μs
			MIN.	5	10	V/μs

STATIC CHARACTERISTICS					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
V _{TM} ⁽²⁾	I _{TM} = 22.5 A, t _p = 380 μs	T _j = 25°C	MAX.	1.55	V
V _{I0} ⁽²⁾	Threshold voltage	T _j = 125°C	MAX.	0.85	V
R _d ⁽²⁾	Dynamic resistance	T _j = 125°C	MAX.	25	mΩ
I _{DRM} I _{RDM}	V _D = V _{DRM} V _R = V _{RDM}	T _j = 25°C	MAX.	5	μA
		T _j = 125°C		1	mA

Note 1: Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: For both polarities of A2 referenced to A1.

THERMAL RESISTANCE					
SYMBOL	TEST CONDITIONS			VALUE	UNIT
R _{th(j-c)}	Junction to case (AC)	TO-220AB, D ² PAK		1.2	°C/W
		TO-220AB Insulated		2.1	
R _{th(j-a)}	Junction to ambient	S ⁽¹⁾ = 1cm ²	D ² PAK	45	°C/W
			TO-220AB Insulated, TO-220AB		

Note 1: S=Copper surface under tab

PRODUCT SELECTOR						
PART NUMBER	VOLTAGE (xx)			SENSITIVITY	TYPE	PACKAGE
	600 V	800 V	1000 V			
16TxxA-B/16TxxAI-B	V	V	V	50 mA	Standard	TO-220AB
16TxxA-BW/16TxxAI-BW	V	V	V	50 mA	Snubberless	TO-220AB
16TxxA-C/16TxxAI-C	V	V	V	25 mA	Standard	TO-220AB
16TxxA-CW/16TxxAI-CW	V	V	V	35 mA	Snubberless	TO-220AB
16TxxA-SW/16TxxAI-SW	V	V	V	10 mA	Logic level	TO-220AB
16TxxH-SW	V	V	V	10 mA	Logic level	D ² PAK
16TxxH-CW	V	V	V	35 mA	Snubberless	D ² PAK

ORDERING INFORMATION					
ORDERING TYPE	MARKING	PACKAGE	WEIGHT	BASE Q'TY	DELIVERY MODE
16TxxA-yy	16TxxA-yy	TO-220AB	2.0g	50	Tube
16TxxAI-yy	16TxxAI-yy	TO-220AB (insulated)	2.3g	50	Tube
16TxxH-yy	16TxxH-yy	TO-236(D ² PAK)	2.0g	50	Tube

Note: xx = voltage, yy = sensitivity

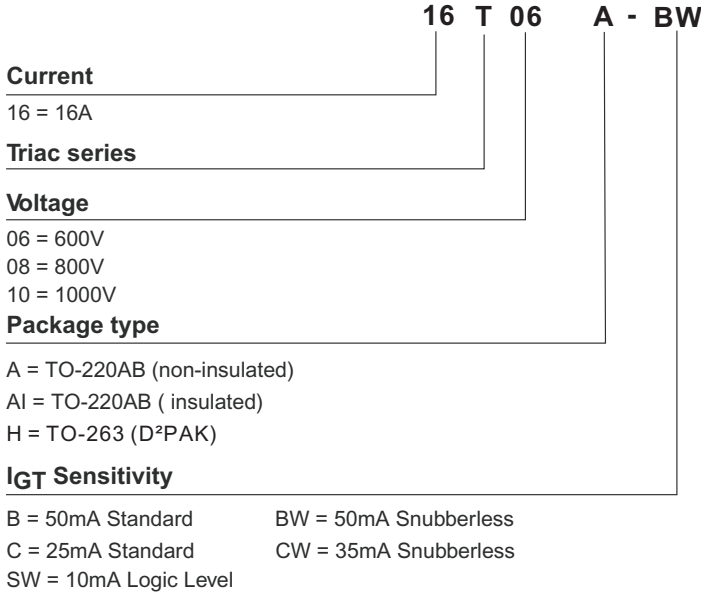
ORDERING INFORMATION SCHEME	
<p>16 T 06 A - BW</p> <p>Current 16 = 16A</p> <p>Triac series</p> <p>Voltage 06 = 600V 08 = 800V 10 = 1000V</p> <p>Package type A = TO-220AB (non-insulated) AI = TO-220AB (insulated) H = TO-263 (D²PAK)</p> <p>IGT Sensitivity B = 50mA Standard BW = 50mA Snubberless C = 25mA Standard CW = 35mA Snubberless SW = 10mA Logic Level</p>	

Fig.1 Maximum power dissipation versus on-state rms current (full cycle)

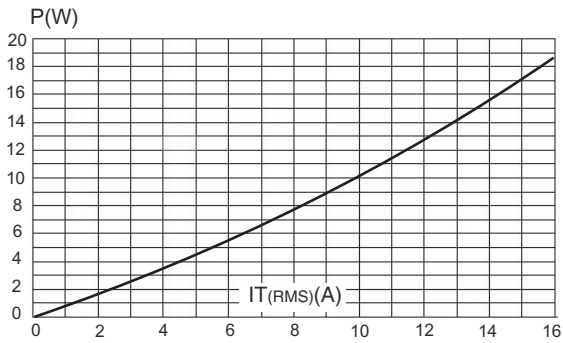


Fig.2 On-state rms current versus case temperature (full cycle)

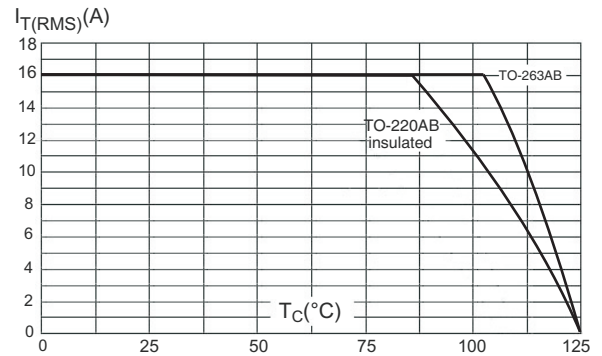


Fig.3 On-state current versus ambient temperature (full cycle)

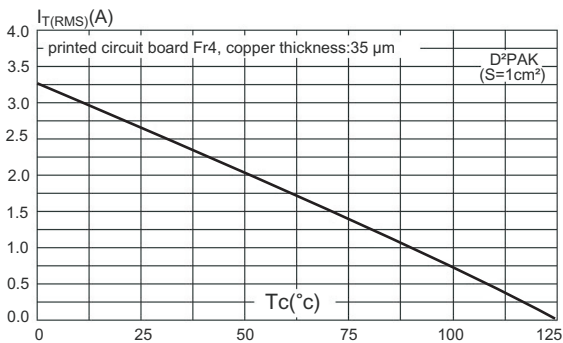


Fig.4 Relative variation of thermal impedance versus pulse duration

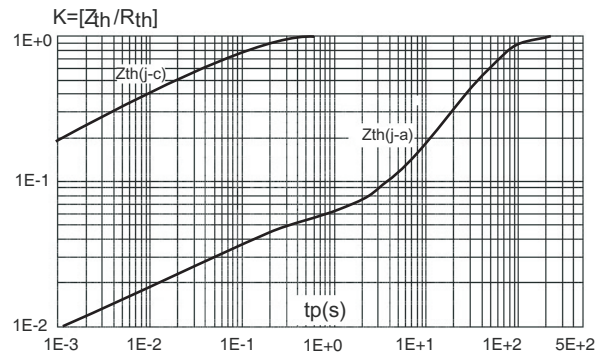


Fig.5 On-state characteristics (maximum values)

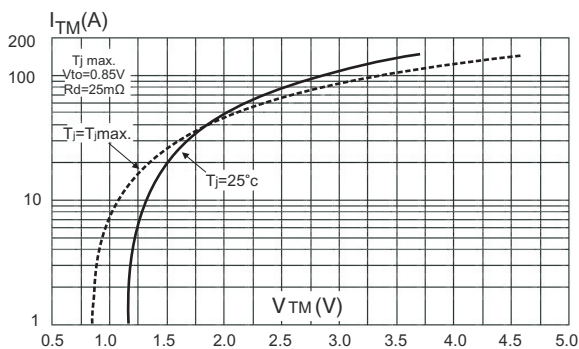


Fig.6 surge peak on-state current versus number of cycles

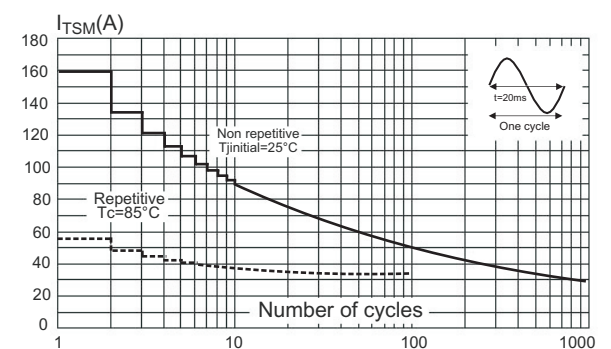


Fig.7. Non-repetitive surge peak on-state current for a sinusoidal

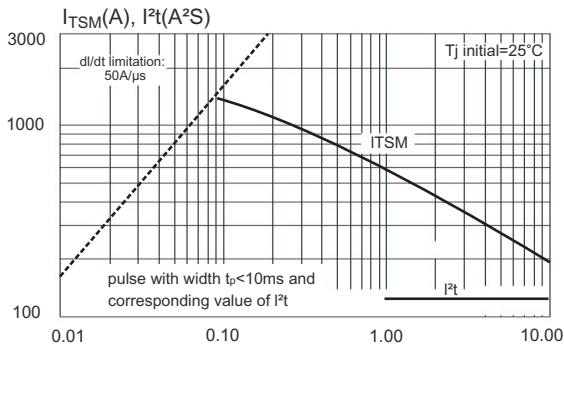


Fig.8 Relative variation of gate trigger current

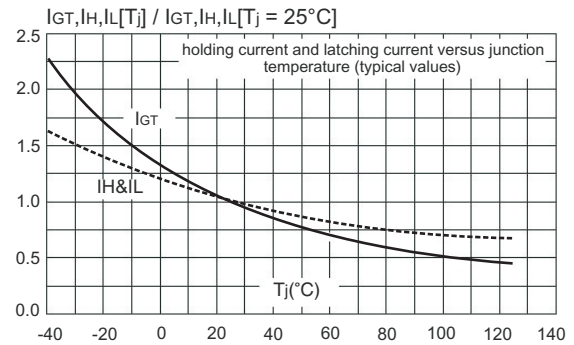


Fig.9 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

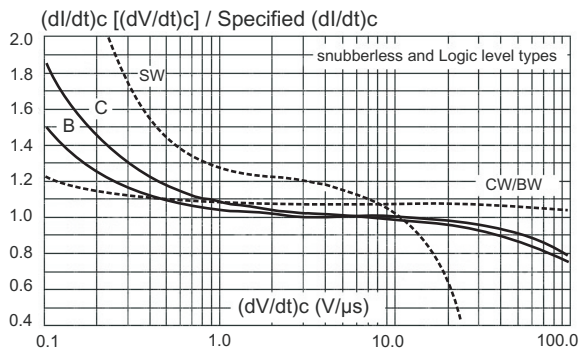


Fig.10 Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

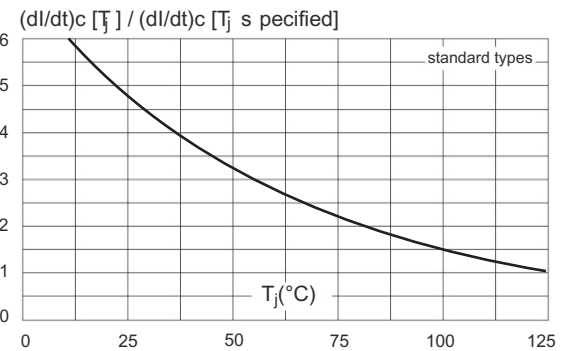
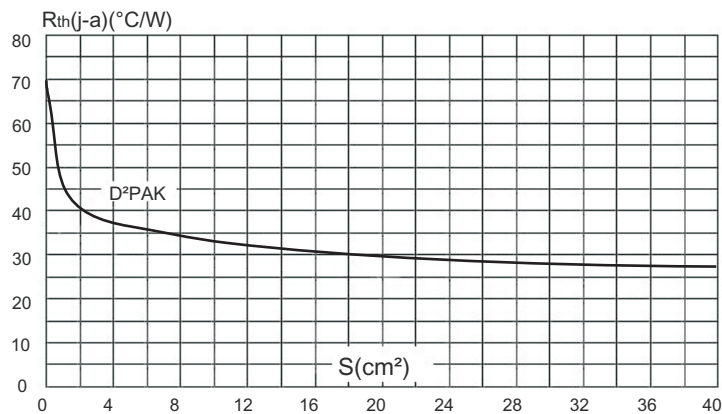
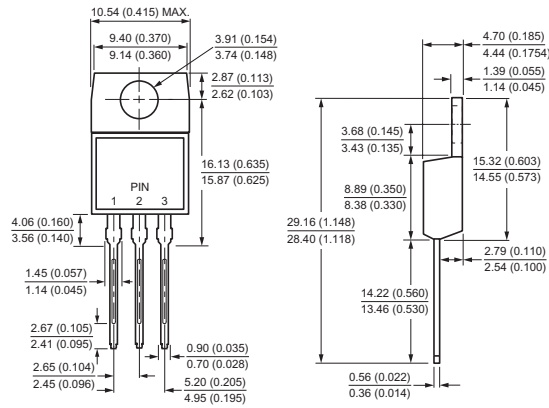


Fig.11 D²PAK thermal resistance junction to ambient versus copper surface under tab (printed circuit FR4, copper thickness: 35μm)

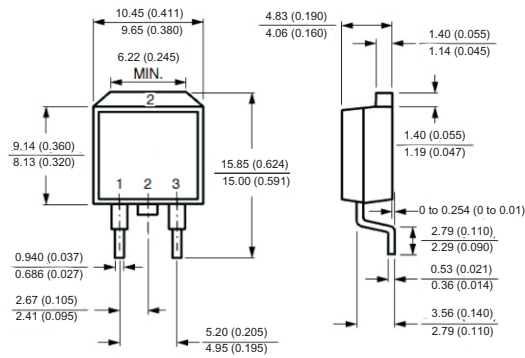


Case Style

TO-220AB



TO-263(D²PAK)



All dimensions in millimeters(inches)

