

## TRSL-9102G / TRSL-9102AG

### 3.3V / 1310 nm / 2.5 Gbps **RoHS Compliant** SFF LC SINGLE-MODE TRANSCEIVER

#### FEATURES

- I Duplex LC Single Mode Transceiver
- I SONET OC-48 SR / SDH STM-16 (I-16) Compliant
- I Fiber Channel 2X/1X SM-LC-L FC-PI Compliant
- I IEEE 802.3z Gigabit Ethernet 1000BASE-LX Compliant
- I Small Form Factor, RJ-45 size, 2X5 pin Package
- I 1310 nm LD Transmitter
- I AC/AC Coupled Signal Input / Output
- I LVTTTL Transmitter Disable Input
- I LVTTTL Signal Detection Output
- I Single +3.3 V Power Supply
- I RoHS Compliant
- I 0 to 70°C Operating : TRSL-9102G
- I **-40 to 85°C Operating: TRSL-9102AG**
- I Wave Solderable and Aqueous Washable
- I Class 1 Laser International Safety Standard IEC-60825 Compliant

#### DESCRIPTION

The TRSL-9102G series single mode transceivers is small form factor, low power, high performance module for bi-directional serial optical data communications such as SONET OC-48 SR / SDH STM-16 (I-16), Gigabit Ethernet and 1X/2X Fiber channel. This module is designed for single mode fiber and operates at a nominal wavelength of 1310 nm. The transmitter section uses a multiple quantum well laser and is a class 1 laser compliant according to International Safety Standard IEC-60825. The receiver section uses an integrated InGaAs detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC. A LVPECL logic interface simplifies interface to external circuitry.

#### LASER SAFETY

This single mode transceiver is a Class 1 laser product. It complies with IEC-60825 and FDA 21 CFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall be terminated with an optical connector or with a dust plug.

#### APPLICATIONS

- I ATM Switches and Routers
- I SONET / SDH Switch Infrastructure
- I XDSL Applications
- I Metro Edge Switching

#### ORDER INFORMATION

P/No.	Bit Rate (Mb/s)	SONET /SDH	Distance (km)	Wavelength (nm)	Package	Temp. (°C)	TX Power (dBm)	RX Sens. (dBm)	RoHS Compliant
TRSL-9102G	2488	SR/I-16	2	1310	2X5 LC	0 to 70	-3 to -9.5	-18	Yes
<b>TRSL-9102AG</b>	2488	SR/I-16	2	1310	2X5 LC	<b>-40 to 85</b>	-3 to -9.5	-18	Yes

Absolute Maximum Ratings					
Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	Tstg	-40	85	°C	
Operating Temperature	Topr	0 -40	70 85	°C	TRSL-9102G TRSL-9102AG
Soldering Temperature	---		260	°C	10 seconds on leads only
Power Supply Voltage	Vcc	0	4.5	V	
Input Voltage	---	GND	Vcc	V	
Output Current	Iout	0	30	mA	

Recommended Operating Conditions					
Parameter	Symbol	Min	Typ	Max	Units / Notes
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Temperature	Topr	0 -40		70 85	°C / TRSL-9102G °C / TRSL-9102AG
Data Rate		622	2488	2670	Mb/s

Transmitter Specifications (0°C < Topr < 70°C, 3.13V < Vcc < 3.47V)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
<b>Optical</b>						
Optical Transmit Power	Po	-9.5	---	-3	dBm	1
Output Center Wavelength	$\lambda$	1270	1310	1360	nm	
Output Spectrum Width	$\Delta\lambda$	---	---	3	nm	RMS ( $\sigma$ )
Extinction Ratio	ER	8.2	---	---	dB	
Output Eye	Compliant with Bellcore GR-253-CORE and ITU recommendation G.957					
Optical Rise Time	t <sub>r</sub>			150	ps	20% to 80% Values
Optical Fall Time	t <sub>f</sub>			150	ps	20% to 80% Values
Relative Intensity Noise	RIN			-120	dB/Hz	
<b>Electrical</b>						
Power Supply Current	I <sub>cc</sub>			140	mA	2
Data Input Current – Low	I <sub>IL</sub>	-350			$\mu$ A	
Data Input Current – High	I <sub>IH</sub>			350	$\mu$ A	
Differential Input Voltage	V <sub>IH</sub> - V <sub>IL</sub>	300			mV	
Data Input Voltage – Low	V <sub>IL</sub> - V <sub>CC</sub>	-2.0		-1.58	V	3
Data Input Voltage -- High	V <sub>IH</sub> - V <sub>CC</sub>	-1.1		-0.74	V	3
Disable Input Voltage -- Low	V <sub>TDIS,L</sub>	0		0.5	V	TX Output Enabled
Disable Input Voltage -- High	V <sub>TDIS,H</sub>	V <sub>cc</sub> - 1.3		V <sub>cc</sub>	V	TX Ouput Disabled
Shut Off Time for TxDis	t <sub>DIS</sub>			1	ms	

- Notes: 1. Output power is power coupled into a 9/125  $\mu$ m single mode fiber.  
 2. Maximum current is specified at Vcc = Maximum @ maximum temperature.  
 3. These inputs are compatible with 10K, 10KH and 100K ECL and PECL inputs.

Receiver Specifications (0°C < Topr < 70°C, 3.13V < Vcc < 3.47V)						
Parameter	Symbol	Min	Typ	Max	Units	Notes
<b>Optical</b>						
Sensitivity	---	---	---	-18	dBm	1
Maximum Input Power	P <sub>in</sub>	-3		---	dBm	
Signal Detect -- Asserted	P <sub>a</sub>	---	---	-18	dBm	Transition: low to high
Signal Detect -- Deasserted	P <sub>d</sub>	-30	---	---	dBm	Transition: high to low
Signal detect -- Hysteresis		1.0	---		dB	
Wavelength of Operation		1100	---	1600	nm	
<b>Electrical</b>						
Power Supply Current	I <sub>cc</sub>			100	mA	2
Data Output Voltage – Low	V <sub>OL</sub> - V <sub>CC</sub>	-2.0		-1.58	V	3
Data Output Voltage – High	V <sub>OH</sub> - V <sub>CC</sub>	-1.1		-0.74	V	3
Signal Detect Output Voltage -- Low	V <sub>OL</sub>			0.8	V	
Signal Detect Output Voltage -- High	V <sub>OH</sub>	2.0			V	

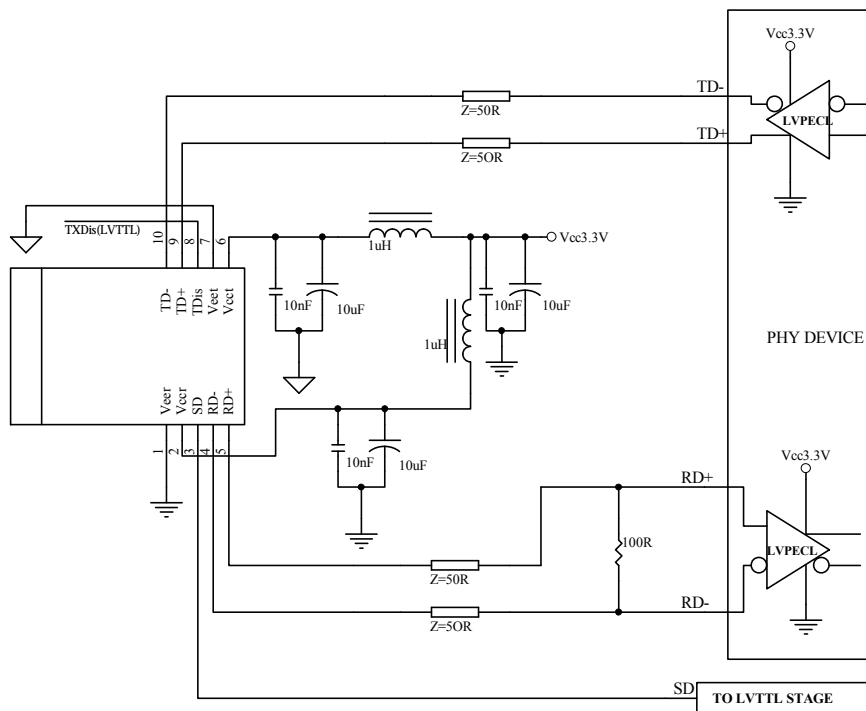
- Notes: 1. Minimum sensitivity and saturation levels at BER=1E-10 for a 2<sup>23</sup>-1 PRBS.  
 2. The current excludes the output load current.  
 3. These outputs are compatible with 10K, 10KH and 100K ECL and PECL outputs.

## CONNECTION DIAGRAM



PIN	Symbol	Notes
1	$V_{EEr}$	Directly connect this pin to the receiver ground plane
2	$V_{CCr}$	+3.3V dc power for the receiver section
3	SD	Active high on this indicates a received optical signal.
4	RD-	Receiver Dataout Bar. See recommended circuit schematic
5	RD+	Receiver Dataout. See recommended circuit schematic
6	$V_{CCt}$	+3.3V dc power for the transmitter section
7	$V_{EEt}$	Directly connect this plan to the transmitter ground plane
8	TxDIs	Transmitter Disable. Connect this pin to +3.3V TTL logic "1" to disable module To enable module connect to TTL logic low "0"
9	TD+	Transmitter Data In. See recommended circuit schematic
10	TD-	Transmitter Data In Bar. See recommended circuit schematic
MS	MS	Mounting Studs. Connect to Chassis Ground

## RECOMMENDED CIRCUIT SCHEMATIC

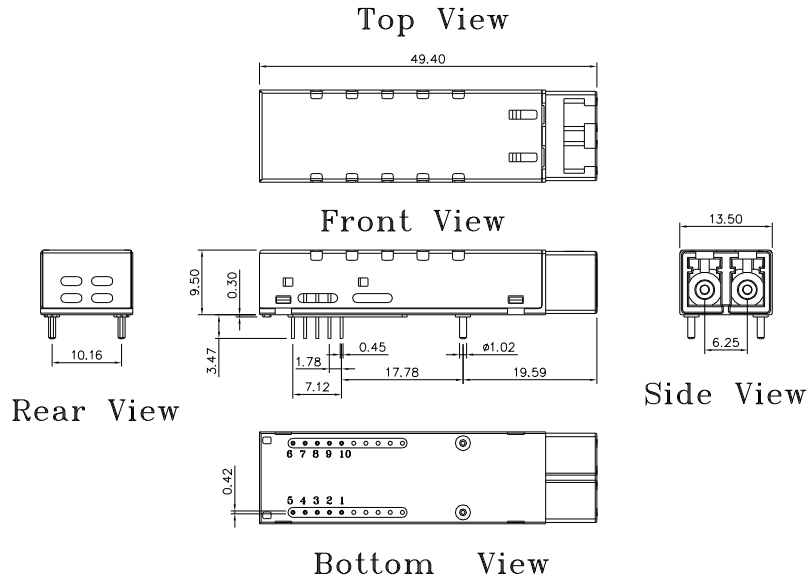


- Note: 1. TX input is terminated inside the module.  
 2. Veer and Veet are not internally connected to each other.  
 3. 50 Ω line pattern and component placements on TD+/TD- and RD+/RD- lines shall be symmetrical for better impedance matching.

PACKAGE DIAGRAM

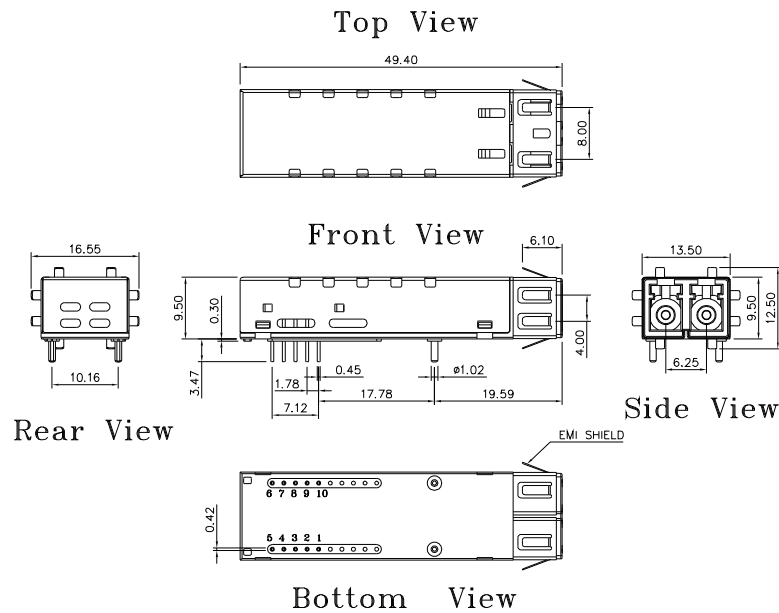
Units in mm

1) Standard Case



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2) Extended Case



TRSL-9102EG / TRSL-9102AEG

**Note:** Specifications subject to change without notice.