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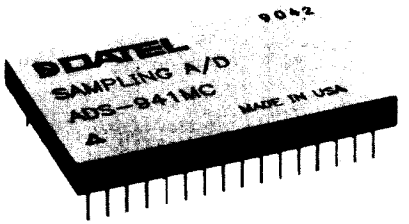
DATEL®
INNOVATION and EXCELLENCE

ADS-941
14-Bit, 1.0 MHz Sampling A/D Converter

FEATURES

- 14-Bit resolution
- 1.0 MHz minimum throughput
- Functionally complete
- Internal reference and Sample/Hold
- -90 dB total harmonic distortion
- -81 dB signal-to-noise ratio
- Full Nyquist-rate sampling
- Small 32-pin DIP
- 2.8 Watts power consumption



GENERAL DESCRIPTION

DATEL's ADS-941 is a functionally complete, 14-bit, 1 MHz, sampling A/D converter. Its standard, 32-pin, triple-wide ceramic DIP contains a fast-settling (250 nanosecond acquisition time) sample/hold amplifier, a 14-bit subranging (two-step) A/D converter, a precision reference, a three-state output register, and all the timing and control logic necessary to operate from a single start convert pulse.

The ADS-941, and the 2 MHz ADS-942, are optimized for wideband frequency-domain applications, and are fully FFT tested. Total harmonic distortion (THD) and signal-to-noise ratio (including distortion) typically run at -90 dB and 81 dB, respectively, with full-scale inputs up to 100 KHz.

The ADS-941 requires ±15V and +5V supplies and typically consumes 2.8 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	ANALOG GROUND	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	CODING SELECT	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	ANALOG GROUND	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT

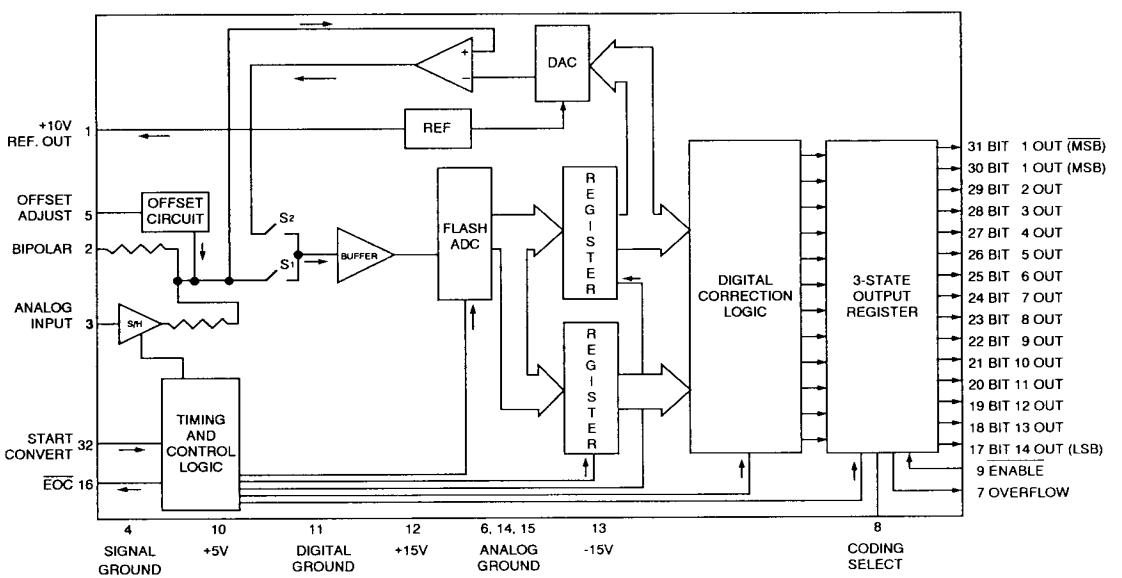


Figure 1. ADS-941 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	-0.3 to +18	Volts dc
-15V Supply (Pin 13)	+0.3 to -18	Volts dc
+5V Supply (Pin 10)	-0.3 to +6.0	Volts dc
Digital Inputs (Pins 8, 9, 32)	-0.3 to V_{DD} +0.3	Volts dc
Analog Input (Pin 3)	±25	Volts
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS ①

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
	—	0 to +10	—	Volts
	—	±5	—	Volts
Input Impedance	2.2	2.5	—	K Ohms
Input Capacitance	—	7	15	pF
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	—	—	Volts dc
Logic "0"	—	—	0.8	Volts dc
Logic Loading "1"	—	—	5.0	µA
Logic Loading "0"	—	—	–600	µA
PERFORMANCE				
Int. Non–Lin. @ f_{IN} = 500 KHz				
+25 °C	—	±1/2	±3/4	LSB
0 to +70 °C	—	±3/4	±1	LSB
–40 to +125 °C	—	±1	±2	LSB
Diff. Non–Lin. @ f_{IN} = 500 KHz				
+25 °C	—	±1/4	±1/2	LSB
0 to +70 °C	—	±1/2	±3/4	LSB
–40 to +125 °C	—	±1	±2	LSB
Full Scale Absolute Accuracy (See Figure 3)				
+25 °C.	—	±0.08	±0.122	%FSR
0 to +70 °C	—	±0.18	±0.36	%FSR
–40 to +125 °C	—	±0.61	±0.85	%FSR
Unipolar Zero Error				
+25 °C (See Figure 3)	—	±0.012	±0.04	%FSR
0 to +70 °C	—	±0.07	±0.13	%FSR
–40 to +125 °C	—	±0.1	±0.17	%FSR
Bipolar Zero Error				
+25 °C (See Figure 3)	—	±0.04	±0.122	%FSR
0 to +70 °C	—	±0.07	±0.18	%FSR
–40 to +125 °C	—	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C(See Figure 3)	—	±0.018	±0.061	%FSR
0 to +70 °C	—	±0.12	±0.3	%FSR
–40 to +125 °C	—	±0.53	±0.73	%FSR
Gain Error (See Figure 3)				
+25 °C	—	±0.018	±0.12	%FSR
0 to +70 °C	—	±0.12	±0.3	%FSR
–40 to +125 °C	—	±0.53	±0.73	%FSR
No Missing Codes 14 Bits @ 500 KHz f_{IN} **Resolution**	Over the Operating Temp. Range. 14 Bits			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding	Straight bin./offset bin./2's Comp. Comp. bin./Comp. offset bin./C2C			
Logic Levels				
Logic "1"	2.4	—	—	Volts dc
Logic "0"	—	—	0.4	Volts dc
Logic Loading "1"	—	—	–160	µA
Logic Loading "0"	—	—	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	—	±13	±30	ppm/ °C
External Current	—	—	5	mA
PERFORMANCE				
Slew Rate	±180	±200	—	V/µSec.
Aperture Delay Time	—	—	10	nSec.
Aperture Uncertainty	—	—	±10	pSec.
S/H Acquisition Time				
(to 0.006%FS (10V step)	—	250	350	nSec.
Total Harm. Distort. (–0.5 dB)				
DC to 100 KHz	–82	–90	—	FS – dB
100 KHz to 500 KHz	–77	–85	—	FS – dB
Signal–to–Noise Ratio (w/o distortion, –0.5 dB)				
DC to 100 KHz	82	90	—	FS – dB
100 KHz to 500 KHz	77	85	—	FS – dB
Signal–to–Noise Ratio & distortion, –0.5 dB				
DC to 100 KHz	76	81	—	FS – dB
100 KHz to 500 KHz	72	76	—	FS – dB
Spurious Free Dynamic Range ②				
DC to 100 KHz	83	92	—	dB
100 to 500 KHz	79	87	—	dB
Effective Bits, –0.5 dB				
DC to 100 KHz	—	13.1	—	Bits
100 KHz to 500 KHz	—	12.3	—	Bits
Two–tone Intermodulation Distortion f_{IN} = 100 KHz, 240 KHz, Fs=1.0 MHz, –0.5 dB)	–92	—	—	FS – dB
Input Bandwidth				
Small Signal (–20 dB)	6	—	—	MHz
Full Power (0 dB)	1.75	—	—	MHz
Feedthrough Rejection @ f_{IN} = 500 KHz	–87	—	—	dB
Overvoltage Recovery, ±12V	—	1000	2000	nSec.
A/D Conversion Rate	1.0	1.1	—	MHz
Noise	—	—	250	µV rms
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
–15V dc Supply	–14.25	–15.0	–15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	—	+62	+85	mA
–15V dc Supply	—	–80	–95	mA
+5V dc Supply ③	—	+140	+160	mA
Power Dissipation	—	2.8	3.3	Watts
Power Supply Rejection	—	—	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
–MC, ambient	0	—	+70	°C
–ME, case	–40	—	+125	°C
Storage Temperature Range	–65	—	+150	°C
Package Type	32–pin hermetic sealed, ceramic TDIP			
Weight	0.42 ounces (12 grams)			

① Warm-up time of 7 minutes to Full Specifications.
② Same specification for In-Band Harmonics
③ +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

2. Bypass the analog and digital supplies and the +10V REF. OUT (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

3. CODING SELECT (pin 8) is compatible with CMOS/TTL logic levels for those users desiring logic control of this function. The device has an internal pull-up resistor on this pin, allowing pin 8 to be connected to +5V or left open when a logic 1 is needed. See the Calibration Procedure for applicable connections for a particular coding.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to START CONVERT (pin 32) at a rate of 200 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1 1/2 LSB
0 to +10V	+305 µV	+9.999085V
±5V	+305 µV	+4.999085V

2. Zero Adjustments
   Apply a precision voltage reference source between ANALOG INPUT (pin 3) and SIGNAL GROUND (pin 4), then adjust the reference source output per Table 2.

   For unipolar, adjust the zero trimpot so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with CODING SELECT (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied high (complementary binary).

   For bipolar operation, adjust the trimpot until the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied low (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied high (complementary offset binary).

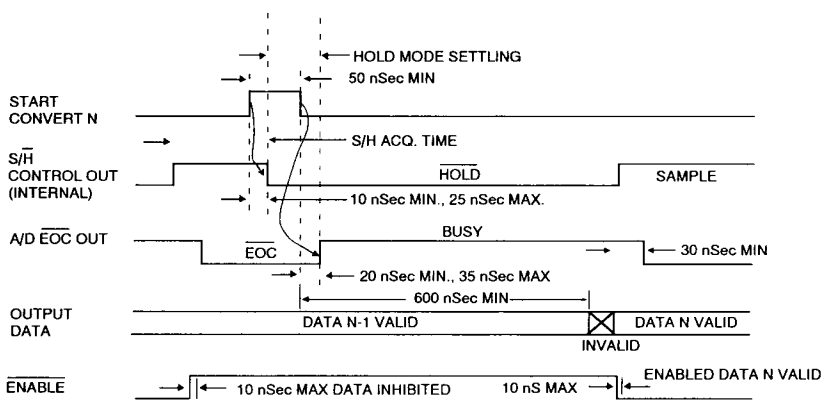
   Two's complement coding requires using BIT 1 OUT (MSB) (pin 31). With pin 8 tied low, adjust the trimpot until the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimpot until the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied low for straight binary/offset binary or between 00 0000 0000 0000 and 00 0000 0000 0001 with pin 8 tied high for complementary binary / complementary offset binary.

   Two's complement coding requires using pin 31. With pin 8 tied low, adjust the gain trimpot until the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

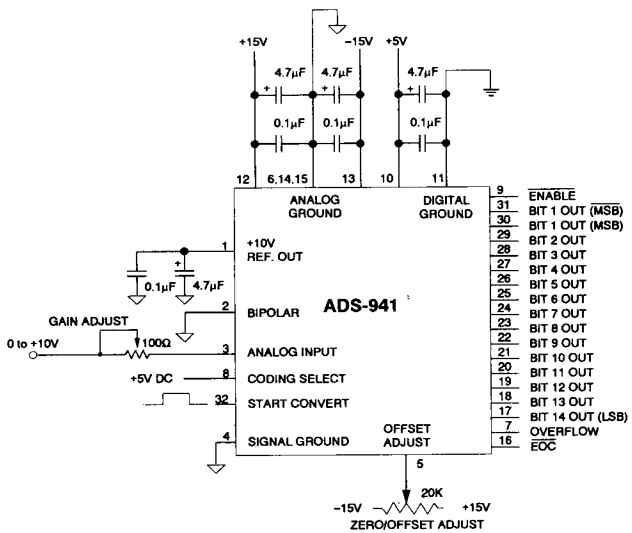


NOTES:
1 - Retriggering the START CONVERT pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.
2 - The specifications listed apply over the full operating temperature range unless otherwise specified.
3 - Not drawn to scale.

Figure 2. ADS-941 Timing Diagram

Table 3. Output Coding

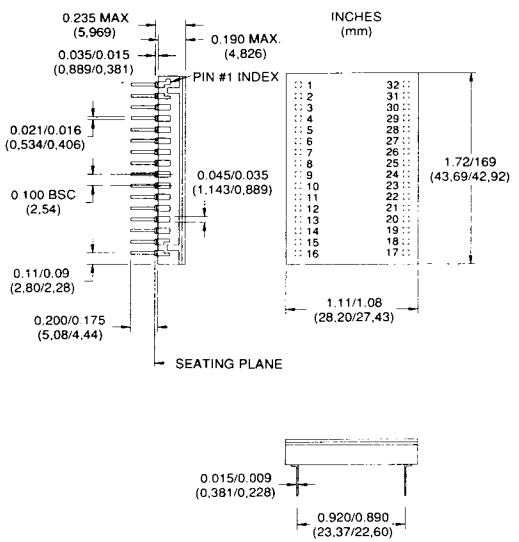
UNIPOLAR SCALE	INPUT RANGE 0 to +10V	STRAIGHT BIN. OUTPUT CODING MSB LSB	COMP. BINARY OUTPUT CODING MSB LSB	OFF. BINARY / TWO'S COMP. OUTPUT CODING MSB LSB	INPUT RANGE ±5V	BIPOLAR SCALE
FS -1 LSB	+9.999390	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	+4.999390	+FS -1 LSB
7/8 FS	+8.750000	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	+3.750000	+3/4 FS
3/4 FS	+7.500000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	+2.500000	+1/2 FS
1/2 FS	+5.000000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.000000	0
1/4 FS	+2.500000	01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000	-2.500000	-1/2 FS
1/8 FS	+1.250000	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	-3.750000	-3/4 FS
1 LSB	+0.000610	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	-4.999390	-FS +1 LSB
0	0.000000	00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000	-5.000000	-FS



NOTE: Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 100 Ω trimpot in series with the analog input for gain adjustment. Use a fixed 50 Ω resistor instead of the trimpot for operation without adjustment. Use a 20K trimpot with the wiper tied to OFFSET ADJUST (pin 5) for zero/offset adjustment. Connect pin 5 to ANALOG GROUND (pin 6) for operation without zero/offset adjustment.

Figure 3. Typical ADS-941 Connection Diagram

MECHANICAL DIMENSIONS INCHES (MM)



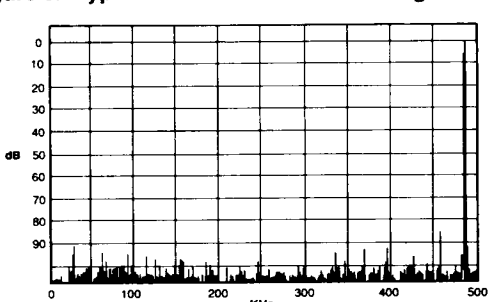


Figure 4. FFT Analysis of ADS-941
(FS = 1.0 MHz, f_{IN} = 480 KHz, -0.5 dB of Full Scale input)

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-941MC	0 °C to +70 °C	Hermetic
ADS-941ME	-40 °C to +125 °C	Hermetic
ACCESSORY	ADS-EVAL4	Evaluation Board (without ADS-941)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

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