ANALOG DEVICES

Stereo, Single-Supply 18-Bit Integrated ΣΔ DAC

AD1859

FEATURES

- Complete, Low Cost Stereo DAC System in a Single Die Package
- Variable Rate Oversampling Interpolation Filter
- Multibit ΣΔ Modulator with Triangular PDF Dither
- Discrete and Continuous Time Analog Reconstruction Filters
- Extremely Low Out-of-Band Energy
- 64 Step (1 dB/Step) Analog Attenuator with Mute
- Buffered Outputs with 2 kΩ Output Load Drive
- Rejects Sample Clock Jitter
- 94 dB Dynamic Range, –88 dB THD+N Performance
- Option for Analog De-emphasis Processing with External Passive Components
- ±0.1° Maximum Phase Linearity Deviation
- Continuously Variable Sample Rate Support
- Digital Phase Locked Loop Based Asynchronous Master Clock
- On-Chip Master Clock Oscillator, Only External Crystal Is Required
- Power-Down Mode
- Flexible Serial Data Port (I^2S-Justified, Left-Justified, Right-Justified and DSP Serial Port Modes)
- SPI* Compatible Serial Control Port
- Single +5 V Supply
- 28-Pin SOIC and SSOP Packages

APPLICATIONS

- Digital Cable TV and Direct Broadcast Satellite Set-Top Decoder Boxes
- Digital Video Disc, Video CD and CD-I Players
- High Definition Televisions, Digital Audio Broadcast Receivers
- CD, CD-R, DAT, DCC, ATAPI CD-ROM and MD Players
- Digital Audio Workstations, Computer Multimedia Products

*SPI is a registered trademark of Motorola, Inc.

PRODUCT OVERVIEW

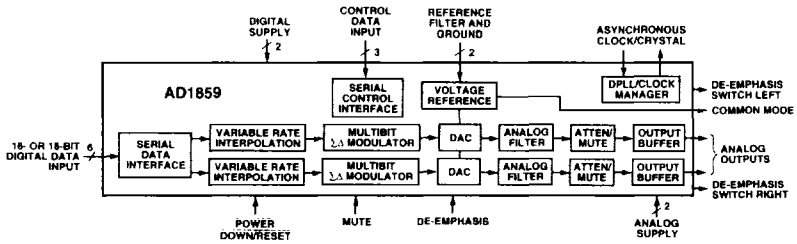
The AD1859 is a complete 16-/18-bit single-chip stereo digital audio playback subsystem. It comprises a variable rate digital interpolation filter, a revolutionary multibit sigma-delta (ΣΔ) modulator with dither, a jitter-tolerant DAC, switched capacitor and continuous time analog filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port.

The key differentiating feature of the AD1859 is its asynchronous master clock capability. Previous ΣΔ audio DACs required a high frequency master clock at 256 or 384 times the intended audio sample rate. The generation and management of this high frequency synchronous clock is burdensome to the board level designer. The analog performance of conventional single bit ΣΔ DACs is also dependent on the spectral purity of the sample and master clocks. The AD1859 has a digital Phase Locked Loop (PLL) which allows the master clock to be asynchronous, and which also strongly rejects jitter on the sample clock (left/right clock). The digital PLL allows the AD1859 to be clocked with a single frequency (27 MHz for example) while the sample frequency (as determined from the left/right clock) can vary over a wide range. The digital PLL will lock to the new sample rate in approximately 100 ms. Jitter components 15 Hz above and below the sample frequency are rejected by 6 dB per octave. This level of jitter rejection is unprecedented in audio DACs.

The AD1859 supports continuously variable sample rates with essentially linear phase response, and with an option for external analog de-emphasis processing. The clock circuit includes an on-chip oscillator, so that the user need only provide an external crystal. The oscillator may be overdriven, if desired, with an external clock source.

The AD1859 has a simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The serial data input port can be configured in left-justified, I^2S-justified, right-justified and DSP serial port compatible modes. The AD1859 accepts 16- or 18-bit serial audio data in MSB-first, twos-complement format. A power-down mode is offered to minimize power consumption when the device is inactive. The AD1859 operates from a single +5 V power supply. It is fabricated on a single monolithic integrated circuit using a 0.6 μM CMOS double polysilicon, double metal process, and is housed in 28-pin SOIC and SSOP packages for operation over the temperature range –40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1859JR	0°C to +70°C	28-Lead SOIC	R-28
AD1859JRS	0°C to +70°C	28-Lead SSOP	RS-28

*For outline information see Package Information section.

PIN CONNECTIONS