Preliminary Product Information

NEC

MOS Integrated Circuit

78K0/KB2

8-BIT SINGLE-CHIP MICROCONTROLLER

The 78K0/KB2 products are 8-bit single-chip microcontrollers of the 78K0 series.

These microcontrollers feature Single-voltage Self-programming Flash memory and many peripherals.

FEATURES

- 78K0 CPU core, 8-bit CISC architecture
- Flash EEPROM and RAM sizes

Item / Product name	Program memory (Flash ROM)	Data memory (RAM)
μPD78F0503	32K bytes (Flash)	1K bytes
μPD78F0502	24K bytes (Flash)	1K bytes
μPD78F0501	16K bytes (Flash)	768 bytes
μPD78F0500	8K bytes (Flash)	512 byte

Minimum instruction cycle

0.1μs (20MHz@4.0V to 5.5V)

0.2μs (10MHz@2.7V to 5.5V)

0.4μs (5MHz@1.8V to 5.5V)

Clock

- MAIN CLOCK
  - Internal High-speed-oscillator 8MHz (Typ.)
  - Ceramic/Crystal Oscillator/External CLK (1MHz to 20MHz)
    (Instruction execution time = 100ns(min.) @20MHz)
- WDT CLOCK
  - Internal Low-speed-oscillator 240KHz (Typ.)

Peripherals.

- On-Chip Power-On-Clear (POC) Circuit
- Low-Voltage Detector (LVI) Circuit
- Timer
  - 16bit Timer 1ch
  - 8bit Timer 4ch
  - Watchdog Timer (Operable with 240KHz Internal-Low-speed -oscillator)
- Serial Interface
  - UART/CSI 1ch
  - UART (with LIN-bus) 1ch
  - IIC 1ch
- AD CONVERTER
  - 10-bit resolution A/D converter 4 ch
- I/O PORT

  Total : 23

  CMOS I/O : 21

  N-ch O.D I/O: 2
- Other
  - Self programming
  - On-chip debug function (μPD78F0503D only)

Interrupt

- Internal 16ch
- External 6ch

Operation Voltage

1.8V to 5.5V

Package

30-pin SSOP (7.62mm(300))

ZUD-CC-04-0125-E
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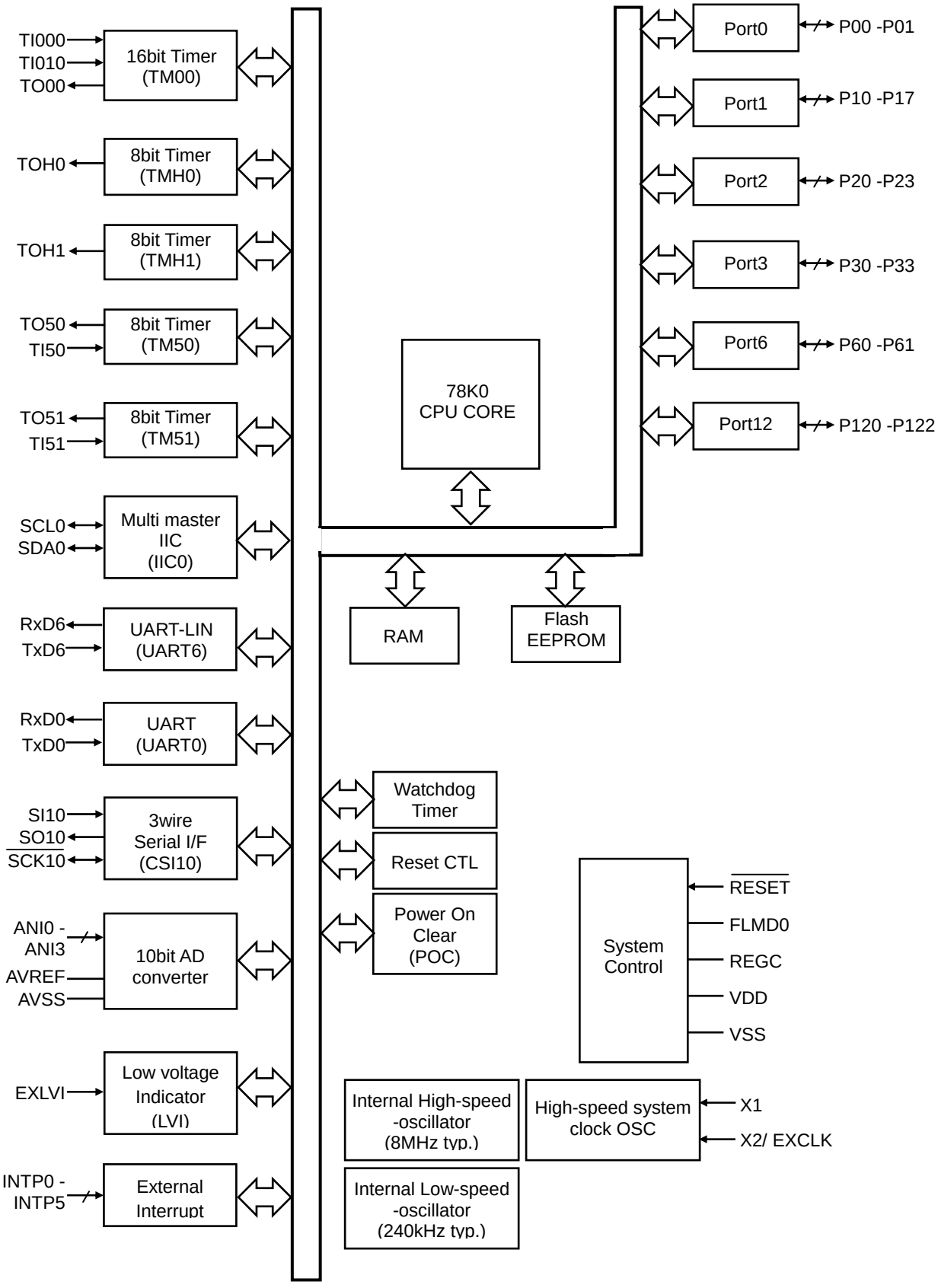
1. Block Diagram

Fig. 78K0/KB2



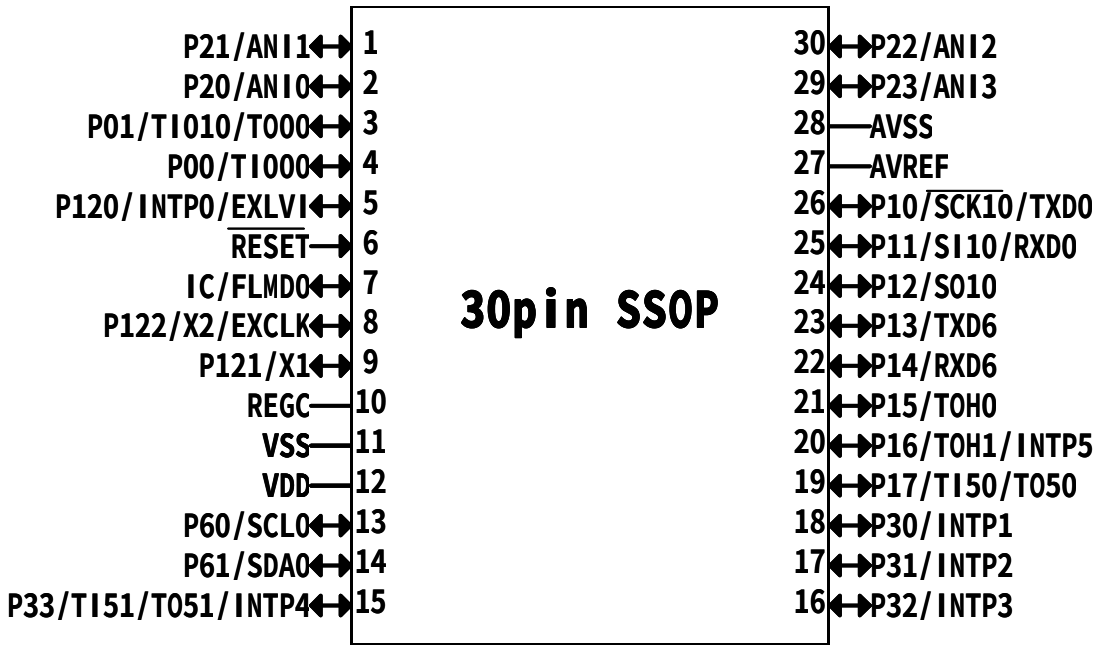
2. Pin Lay Out

78K0/KB2

30-pin plastic SSOP (7.62mm(300))

μPD78F0500MC-5A4, μPD78F0501MC-5A4

μPD78F0502MC-5A4, μPD78F0503MC-5A4



3. Pin Function

Table (1/2)

PIN NAME	Function
VDD	Positive power supply except for ports (except P20-P23) and AD converter
VSS	Ground potential except for ports (except P20-P23) and AD converter
RESET	System reset input
FLMD0	Flash EEPROM programming mode setting
REGC	Connecting regulator output stabilization capacitor. Connect to GND via a capacitor (0.47μF)
AVREF	A/D converter analog power supply and power supply for P20-P23
AVSS	Ground potential for A/D converter and P20 - P23.
P00	I/O port
/TI000	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of16-bit timer/event counter 00 (TM00)
P01	I/O port
/TI010	Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00 (TM00)
/TO00	16-bit timer/event counter 00 output (TM00)
P10	I/O port
/SCK10	Clock input/ output for serial interface (CSI10)
/TXD0	Serial data output from asynchronous serial interface (UART0)
P11	I/O port
/SI10	Serial data input to serial interface (CSI10)
/RXD0	Serial data input to asynchronous serial interface (UART0)
P12	I/O port
/SO10	Serial data output form serial interface (CSI10)
P13	I/O port
/TXD6	Serial data output from asynchronous serial interface (UART6)
P14	I/O port
/RXD6	Serial data input to asynchronous serial interface (UART6)
P15	I/O port
/TOH0	8-bit timer H0 output (TMH0)
P16	I/O port
/TOH1	8-bit timer H1 output (TMH1)
/INTP5	External interrupt request input with specifiable valid edges
P17	I/O port
/TI50	External count clock input to 8-bit timer/event counter 50 (TM50)
/TO50	8-bit timer/event counter 50 output (TM50)

Table(2/2)

PIN NAME	Function
P20- P23 / ANI0- ANI3	I/O ports A/D converter analog input
P30/INTP1	I/O port External interrupt request input with specifiable valid edges
P31/INTP2	
P32/INTP3	
P33 /TI51 /TO51 /INTP4	I/O port
	External count clock input to 8-bit timer/event counter 51(TM51)
	8-bit timer/event counter 51output (TM51)
	External interrupt request input with specifiable valid edges
P60 /SCL0	I/O port (N-ch Open drain)
	Clock input/ output for serial interface (IIC0)
P61 /SDA0	I/O port (N-ch Open drain)
	Serial data input/ output for serial interface (IIC0)
P120 /INTP0 /EXLVI	I/O port
	External interrupt request input with specifiable valid edges
	Reference voltage input for Low voltage Indicator
P121 /X1	I/O port (An external oscillation circuit is not used)
	Connecting resonator for main system clock oscillation
P122 /X2 /EXCLK	I/O port (An external oscillation circuit is not used)
	Connecting resonator for main system clock oscillation
	External clock input for main system clock

4. Memory space

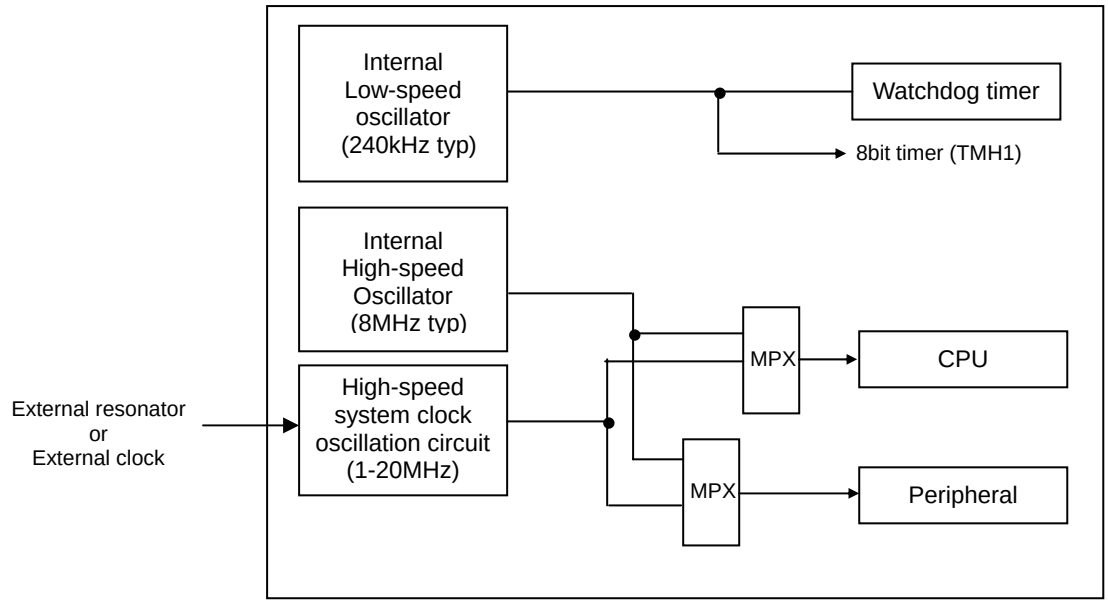
78K0/KB2 have 64kB linear address area.

Products	ROM size	Common ROM	Bank ROM	
		Address	Address	Number of Bank
μPD78F0503	32KB	0000H-7FFFH (32KB)	-	-
μPD78F0502	24KB	0000H-5FFFH (24KB)	-	-
μPD78F0501	16KB	0000H-3FFFH (16KB)	-	-
μPD78F0500	8KB	0000H-1FFFH (8KB)	-	-

5. Clock

78K0/KB2 have 2 type internal oscillator and 2 type external resonator oscillation circuit.
78K0/KB2 can be operated Internal High-speed oscillator only. Internal Low-speed oscillator can connect to Watch dog timer and 8bit timer (TMH1) only for high secure.

Fig. Clock connecting block image



6. Outline of Functions of KB2

		μPD78F0500	μPD78F0501	μPD78F0502	μPD78F0503
Internal Memory (Byte)	Flash Memory	8 K	16K	24K	32 K
	Bank	-	-	-	-
	High Speed RAM	512	768	1K	
	Extend RAM	-			
Main System Clock	Ceramic/Crystal	- 1 to 20 MHz: V_{DD} = 4.0 to 5.5 V - 1 to 10 MHz: V_{DD} = 2.7 to 5.5 V - 1 to 5 MHz: V_{DD} = 1.8 to 5.5 V			
	Internal oscillator	- 8 MHz(TYP.)			
Sub System Clock		-			
Internal Low Speed oscillator (For TMH1, WDT)		- 240 kHz(TYP.)			
Minimum Instruction Cycle		- 0.1 μs (Ceramic/ Crystal Operation f_{XH} = 20 MHz V_{DD} = 4.0 to 5.5 V)			
I/O		Total :23 - CMOS I/O :21 - N-ch O.D. :2			
Timer		- 16 Bit Timer/Event Counter:1ch - 8 Bit Timer/Event Counter:2ch - 8 bit Timer:2ch - Watch Dog Timer:1ch			
	Timer Output	-5(PWM:3)			
PCL output		-			
Buzzer Output		-			
A/D Converter		- 10bit x 4ch			
Serial Interface		- UART (with LIN-bus):1ch - CSI/ UART:1ch - I^2C:1ch			
Multiplier/Divider		-			
Interrupt	Internal	16			
	External	6			
Key Return		-			
On Chip Debug Function		Product name undecided			
Voltage Range		V_{DD} = 1.8 to 5.5 V			
Operation temperature		Ta = -40°C to +85°C			
Package		- 30pin SSOP(7.62mm(300))			

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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