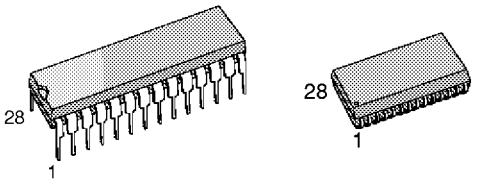
SGS-THOMSON MICROELECTRONICS

MK48S74

VERY FAST CMOS 8K x 8 CACHE TAGRAM

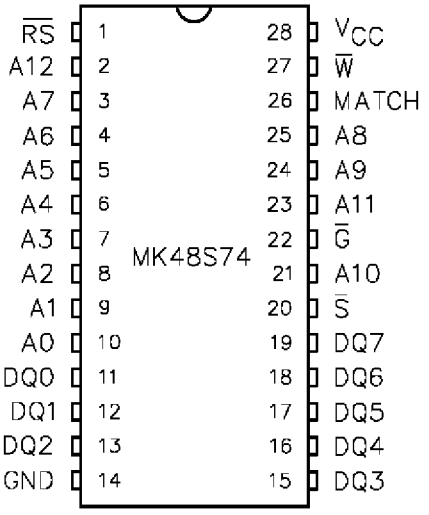
- 8K x 8 CMOS SRAM with ONBOARD COMPARATOR
- ADDRESS to COMPARE ACCESS TIME: 20, 25, 35ns
- FAST CHIP SELECT COMPARE ACCESS 10ns
- MATCH OUTPUT with FAST TAG DATA to COMPARE ACCESS of 12ns Max
- STATIC OPERATION - NO CLOCKS or TIMING STROBES REQUIRED
- ALL INPUTS and OUTPUTS ARE FULLY TTL COMPATIBLE
- FULL CMOS for LOW POWER OPERATION
- OPEN DRAIN MATCH OUTPUT
- 28 PIN 300 MIL DIP & 28 PIN 300 MIL SOJ



PSDIP28 (N)

SOJ28 (X)
300 mils

Figure 1. Pin Connection



VA00625

TRUTH TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	$\overline{RS}$	Mode	DQ	Match
X	X	X	L	Reset Clear	High-Z	Invalid
X	H	X	H	Deselect	High-Z	Invalid
H	L	H	H	Miss	D_{IN}	Low
H	L	H	H	Match	D_{IN}	High-Z
H	L	L	H	Read	Q_{OUT}	Invalid
L	L	X	H	Write	D_{IN}	Invalid

Note: MATCH is High-Z during an invalid state

PIN NAMES

A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs / Outputs
MATCH	Comparator Output
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RS}$	Rest Flash Clear
V_{CC}, GND	5 Volts, Ground

DESCRIPTION

The MK48S74 is a 65, 536 fast static cache TAGRAM™ organized as 8K x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance HCMOS4 technology. The MK48S74 features fully static operation requiring no external clocks or timing strobes, and equal access and cycle times. The device requires a single 5V ± 5 % supply and is fully TTL compatible. The MK48S74 has a fast Chip Select control for high speed operation to the Match Compare valid, and device select/deselect operations. Additionally, the MK48S74 provides a Reset Clear, and MATCH compare pin. The Reset Clear input provides an asynchronous RAM clear control which clears all internal RAM bits to zero in only two cycles. The MATCH output features an open drain for wired-OR operations. During a MATCH compare cycle, an on-board 8-bit comparator compares the Data Inputs (8-bit TAG) at the specified address index (A0-A12) to the internal RAM data. If a miss condition exists, where at least one bit of TAG data does not match the internal RAM, then the MATCH output issues a LOW miss signal.

OPERATIONS

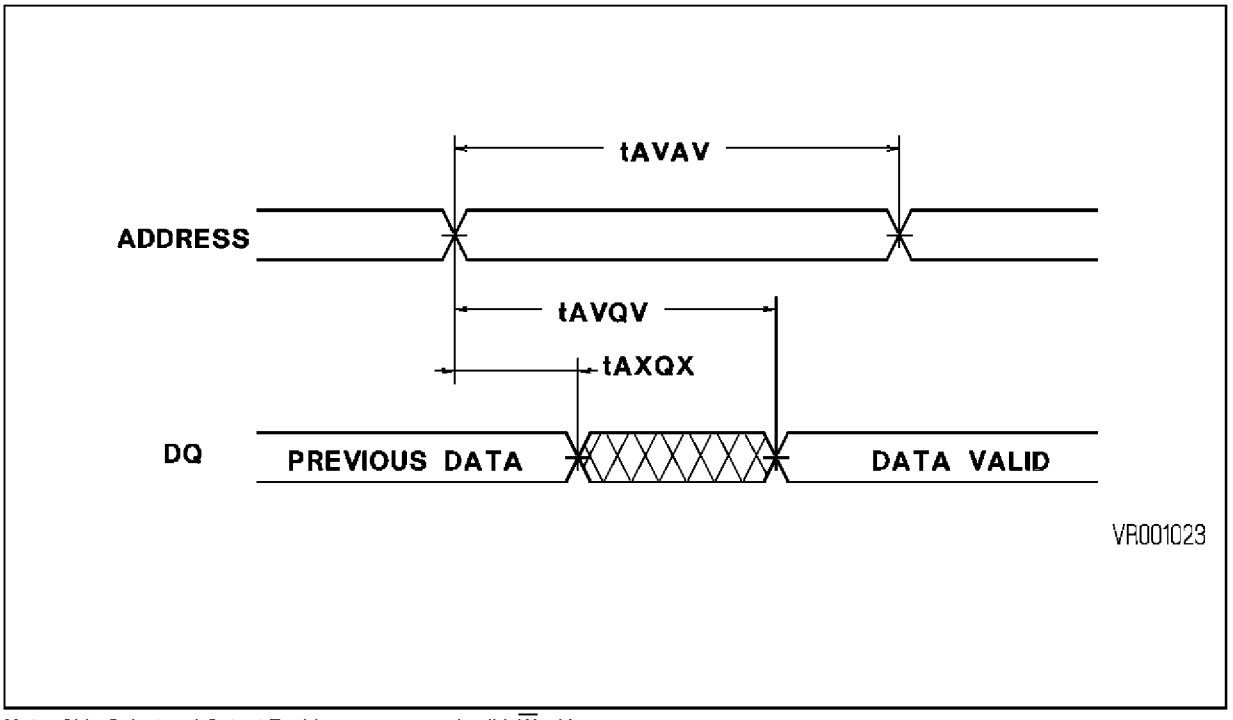
READ MODE

The MK48S74 is in the read mode whenever Write Enable ($\overline{W}$) is HIGH with Output Enable ($\overline{G}$) LOW and Chip Select ($\overline{S}$) is active. This provides access to data from eight of 65, 536 locations in the static memory array. The unique address specified by the 13 address inputs defines which one of the 8192-8-bit bytes is to be accessed. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is LOW and $\overline{S}$ is LOW. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{SLQV} or t_{GLQV} rather than the addresses. The state of the DQ pins is controlled by the $\overline{S}$, $\overline{G}$ and $\overline{W}$ control signals. Data out may be inderterminate at t_{SLQX} and t_{GLQX} but data lines will always be valid at t_{AVQV}.

READ CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \leq T_A \leq +70°C$; $V_{CC} = 5V \pm 5\%$)

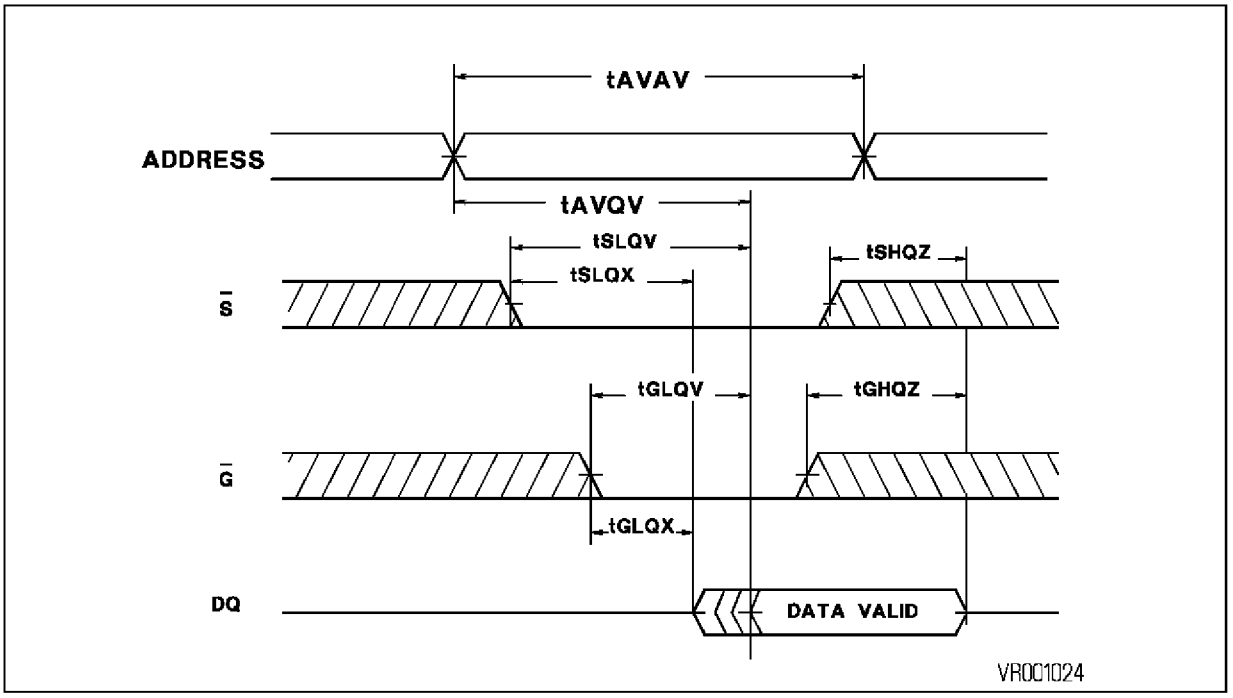
Symbol		Parameter	20		25		35		Unit	Notes
Std	Alt		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{RC}	Read Cycle Time	20		25		35		ns	
t_{AVQV}	t_{AA}	Address Access Time		20		25		35	ns	1
t_{SLQV}	t_{CSA}	Chip Select Access Time		15		15		20	ns	
t_{GLQV}	t_{OEA}	Output Enable Access Time		15		15		20	ns	1
t_{SLQX}	t_{CSL}	Chip Select to Output Low-Z	0		0		0		ns	
t_{GLQX}	t_{OEL}	Output Enable to Low-Z	0		0		0		ns	
t_{SHQZ}	t_{CSZ}	Chip Select to High-Z		9		9		9	ns	
t_{GHQZ}	t_{OEZ}	Output Enable to High-Z		8		8		8	ns	2
t_{AXQX}	t_{OH}	Output Hold From Address Change	3		3		3		ns	1

Figure 2. Read Timing No. 1 (Address Access)



Note: Chip Select and Output Enable one presumed valid, $\overline{W} = V_{IH}$

Figure 3. Read Timing No. 2 ($W = V_{IH}$)



WRITE MODE

The MK48S74 is the Write mode whenever the $\overline{W}$ and $\overline{S}$ pins are LOW. Chip Select or $\overline{W}$ must be inactive during address transitions. The Write begins with the concurrence of Chip Select being active with $\overline{W}$ LOW. Therefore address setup times are referenced to Write Enable and Chip Select as t_{AVWL} and t_{AVSL} and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{S}$ or $\overline{W}$. If the outputs are enabled ($\overline{S}$ = LOW, $\overline{G}$ = LOW), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{S}$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{S}$ or $\overline{W}$.

WRITE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
($0°C \le T_A \le +70°C$; $V_{CC} = 5V \pm 5\%$)

Symbol		Parameter	20		25		35		Unit	Notes
Std	Alt		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVAV}	t_{WC}	Write Cycle Time	20		25		35		ns	
t_{AVWL}	t_{AS}	Address Set-up to Write Enable Low	0		0		0		ns	
t_{AVSL}	t_{AS}	Address Set-up to Chip Select	0		0		0		ns	
t_{AVWH}	t_{AW}	Address Valid to End of Write	15		20		25		ns	
t_{WLWH}	t_{WEW}	Write Pulse Width	15		20		25		ns	
t_{WHAX}	t_{AH}	Address Hold Time After End of Write	0		0		0		ns	
t_{SLSH}	t_{CSW}	Chip Select to End of Write	15		20		25		ns	
t_{SHAX}	t_{WR}	Write Recovery Time To Chip Select	0		0		0		ns	
t_{DVWH}	t_{DW}	Data Valid to End of Write	10		13		15		ns	
t_{WHDX}	t_{DH}	Data Hold Time	0		0		0		ns	
t_{WHQX}	t_{WEL}	Write High to Output Low-Z (Active)	0		0		0		ns	2
t_{WLQZ}	t_{WEZ}	Write Enable to Output High-Z		5		5		5	ns	2

Figure 4. Writing Timing No.1 (Write Control)

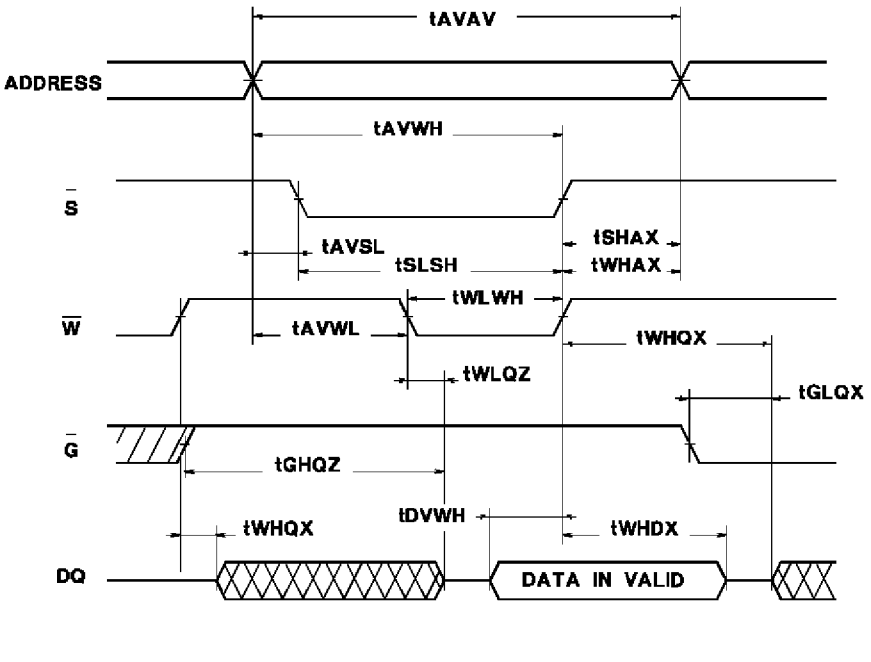
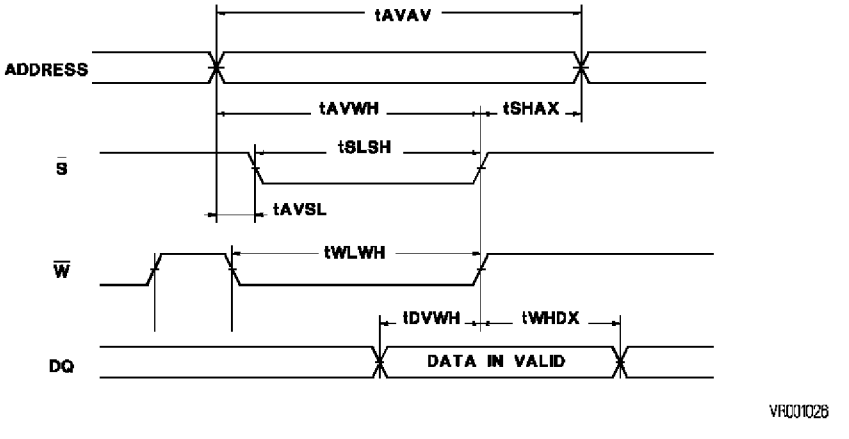


Figure 5. Writing Timing No. 2 (Chip Select Control)



Note: $\overline{G}$ = V_{IH}

COMPARE MODE

THe MK48S74 is in the Compare mode whevenver $\overline{W}$ and $\overline{G}$ are HIGH provided Chip Select ($\overline{S}$) is active LOW. The 13 index address inputs (A0-A12) define a unique location in the static RAM array. The data presented on the Data Inputs (DQ0-DQ7) as Tag Data is compared to the internal RAM data as specified by the index. If all bits are equal, then a hit condition occurs (MATCH = High-Z). When at least one bit is not equal, the MATCH will go LOW signifying a miss condition. The MATCH output will be valid t_{AVMV} from stable address, or t_{TVMV} from valid Tag Data when $\overline{S}$ is LOW. Should the address be stable with valid Tag Data, and the device is deselected ($\overline{S}$ = HIGH), then MATCH will be valid t_{SLMV} from the falling edge of Chip Select ($\overline{S}$). When executing a write-to-compare cycle ($\overline{W}$ = LOW, $\overline{G}$ = LOW or HIGH), MATCH will be valid t_{WHMV} or t_{GHMV} from the latter rising edge of $\overline{W}$ or $\overline{G}$ respectively.

RESET MODE

The MK48S74 allows an asynchronous reset clear whevever $\overline{RS}$ is LOW regardless of the logic state on the other input pins. Reset clears all internal RAM bits (65, 536 bits) to a logic zero as long as $t_{RSL-RSH}$ is satisfied. The MATCH output will go HIGH-Z t_{RSL-MH} from the falling edge of $\overline{RS}$ and all inputs will not be recongnized until t_{RSH-AV} from the rising edge of reset ($\overline{RS}$).

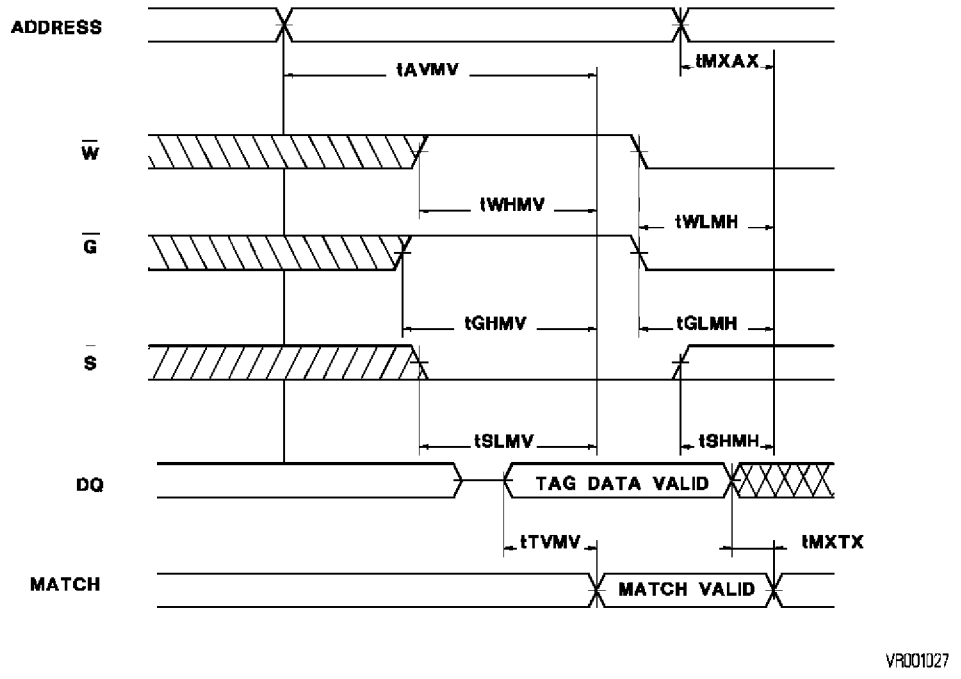
COMPARE CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions

Symbol		Parameter	20		25		35		Unit	Notes
Std	Alt		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AVMV}	t_{AMA}	Address to MATCH Valid		20		25		35	ns	3
t_{SLMV}	t_{CSM}	Chip Select to MATCH Valid		10		15		15	ns	3
t_{SHMH}	t_{CSMH}	Chip Deselect to MATCH High-Z		8		12		12	ns	3
t_{TVMV}	t_{DMA}	Tag Data to MATCH Valid		12		15		15	ns	3
t_{GHMV}	t_{OEM}	$\overline{G}$ High to MATCH Valid		10		15		15	ns	3
t_{GLMH}	t_{OEMH}	$\overline{G}$ Low to MATCH High-Z		10		12		12	ns	3
t_{WHMV}	t_{WEM}	$\overline{W}$ High to MATCH Valid		10		20		20	ns	3
t_{WLMH}	t_{WEMH}	$\overline{W}$ Low to MATCH High-Z		10		15		15	ns	3
t_{MXAX}	t_{MHA}	MATCH Hold From Address	2		2		2		ns	3
t_{MXTX}	t_{MHD}	MATCH Hold From Tag Data	0		0		0		ns	3

RESET CYCLE TIMING - Electrical Characteristics and Recommended AC Operating Conditions
(0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 5%)

Symbol		Parameter	20		25		35		Unit	Notes
Std	Alt		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RSC}	t_{RC}	Flash Clear Cycle Time	80		80		100		ns	
t_{RSL-AX}	t_{RSX}	Reset Clear ($\overline{RS}$) to Inputs Don't Care	0		0		0		ns	
t_{RSH-AV}	t_{RSV}	$\overline{RS}$ to Inputs Valid	5		5		5		ns	
$t_{RSL-RSH}$	t_{RSP}	Reset ($\overline{RS}$) Pulse Width	75		75		95		ns	
t_{RSL-MH}	t_{RSM}	Reset ($\overline{RS}$) to MATCH High-Z		15		15		15	ns	

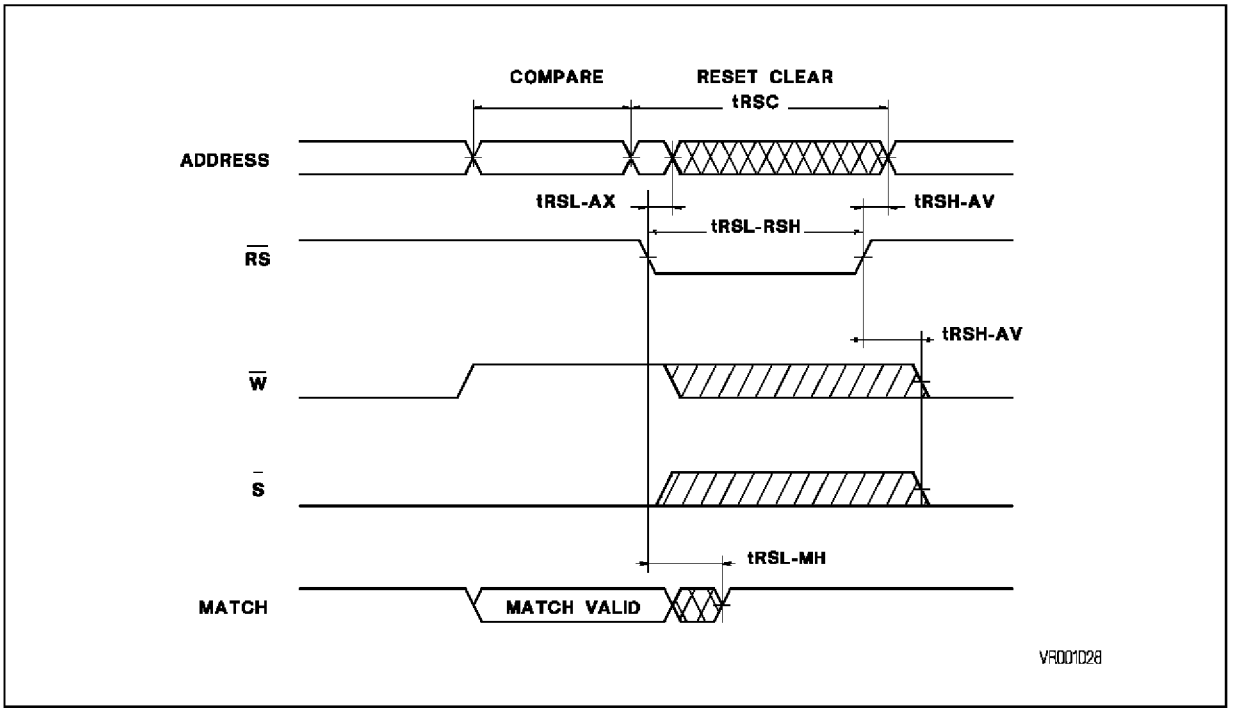
Figure 6. Match Compare Timing



APPLICATION

The MK48S74 operates from a 5V supply. It is compatible with all standard TTL families on all inputs and outputs. The device should share a solid ground plane with any other devices interfaces with it, particularly TTL devices. A pull-up resistor is also recommended for the $\overline{RS}$ input. This will ensure that any low going system noise, coupled onto the input does not drive $\overline{RS}$ below V_{IH} minimum specifications. This will enhance proper device operation, and avoid possible partial flash clear cycles. Additionally because the outputs can drive rail-to-rail into high impedance loads, the MK48S74 can also interface to 5V CMOS on all inputs and outputs. The MK48S74 provides the system designer with 64K fast static memory, a MATCH output, and a BYTEWIDE™ on-board comparator — all in one chip. The MK48S74 compares contents of addressed RAM locations to the current data inputs. A High-Z output on the MATCH Pin indicates that the input data and the RAM data match. Conversely, a logic zero "0" on the MATCH pin indicates at least one bit of difference between the RAM contents and the input TAG, generating in a miss. The MATCH output is constructed with an open drain arrangement. The open drain provides easy wired-OR implementation when generating a composite MATCH signal. In a cache subsystem, the MATCH signal provides the processor or CPU with the necessary information concerning wait state conditions. The purpose of a cache subsystem is to maintain a duplicate copy of portions of the main memory. When a valid match occurs, the system processor uses data from the fast cache memory, and avoids longer cycles to the main memory. Therefore, implementing cache subsystems with the MK48S74, and providing good hit or match ratio designs will enhance overall system performance. Because high frequency current transients will be associated with the operation of the MK48S74, power line inductance must be minimized on the circuit board power distribution network. Power and ground trace gridding or seprarate power planes can be employed to reduce line inductance. Though often times not thought of as such, the traces of a memory board are basically unterminated, low impedance trasmission lines. As such they are subject to signal reflections manifested as noise, undershoots and excessive ringing. Series termination in close proximity to the TTL drivers can improve driver/signal path impedance matching. While experimentaiton most often proves to be the only practical approach to selection of series resistors, values in the range of 10 to 33 ohms often prove most suitable.

Figure 7. Reset Timing



Note: $\overline{G}$ = High

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to Ground	– 0.3 to 6	V
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	– 65 to +150	°C
P_D	Power Dissipation	1	W
I_{OUT}	Output Current	50	mA

Note: This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_A \le +70°C$)

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{CC}	Supply Voltage	4.75	5.25	V	4
GND	Ground	0	0	V	4
V_{IH}	Logic 1 All Inputs	2.2	V_{CC} + 0.3	V	4
V_{IL}	Logic 0 All Inputs	– 0.3	0.8	V	4

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le +70°C$, $V_{CC} = 5V \pm 5\%$)

Symbol	Parameter	Min.	Max.	Unit	Notes
I_{CC1}	Average V_{CC} Power Supply Current		160	mA	5
I_{IL}	Input Leakage Current	– 1	1	µA	6
I_{OL}	Output Leakage Current	– 5	5	µA	7
V_{OH}	Logic 1 Output Voltage (I_{OUT} = –4 mA)	2.4		V	4
V_{OL}	Logic 0 Output Voltage (I_{OUT} = 8 mA)		0.4	V	4
V_{OL}	Match Output LOgic 0 Voltage (I_{OUT} = 18 mA)		0.4	V	4

Notes :

1. Measured with load shown in Figure 8A.
2. Measured with load in Figure 8B.
3. Measured with load in Figure 8C.
4. All Voltages referenced to GND.
5. I_{CC1} is measured as the average AC current with $V_{CC} = V_{CC}$ (max) and with the outputs open circuits. $t_{AVAV} = t_{AVAV}$ (min) duty cycle 100%.
6. Input leakage current specifications are valid for all V_{IN} such that $0V < V_{IN} < V_{CC}$. Measured at $V_{CC} = V_{CC}$ (max).
7. Output leakage current specifications are valid for all V_{OUT} such that $0V < V_{OUT} < V_{CC}$, S = V_{IH} and V_{CC} in valid operating range.
8. Sampled, not 100% tested, outputs deselected.

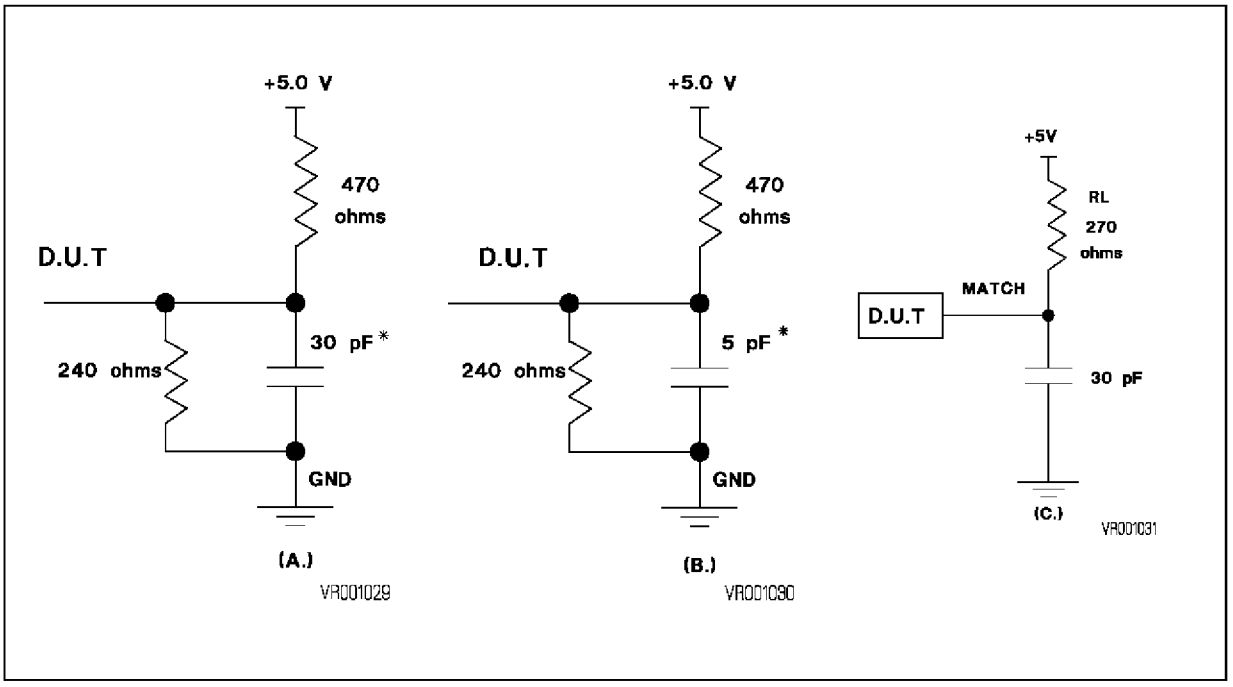
CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Notes
C_{IN}	Capacitance on all Input pins	4	pF	8
C_{OUT}	Capacitance on Q Output pins	10	pF	8

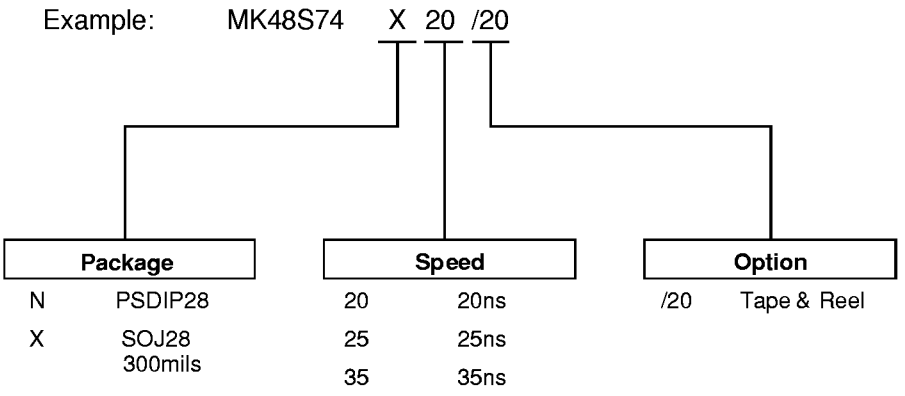
AC TEST CONDITIONS

Parameter	Value	Unit
Input Levels	0 to 3	V
Transition Time	1.5	ns
Input and Output Signal Timing Reference Level	1.5	V
Ambient Temperature	0 to 70	°C
Supply Voltage	5 ± 5%	V

Figure 8. Equivalent Output Load Circuits



ORDERING INFORMATION SCHEME



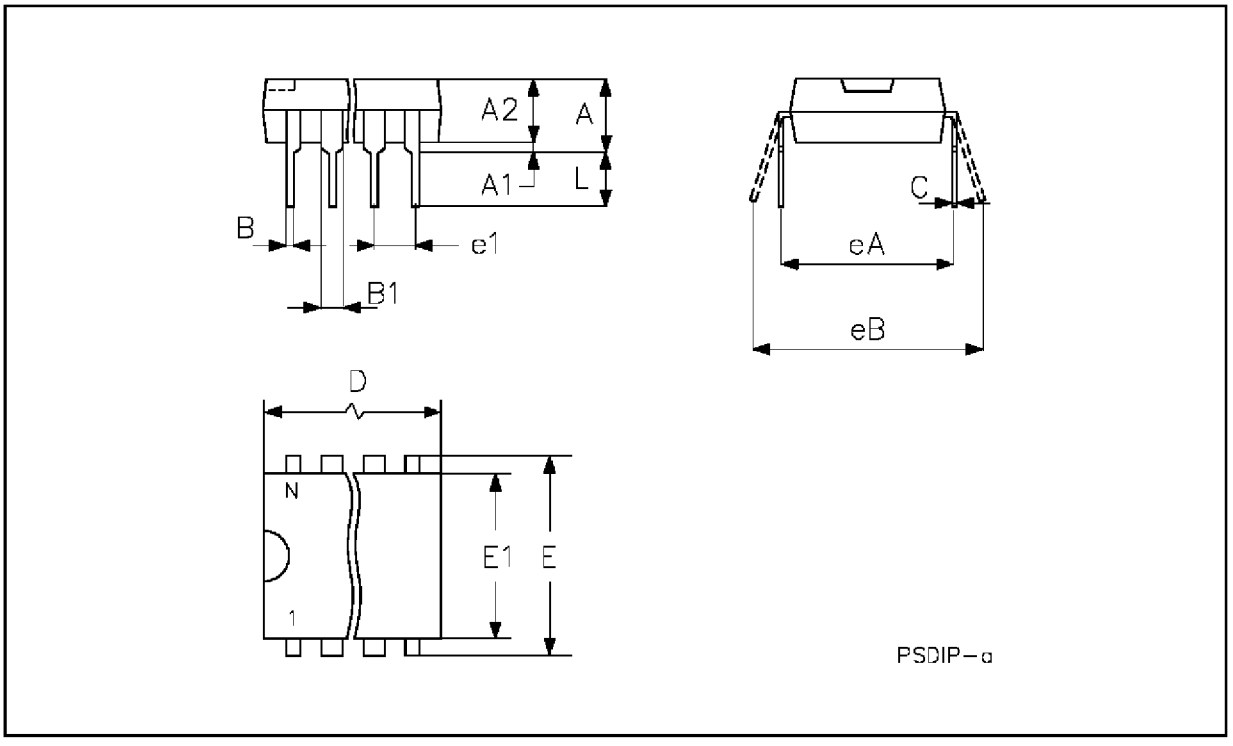
For a list of available options of Package and Speed, refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

PSDIP28 - 28 pin Plastic Skinny DIP, 300 mils width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			4.57			0.180
A1		0.38	–		0.015	–
A2		3.05	3.56		0.120	0.140
B		0.38	0.53		0.015	0.021
B1		1.14	1.27		0.045	0.050
C		0.20	0.30		0.008	0.012
D		34.54	34.80		1.360	1.370
E		7.62	8.26		0.300	0.325
E1		7.11	7.49		0.280	0.295
e1	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L		3.18	3.43		0.125	0.135
N	28			28		

PSDIP28

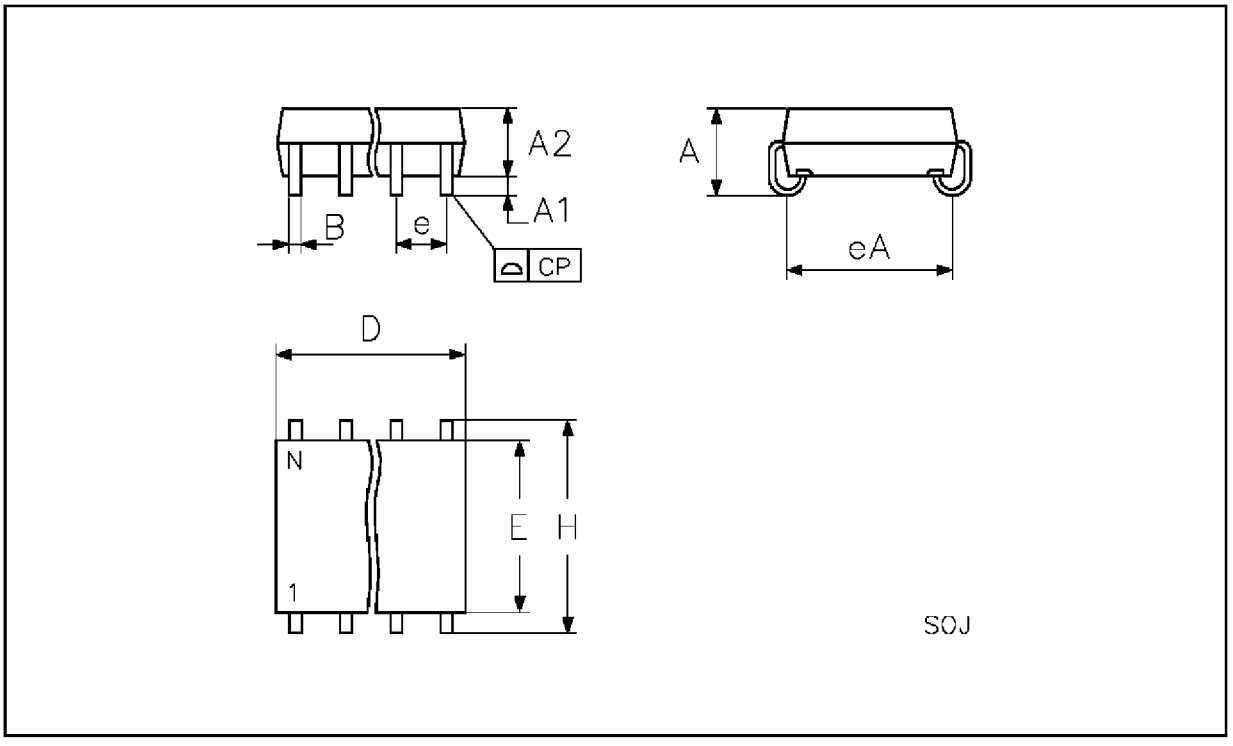


Drawing is out of scale

SOJ28 - 28 lead Plastic Small Outline J-lead, 300 mils

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.05	3.56		0.120	0.140
A1		0.71	0.91		0.028	0.036
A2		2.29	2.39		0.090	0.094
B		0.36	0.48		0.014	0.019
D		17.81	18.06		0.701	0.711
E		7.42	7.59		0.292	0.299
e	1.27	–	–	0.050	–	–
eA		6.65	6.91		0.262	0.272
H		8.51	8.81		0.335	0.347
N	28			28		
CP			0.10			0.004

SOJ28



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