October 1989
Edition 2.0

FUJITSU

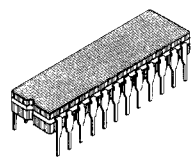
DATA SHEET

MB7238RA-20/-25/-25W, MB7238RS-20/-25/-25W
SCHOTTKY 16K-BIT REGISTERED PROM

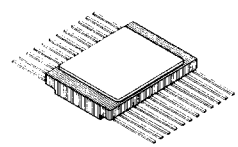
SCHOTTKY 16,384-BIT REGISTERED OUTPUT PROM

The Fujitsu MB7238 is a 16 Kbit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to a field programmable value, either synchronously (MB7238RS) or asynchronously (MB7238RA). Three-state outputs can also be enabled either synchronously or asynchronously, in either model. DEAP (diffused eutectic aluminum process) memory cells are used to provide fast and reliable programming.

- 2048 word x 8 bit PROM data organization
- Fast clock access time:
  - 20 ns (MB7238RA/RS-20)
  - 25 ns (MB7238RA/RS-25)
- Output register can be preset to a field-programmable value.
- Register can be initialized synchronously (MB7238RS) or asynchronously (MB7238RA).
- Single +5 V operation
- TTL compatible I/O
- Low current inputs
- Three-state outputs
- Outputs can be enabled either synchronously or asynchronously.
- Outputs are kept disabled on power-up.
- DEAP memory cells are reliable and easily programmed.
- Test cells allow extensive testing of AC, DC and programming characteristics before shipment.



CERAMIC PACKAGE
DIP-24C-C04



CERAMIC PACKAGE
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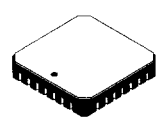

CERAMIC PACKAGE
LCC-28C-A01

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−1.5 to +5.5	V
Input Current	I_{IN}	−20	mA
Output Current	I_{OUT}	+100	mA
Power Supply Voltage (during programming)	V_{CCP}	−0.5 to +7.5	V
Input Voltage (during programming)	V_{IPRG}	+22.5	V
Input Current (during programming)	I_{IPRG}	+270	mA
Output Voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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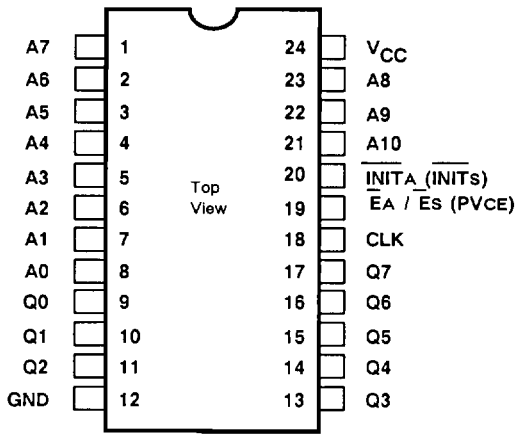
PIN ASSIGNMENT



Symbols in blankets: MB7238RS

PAD CONFIGURATION

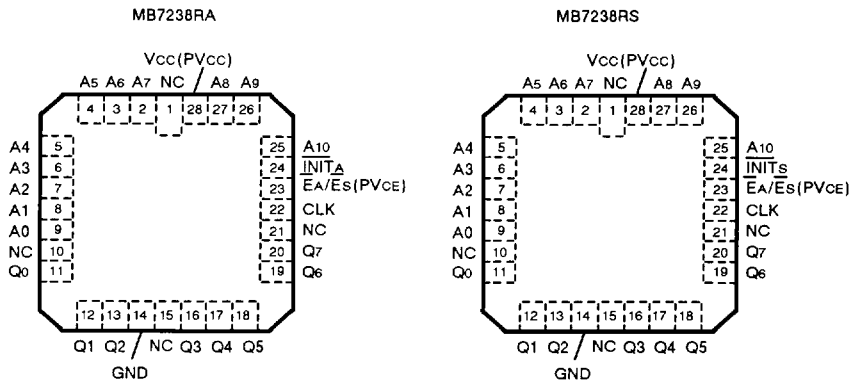


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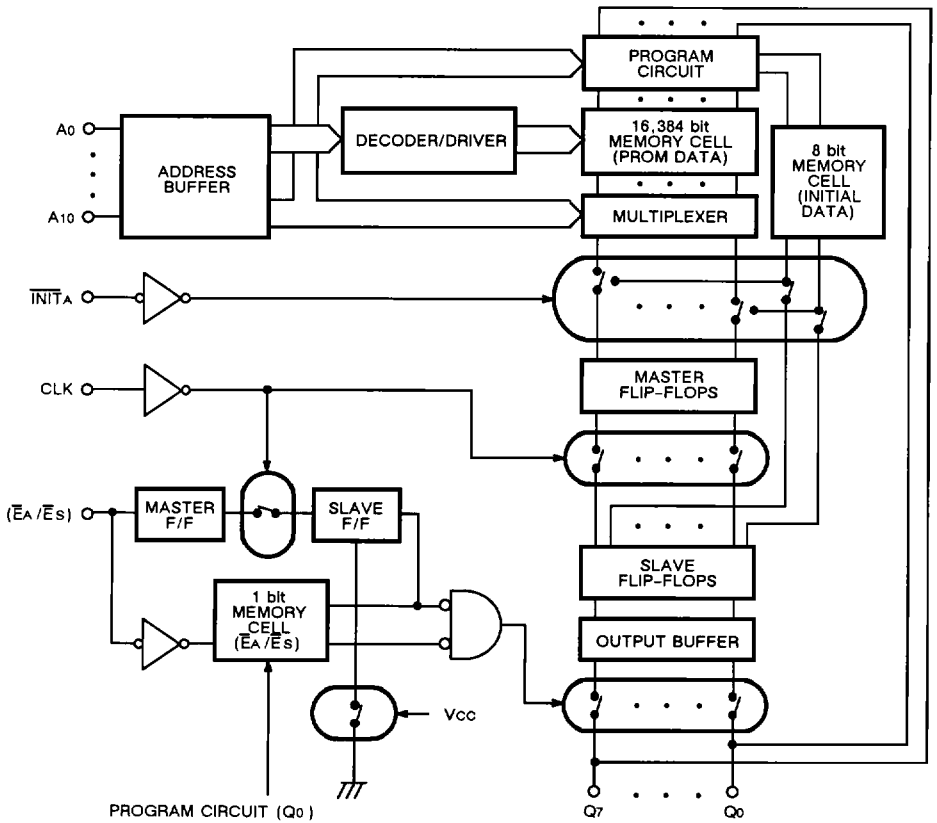
Fig. 1 — MB7238RA BLOCK DIAGRAM



Input				Output	Operating Mode	Remarks
$\overline{INIT}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	X	L	—	Initial Data	Initialize	E_A Mode
H	↑	L	—	PROM Data	Load Register	
X	X	H	—	Z	Chip Disable	
L	X	—	L	Initial Data	Initialize	E_S Mode
H	↑	—	L	PROM Data	Load Register	
X	↑	—	H	Z	Chip Disable	

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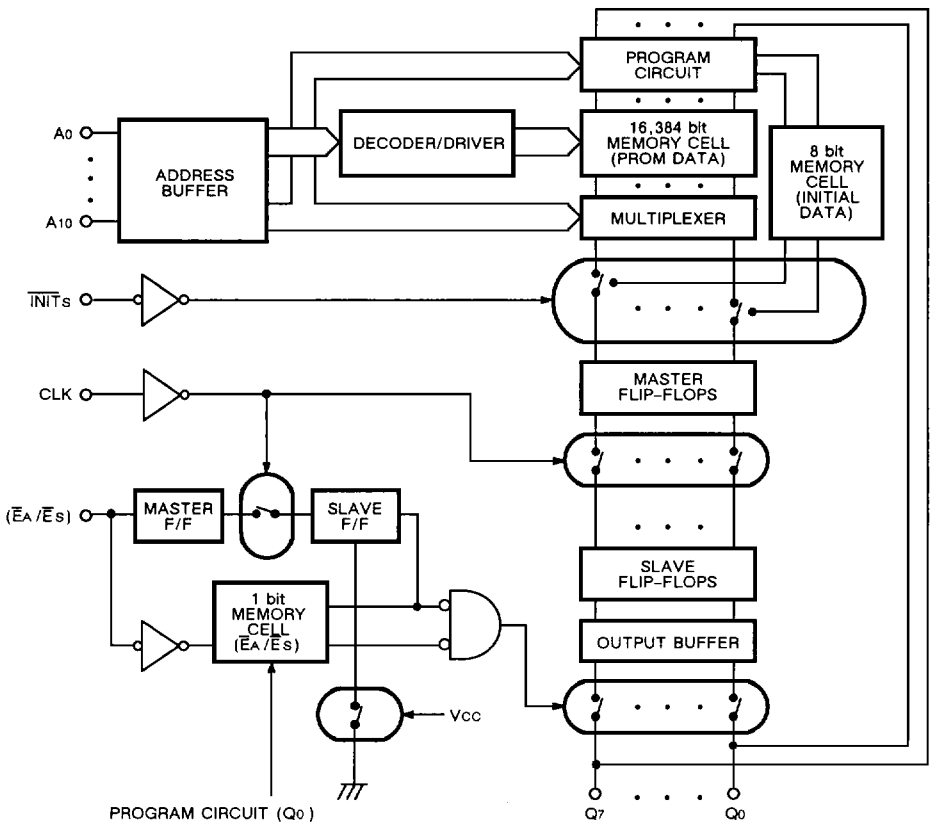
Fig. 2 — MB7238RS BLOCK DIAGRAM



Input				Output	Operating Mode	Remarks
INITs	CLK	EA	Es			
L	↑	L	—	Initial Data	Initialize	EA Mode
H	↑	L	—	PROM Data	Load Register	
X	X	H	—	Z	Chip Disable	
L	↑	—	L	Initial Data	Initialize	Es Mode
H	↑	—	L	PROM Data	Load Register	
X	↑	—	H	Z	Chip Disable	

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READ OPERATIONS

OVERVIEW (SEE FIGURES 1 AND 2)

During PROM reads, data is shifted through a register latch, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_{10}), new data appears in the master register. At the next clock pulse this data is transferred to the slave register. The MB7238 only has one chip enable pin $\overline{E}_A/\overline{E}_S$. $\overline{E}_A/\overline{E}_S$ pin is normally $\overline{E}_A$ mode, but you can change $\overline{E}_A$ mode to $\overline{E}_S$ mode (see page 11).

The chip enable input must be low in order for the data in the slave register to appear at the outputs (Q_0 through Q_7). Bringing the asynchronous chip enable ($\overline{E}_A$) low immediately enables the outputs. And bringing the synchronous chip enable ($\overline{E}_S$) low enables the outputs at the next clock pulse. Likewise, when the outputs are enabled, bringing either of the inputs high will cause them to be disabled, e.g., put into a high-impedance state. When $\overline{E}_A$ is brought high, the outputs are immediately disabled, whereas when $\overline{E}_S$ is brought high, they are disabled after the next clock pulse.

If the $\overline{INIT}$ input is brought low the register latch is loaded with a field-programmable initial value, rather than with PROM data. In the MB7238RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB7238RA both the master and slave registers are loaded immediately.

TIMING CONSIDERATIONS

Data Read (see Figure 3)

After an address change, address setup time t_S (A) must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time t_H (A), to shift the data to the slave register. The data will appear at the outputs within clock access time t_A (CLK) after the rising edge of the clock, if the outputs had been previously enabled.

If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time t_{EN} ($\overline{E}_A$) must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time t_{EN} (CLK) must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

In the MB7238RA, when the registers have been initialized by $\overline{INIT}$, and $\overline{INIT}$ is then brought high to select PROM data, asynchronous initialize recovery time t_R ($\overline{INIT}_A$) must elapse after the clock signal is applied.

Initial Data Read (see Figures 4 and 5)

In the MB7238RA, after the $\overline{INIT}$ input is brought low, asynchronous initialize access time t_A ($\overline{INIT}_A$) must elapse before the initial data appears at the outputs.

In the MB7238RS, after the $\overline{INIT}$ input is brought low, synchronous initialize setup time t_S ($\overline{INIT}_S$) must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

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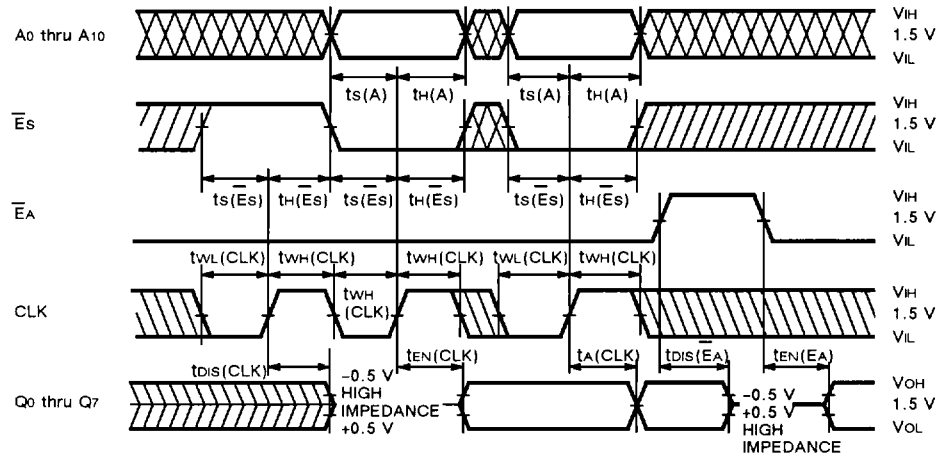
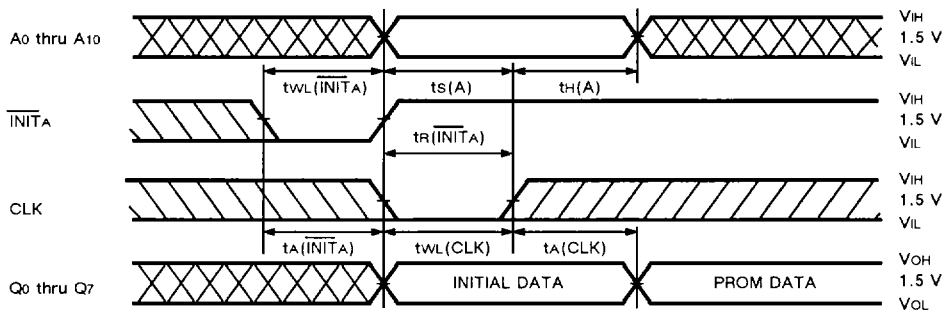
Fig. 3 — PROM DATA READ TIMING *1



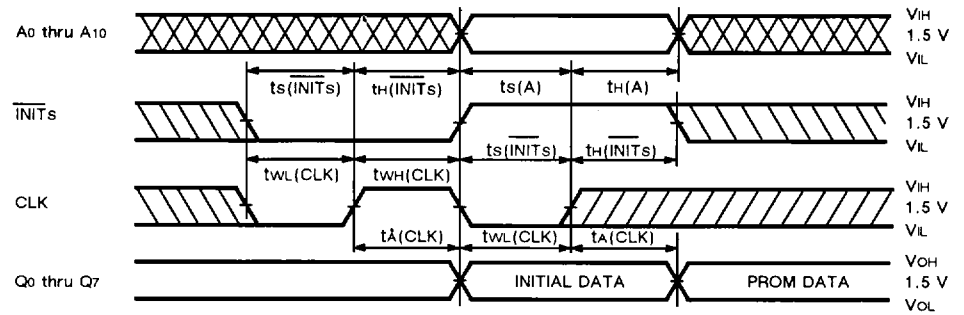
Note:
*1. INIT is high.

Fig. 4 — ASYNCHRONOUS INITIAL DATA READ TIMING (MB7238RA) *1



Notes:
*1. EA/ES input is low.
*2. ⊠ Don't care.

Fig. 5 — SYNCHRONOUS INITIAL DATA READ TIMING (MB7238RS)*1



Notes:
*1. $\overline{E_A}/\overline{E_S}$ input are low.
*2. ⊠ Don't care.

DATA READ SPECIFICATIONS

Table 1—Guaranteed Operating Conditions

Parameter	Symbol	MB7238RA-20/-25 MB7238RS-20/-25			MB7238RA-25W MB7238RS-25W			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	0	—	0.8	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5	2.0	—	5.5	V
Ambient Temperature	T_A	0	—	75	-55	—	+125	°C

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AC CHARACTERISTICS

Parameter	Symbol	Typical	MB7238RA-20 MB7238RS-20		MB7238RA-25 MB7238RS-25		MB7238RA-25W MB7238RS-25W		Unit	Remarks
			Min	Max	Min	Max	Min	Max		
Address Setup Time	t_S (A)	28	40	—	45	—	45	—	ns	—
Address Hold Time	t_H (A)	-8	0	—	0	—	0	—	ns	—
Clock Access Time	t_A (CLK)	15	—	20	—	25	—	25	ns	—
Clock Pulse Width	t_{WH} (CLK) t_{WL} (CLK)	10	20	—	20	—	20	—	ns	
Synchronous Enable Setup Time	t_S ($\overline{E_S}$)	5	10	—	15	—	15	—	ns	—
Synchronous Enable Hold Time	t_H ($\overline{E_S}$)	0	5	—	5	—	5	—	ns	—
Asynchronous Initialize Access Time	t_A ($\overline{INIT_A}$)	20	—	30	—	35	—	35	ns	MB7238RA
Asynchronous Initialize Recovery Time	t_R ($\overline{INIT_A}$)	11	20	—	25	—	25	—	ns	MB7238RA
Asynchronous Initialize Pulse Width	t_{WL} ($\overline{INIT_A}$)	13	20	—	20	—	20	—	ns	MB7238RA
Synchronous Initialize Setup Time	t_S ($\overline{INIT_S}$)	15	25	—	30	—	30	—	ns	MB7238RS
Synchronous Initialize Hold Time	t_H ($\overline{INIT_S}$)	-10	0	—	0	—	0	—	ns	MB7238RS
Clock Enable Time	t_{EN} (CLK)	18	—	25	—	30	—	30	ns	—
Asynchronous Enable Time	t_{EN} ($\overline{E_A}$)	15	—	25	—	30	—	30	ns	—
Clock Disable Time*2	t_{DIS} (CLK)	18	—	25	—	30	—	30	ns	—
Asynchronous Disable Time *2	t_{DIS} ($\overline{E_A}$)	11	—	25	—	30	—	30	ns	—

Notes:
*1. At T_A = 25°C and V_{CC} = 5.0 V.
*2. Measured at a point on the output waveform 0.5 V from the active output level.

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DC CHARACTERISTICS (Under Guaranteed Operating Conditions)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Current	I_{IH}	V_{IH} = 5.5V	—	—	40	μA
	I_{IL}	V_{IL} = 0.45 V	—	—	-250	μA
Input Clamp Voltage	V_{IC}	I_I = -18 mA	—	—	-1.2	V
Output Low Voltage	V_{OL}	I_{OL} = 10 mA *3	—	—	0.45	V
		I_{OL} = 16 mA	—	—	0.5	V
Output Leakage Current (Chip Disabled)	I_{OIL}	V_O = 0.45 V	—	—	-40	μA
	I_{OIH}	V_O = 2.4 V	—	—	40	μA
Output High Voltage *1	V_{OH}	I_{OH} = -2.4 mA	2.4	—	—	V
Output Short-Circuit Current *1	I_{OS}	V_O = 0 V	-15	—	-60	mA
Power Supply Current	I_{CC}	V_I = Open or 0 V	—	140 *2	185	mA

Notes:

*1. Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

*2. T_A = 25°C and V_{CC} = 5.0 V.

*3. This is not applied for W-version.

TERMINAL CAPACITANCE

(T_A = 25°C, V_{CC} = +5.0 V, V_{IN} = +2.0 V, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Terminal Capacitance	C_{IN}	—	10	pF
Output Terminal Capacitance	C_{OUT}	—	15	pF

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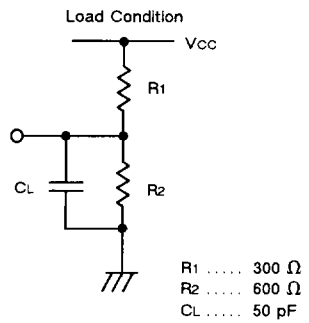
Fig. 6 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0 V to 3 V
Rise and Fall Time ..... 5 ns from 1 V to 2 V
Frequency ..... 1 MHz



FABRICATION TECHNOLOGY

INPUT/OUTPUT CIRCUITS

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low, and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to a bus-oriented system. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

MEMORY CELLS

The memory cells in the MB7238 are of the junction-shorting type, using DEAP technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, thus permanently changing the cell's state to 1 (high).

By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Poly-silicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

PROGRAMMING

OVERVIEW (See Figure 7)

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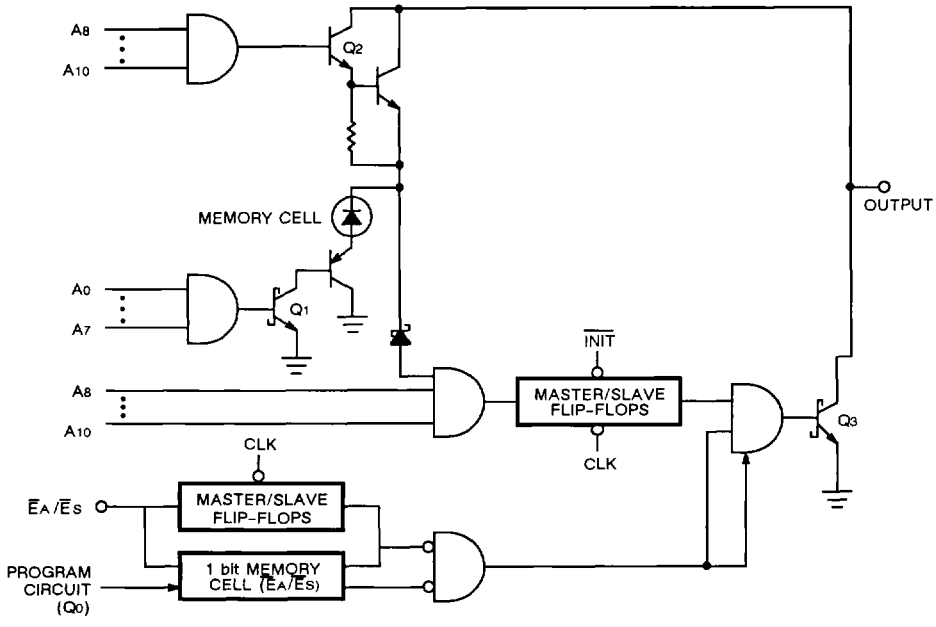
As shipped, all the bits in the MB7238 are in the 0 (low) state. In programming, individual cells are addressed and a programming current applied, to change that bit's state to 1. Only one bit at a time can be programmed, because the internal decoding circuitry can only sink one unit of programming current at a time.

The word containing the desired bit is first selected, using the normal address inputs. The decoded address lines turn on transistors Q_1 and Q_2. When the PV_{CE} level is applied to the $\overline{E}_A/\overline{E}_S$ input, the chip outputs are disabled, turning off transistor Q_3. Programming pulses are applied to the output of the desired bit, eventually fusing the diode attached to Q_1. At this point, if the output is read, it will be in the 1 (high) state. Two additional programming pulses are then applied, to ensure reliability.

Initial data is programmed in the same way, except that the address inputs are kept low, and $\overline{INIT}$ is applied to an $\overline{INIT}$ pulse, to select the initial data word rather than a PROM data word.

Fig. 7 — PROGRAMMABLE MEMORY CELL



PROCEDURE

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E}_A/\overline{E}_S$ low. Set $\overline{INIT}$ input high to select PROM data for programming, or set initialize inputs and address inputs low to select initial data.
3) Select the desired bit.
4) Apply a clock pulse.
5) Read the output to confirm that the desired bit is in fact 0. If not, go on to the next bit.
6) Raise the V_{CC} terminal to PV_{CC} (7 V).
7) Raise the $\overline{E}_A/\overline{E}_S$ terminal to PV_{CE} (20 V).
8) Apply a clock pulse.
9) Apply a programming pulse (125 mA, 11 µS) to the output (Qx) of the desired bit.
10) Return PV_{CC} to a 5 V and PV_{CE} to 0 V. And in case of initial data, apply an $\overline{INIT}$ pulse.
11) Apply a clock pulse.
12) After a delay of t_{PR} (5 µs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (6) through (12), allowing t_{CYC} (50 µs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.
13) If there are more bits to be programmed, repeat steps (3) through (12).

LIABILITY

Fujitsu performs an extensive series of tests to ensure device performance before shipping. However, 100% programmability is not guaranteed. Furthermore, it is imperative that the programming specifications be rigorously adhered to in order to achieve a satisfactory programming yield.

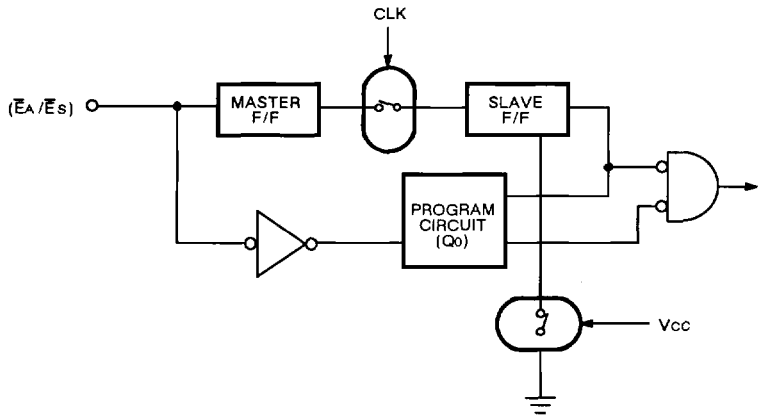
Fujitsu will not accept responsibility for any device found defective if it was not programmed according to these specifications. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of suspected defective memory cells.

8

CHANGING $\overline{E}_A$ INPUT TO $\overline{E}_S$ INPUT

The MB7238 has only one chip enable pin, $\overline{E}_A$. However, this can be changed to an $\overline{E}_S$ input, by programming a special memory cell. The programming method is similar to that described above for PROM and initial data, the only differences being that address line A_0 is raised to 20 V, and programming pulses are applied only to output Q_0. Also, when reading the output voltage to confirm programming, the state of the special memory cell is reflected in the outputs, Q_0.

Fig. 8 — ENABLE INPUT PROGRAMMING CIRCUIT



PROCEDURE

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E}_A$ low. Raise A_0 to PV_{A0} (20 V), and set all the other address lines low. Set the $\overline{INIT}$ input low.
3) Apply a clock pulse.
4) Read the Q_0 output to confirm that it is in fact 0. If not, no programming is necessary.
5) Raise the V_{CC} terminal to PV_{CC} (7 V).
6) Raise the $\overline{E}_A$ terminal to PV_{CE} (20 V).
7) Apply a clock pulse.
8) Apply a programming pulse (125 mA, 11 µs) to output terminal Q_0.
9) Return PV_{CC} to 5 V and PV_{CE} to 0 V.
10) Apply a clock pulse.
11) After a delay of t_{PR} (5 µs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (5) through (11), allowing t_{CYC} (50 µs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.

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Fig. 9a – PROGRAMMING TIMING CHART

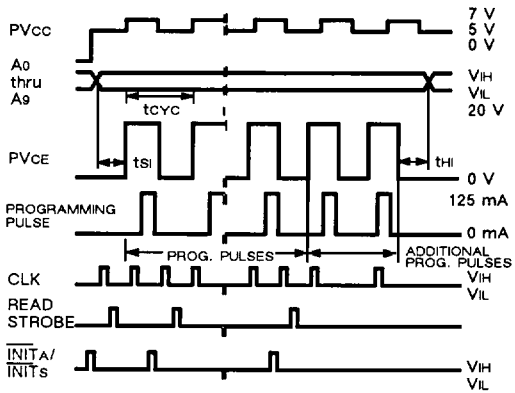
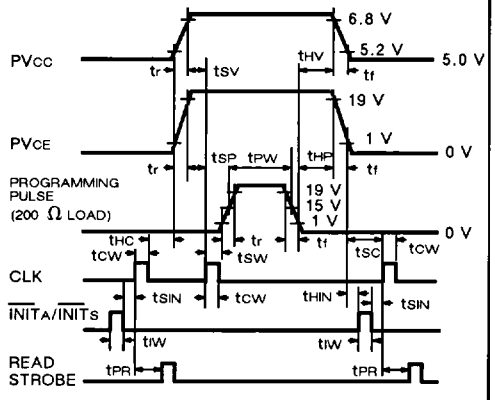


Fig. 9b – ONE DETAILED PROGRAMMING CYCLE



PROGRAMMING SPECIFICATIONS, DC

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power-supply Voltage	V_{CC}	4.75	5.0	5.25	V
Power-supply Current	I_{CC}	—	—	200	mA
PV_{CC} Power-supply Voltage	PV_{CC}	6.7	7.0	7.3	V
PV_{CC} Power-supply Current	PI_{CC}	—	—	300	mA
Programming Pulse Current	I_{PRG}	120	—	130	mA
Programming Pulse Clamp Voltage	V_{PRG}	20	20	22	V
PV_{CE} Pulse Voltage	PV_{CE}	20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}	230	—	260	mA
PV_{AO} Pulse Voltage	PV_{AO}	10	—	22	V
PV_{AO} Pulse Clamp Current	PI_{AO}	10	—	—	mA
Reference Level for Output High Voltage	V_{REF}	1.0	1.5	2.4	V

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PROGRAMMING SPECIFICATIONS, AC

Parameter	Symbol	Min	Max	Typ	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW}	10	11	12	µs
Clock Pulse Width	t_{CW}	0.5	—	—	µs
Programming Pulse Rise Time	t_r	—	—	2	µs
PVcc Pulse Rise Time	t_r	—	—	2	µs
PVCE Pulse Rise Time	t_r	—	—	2	µs
Programming Pulse Fall Time	t_f	—	—	2	µs
PVcc Pulse Fall Time	t_f	—	—	2	µs
PVCE Pulse Fall Time	t_f	—	—	2	µs
Input Setup Time	t_{SI}	2	—	—	µs
PVcc Pulse Setup Time	t_{SV}	2	—	—	µs
PVCE Pulse Setup Time	t_{SP}	2	—	—	µs
Programming Pulse Setup Time	t_{SW}	2	—	—	µs
Input Hold Time	t_{HI}	2	—	—	µs
PVcc Pulse Hold Time	t_{HV}	2	—	—	µs
PVCE Pulse Hold Time	t_{HP}	2	—	—	µs
Clock Pulse Setup Time	t_{SC}	5	—	—	µs
Clock Pulse Hold Time	t_{HC}	5	—	—	µs
Init Pulse Setup Time	t_{SIN}	0.5	—	—	µs
Init Pulse Hold Time	t_{HIN}	2	—	—	µs
Init Pulse Width	t_{IW}	0.5	—	—	µs
Clock Pulse Rising Edge to Read Strobe Time	t_{PR}	5	—	—	µs
Number of Programming Pulses	n	—	—	100	pulses
Programming Time/Bit	—	120	—	6120	µs/bit
Number of Additional Programming Pulses	—	2	—	2	pulses

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TYPICAL PERFORMANCE CHARACTERISTICS

DC CHARACTERISTICS

Fig. 10 – I_{IN} Input Current vs. V_{IN} Input Voltage

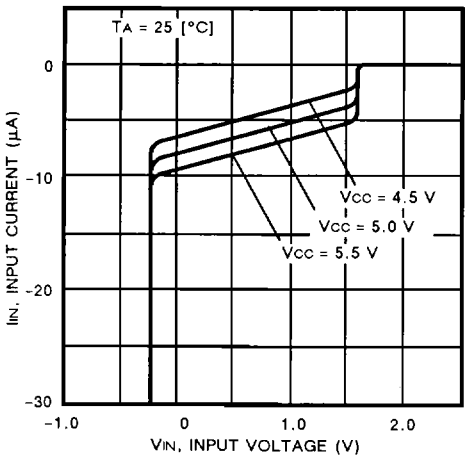


Fig. 11 – I_{OH} Output High Current vs. V_{OH} Output High Voltage

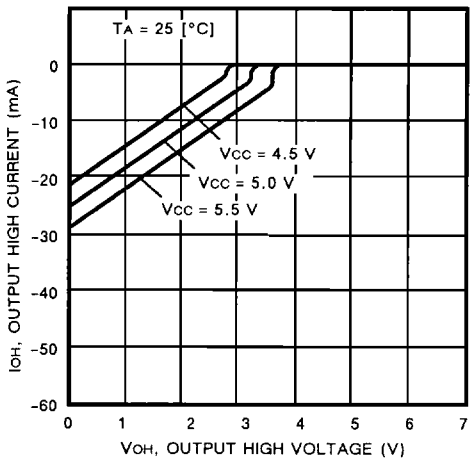
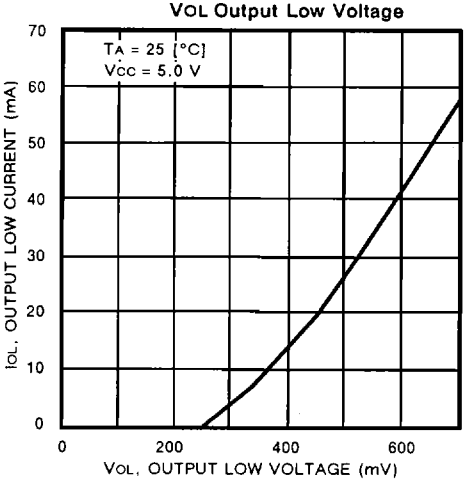


Fig. 12 – I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



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DC CHARACTERISTICS (Cont.)

Fig. 13 – tS (A) Address Setup Time vs. Ambient Temperature

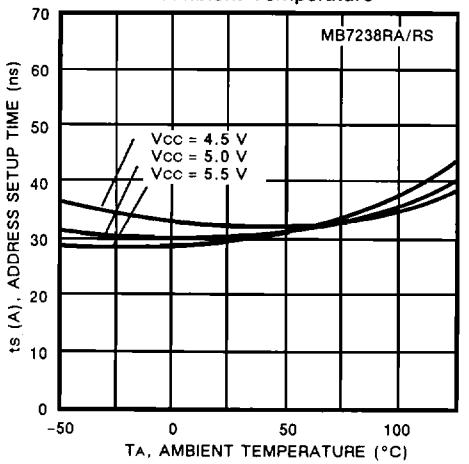


Fig. 14 – tH(A) Address Hold Time vs. Ambient Temperature

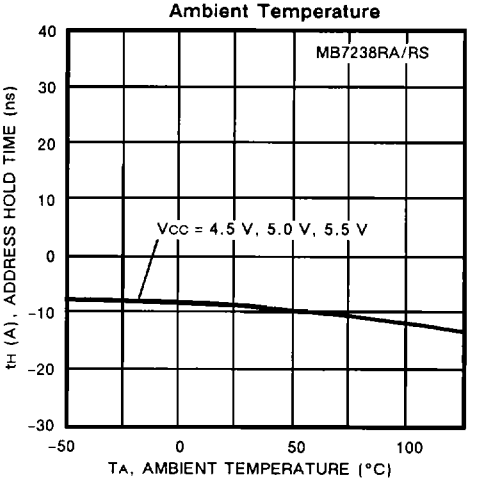


Fig. 15 – tA (CLK) Clock Access Time vs. Ambient Temperature

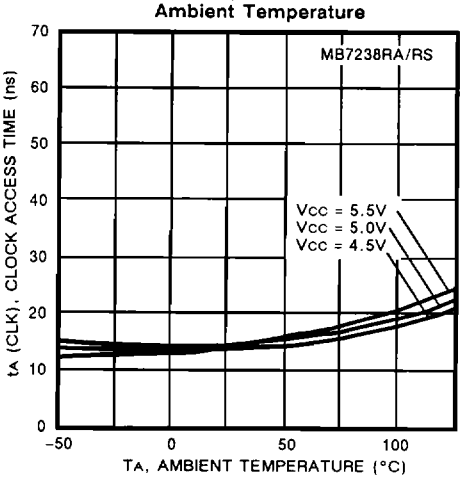
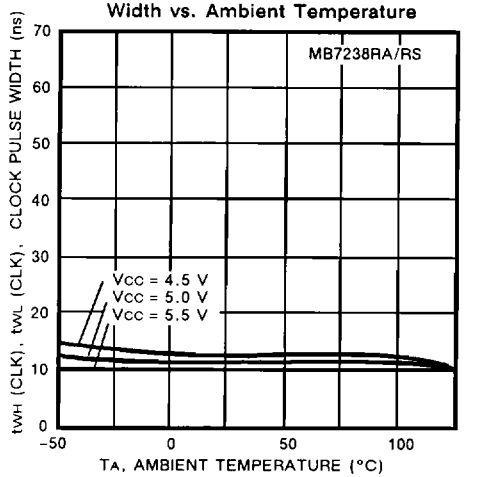


Fig. 16 – tWH (CLK) and tWL (CLK) Clock Pulse Width vs. Ambient Temperature



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DC CHARACTERISTICS (Cont.)

Fig. 17 – t_S ($\overline{E}_S$) Synchronous Enable SetupTime vs. Ambient Temperature

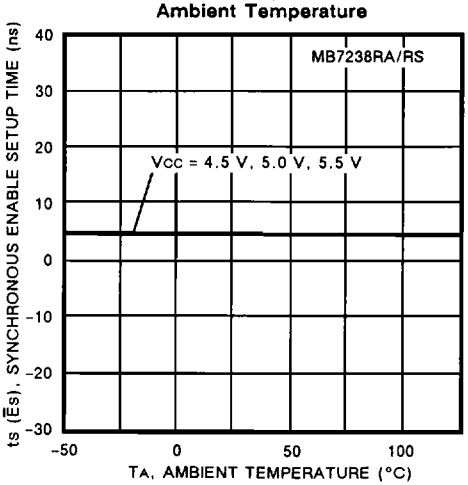


Fig. 18 – t_H ($\overline{E}_S$) Synchronous Enable Hold Time vs. Ambient Temperature

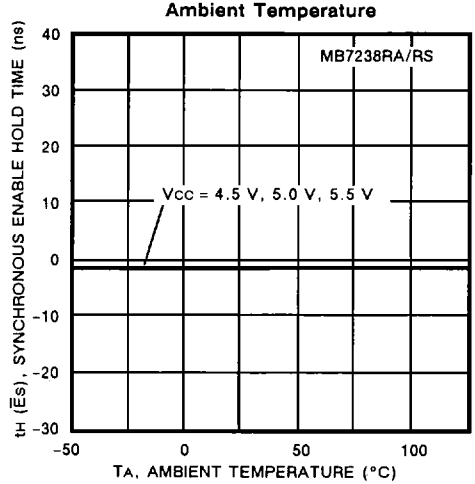


Fig. 19 – t_A ($\overline{INIT}_A$) Asynchronous Initialize Access Time vs. Ambient Temperature

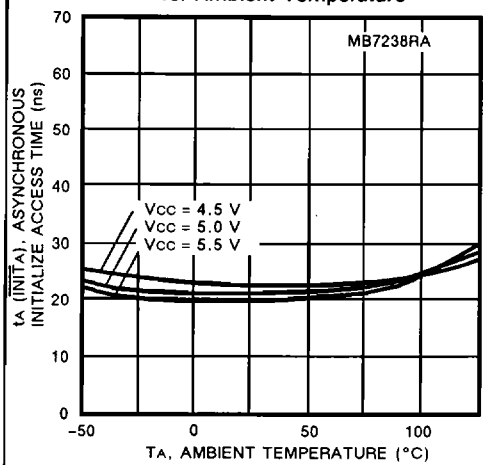
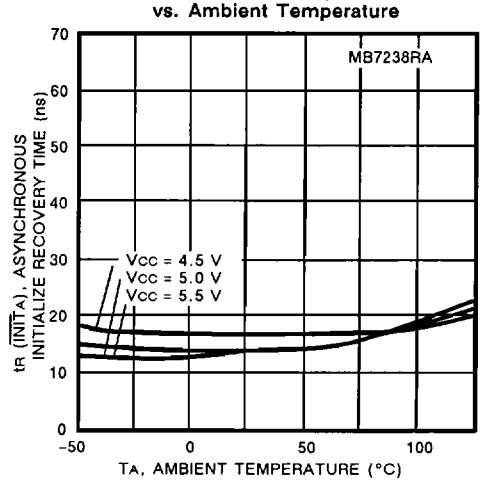


Fig. 20 – t_R ($\overline{INIT}_A$) Asynchronous Initialize Recovery Time vs. Ambient Temperature



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DC CHARACTERISTICS (Cont.)

Fig. 21 – t_{WL} ($\overline{INITA}$) Asynchronous Initialize Pulse Width vs. Ambient Temperature

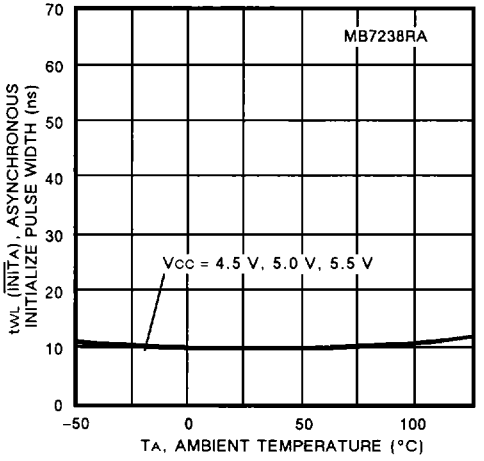


Fig. 22 – t_S ($\overline{INITs}$) Synchronous Initialize Setup Time vs. Ambient Temperature

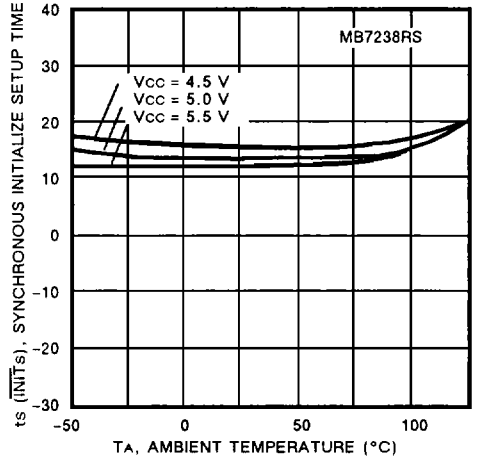


Fig. 23 – t_H ($\overline{INITs}$) Synchronous Initialize Hold Time vs. Ambient Temperature

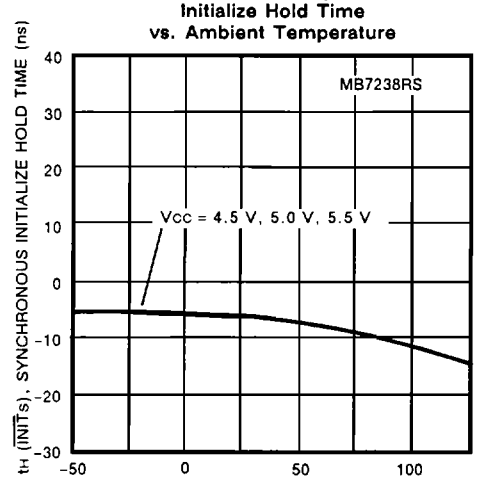
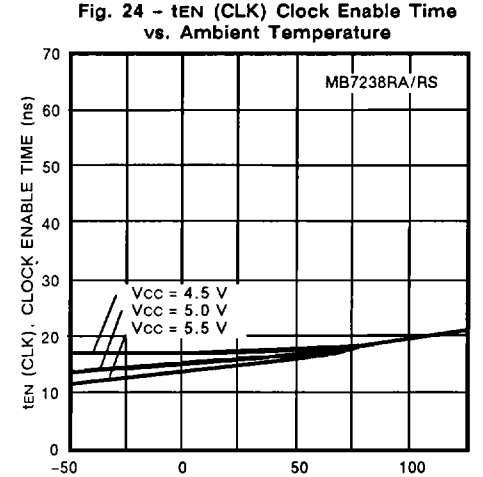


Fig. 24 – t_{EN} (CLK) Clock Enable Time vs. Ambient Temperature



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DC CHARACTERISTICS (Cont.)

Fig. 25 – t_{EN} ($\overline{E}_A$) Asynchronous Enable Time vs. Ambient Temperature

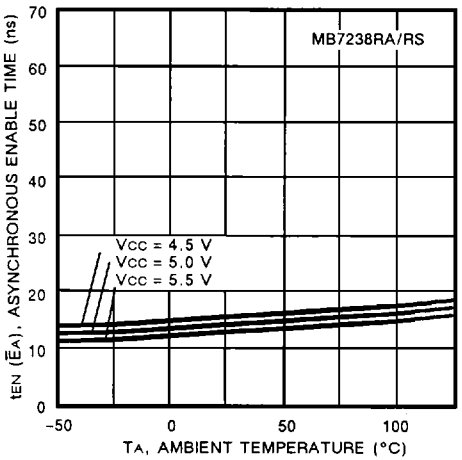


Fig. 26 – t_{DIS} (CLK) Clock Disable Time vs. Ambient Temperature

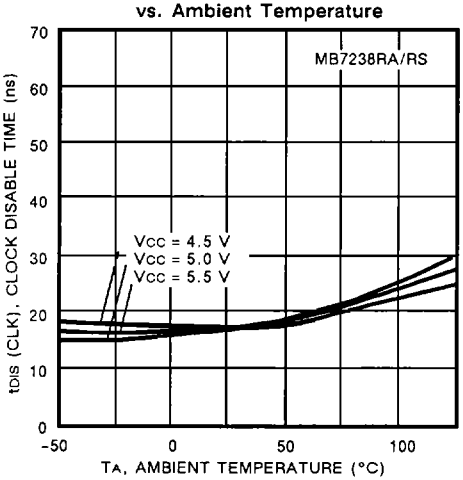


Fig. 27 – t_{DIS} ($\overline{E}_A$) Asynchronous Disable Time vs. Ambient Temperature

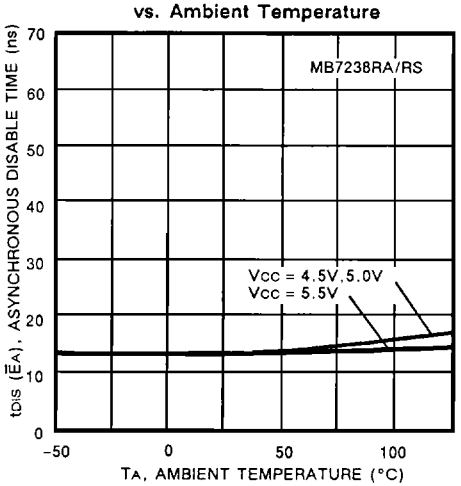
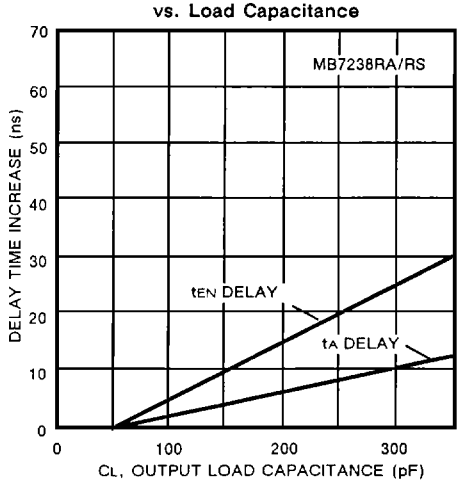


Fig. 28 – Delay Time Increase vs. Load Capacitance



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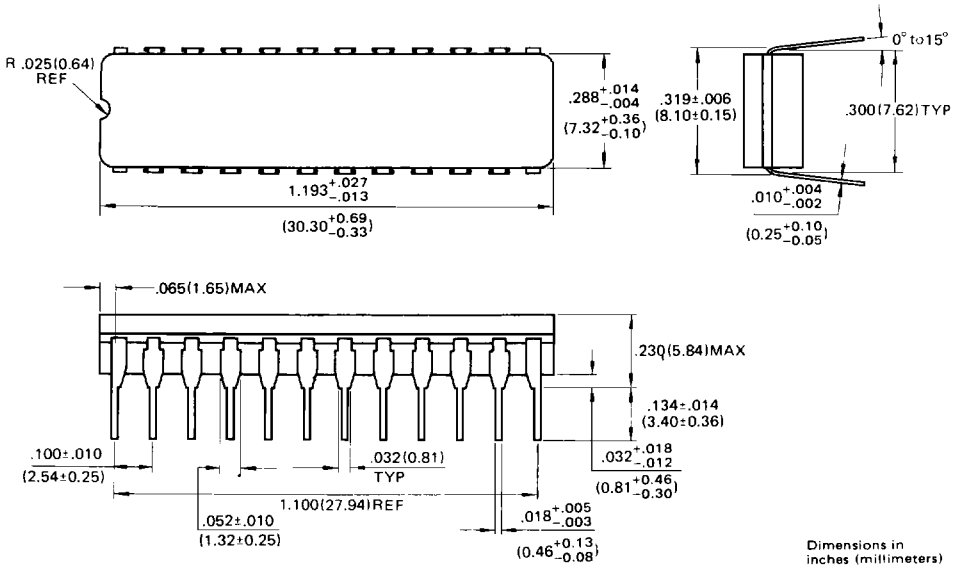
PACKAGE DIMENSIONS

Standard 24-pin Ceramic DIP (Suffix : -Z)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)



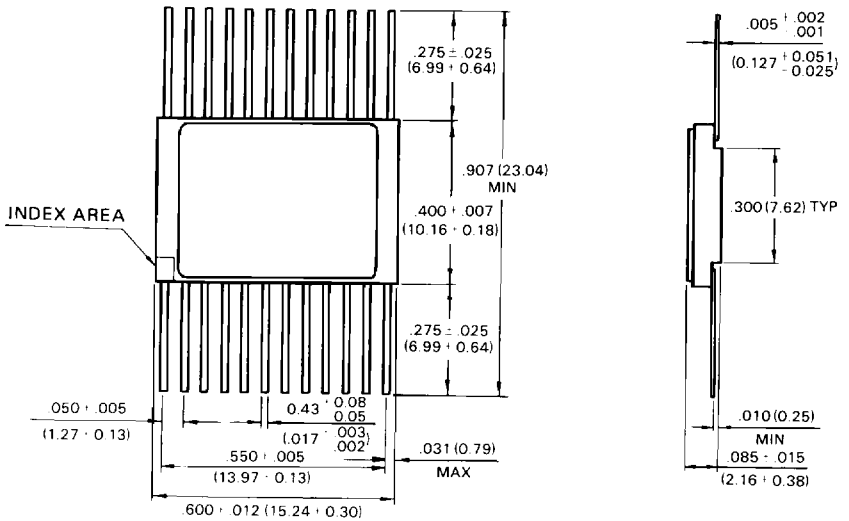
Dimensions in inches (millimeters)

8

PACKAGE DIMENSIONS (Continued)

Standard 24-pin Ceramic Flat Package (Suffix : -CF)

24-LEAD CERAMIC FLAT PACKAGE
(Case No. : FPT-24C-A02)



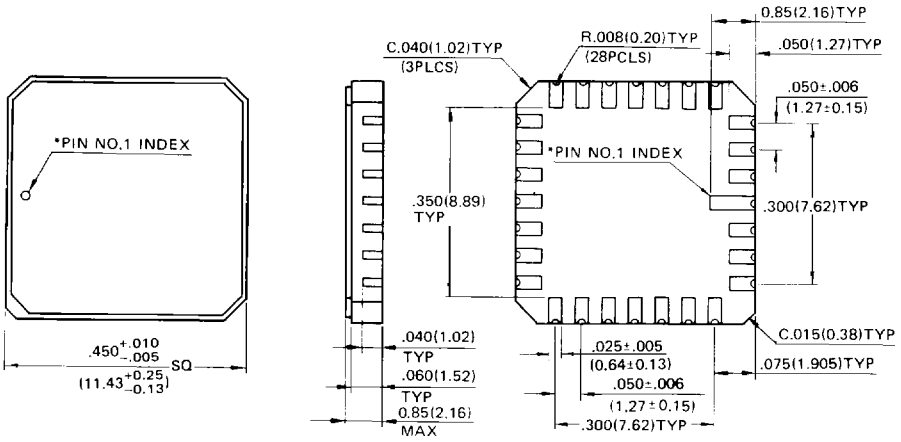
Dimensions in
inches (millimeters)

8

PACKAGE DIMENSIONS (Continued)

Standard 28-pad Ceramic LCC (Suffix : -CV)

28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

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