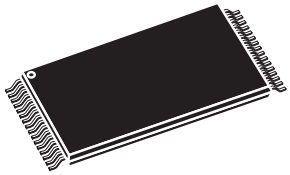
M68Z128W

3V, 1 Mbit (128 Kbit x 8) Low Power SRAM with Output Enable

FEATURES SUMMARY

- ULTRA LOW DATA RETENTION CURRENT
  - 10nA (typical)
  - 2.0µA (max)
- OPERATION VOLTAGE: 3.0V (+0.6 / –0.3V)
- 128 Kbit x 8 SRAM WITH OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIMES: 70ns
- LOW V_{CC} DATA RETENTION: 1.4V
- TRI-STATE COMMON I/O
- LOW ACTIVE and STANDBY POWER
- INTENDED FOR USE WITH ST ZEROPOWER® AND TIMEKEEPER® CONTROLLERS

Figure 1. Package



TSOP32 (N)
8 x 20mm

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DESCRIPTION

The M68Z128W is a 1 Mbit (1,048,576 bit) CMOS SRAM, organized as 131,072 words by 8 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 3V (+0.6 / –0.3V) supply, and all inputs and outputs are TTL compatible.

This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68Z128W is available in TSOP32 (8 x 20mm) package.

Figure 2. Logic Diagram

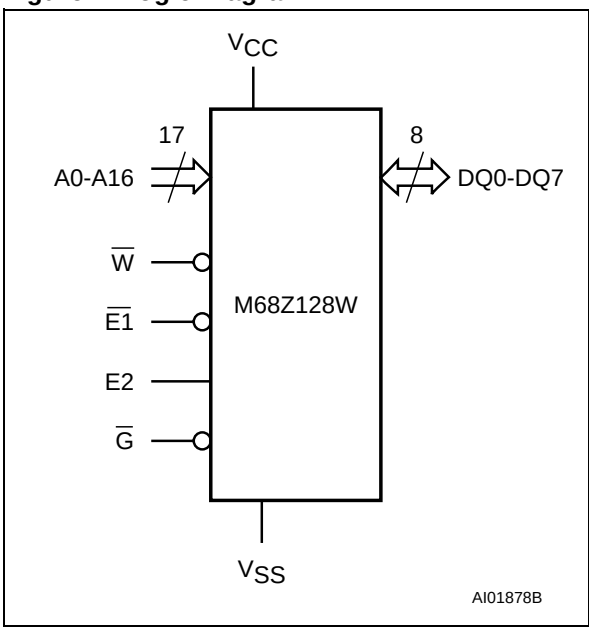


Table 1. Signal Names

A0-A16	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{E1}$	Chip Enable 1
E2	Chip Enable 2
$\overline{G}$	Output Enable
$\overline{W}$	WRITE Enable
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

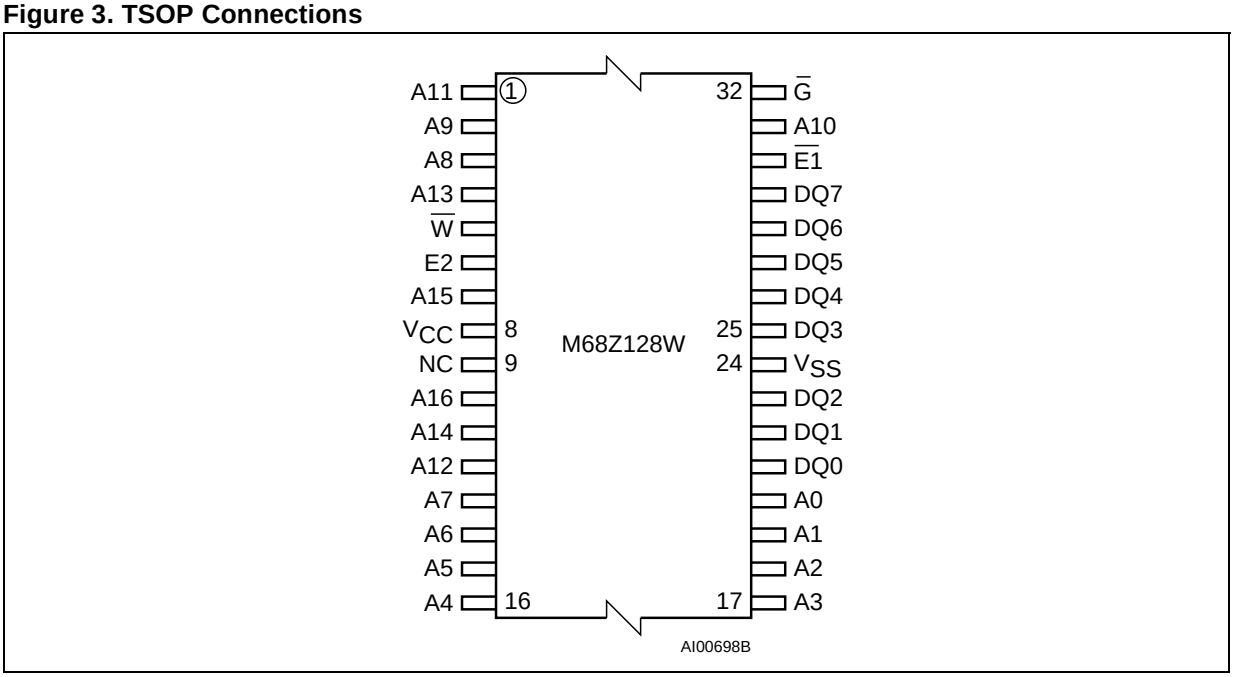
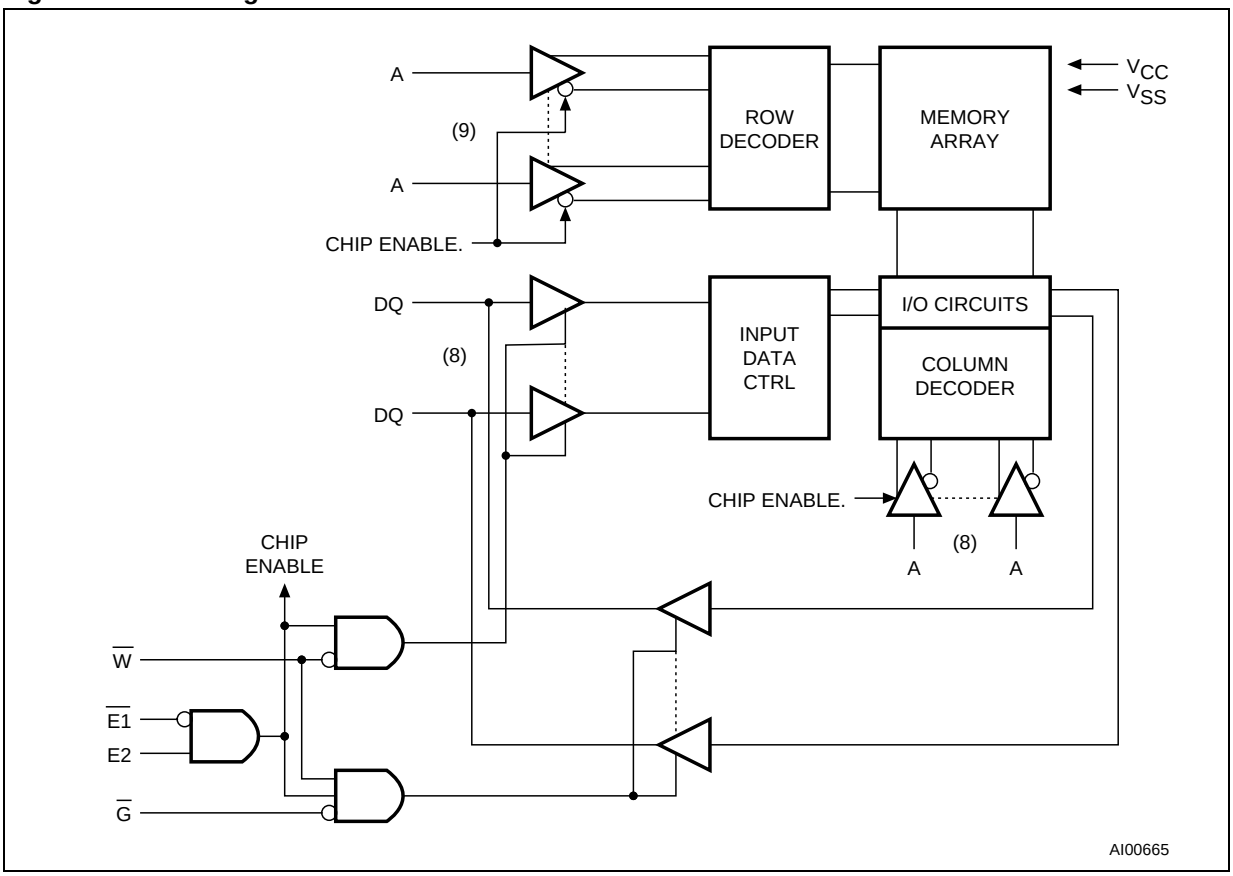


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}(1)	Storage Temperature	–65 to 150	°C
V_{IO}(2)	Input or Output Voltage	–0.5 to V_{CC} + 0.5	V
V_{CC}	Supply Voltage	–0.5 to 4.6	V
I_O(3)	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 and 120 seconds).
2. Up to a maximum operating V_{CC} of 5.5V only.
3. One output at a time, not to exceed 1 second duration.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC Measurement Conditions

Parameter	M68Z128
V_{CC} Supply Voltage	2.7 to 3.6V
Ambient Operating Temperature	0 to 70°C
Load Capacitance (C_L)	50pF
Input Rise and Fall Times	≤ 15ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output High Z is defined as the point where data is no longer driven (see Table 3, page 5).

Figure 5. AC Testing Load Circuit

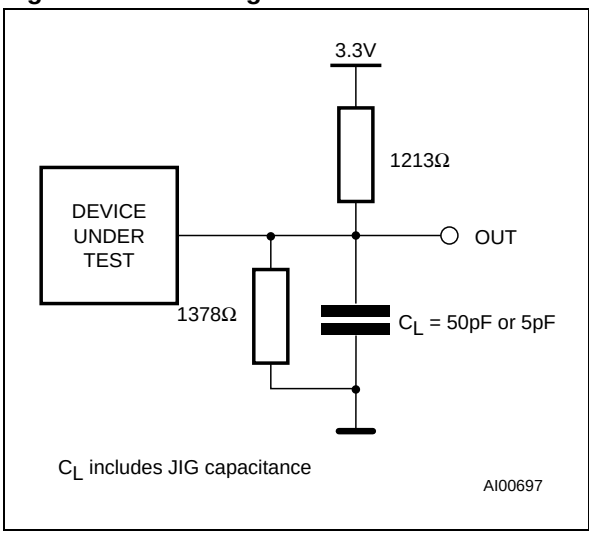


Table 4. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)		6	pF
C_{OUT}[3]	Output Capacitance		8	pF

Note: 1. Sampled only, not 100% tested.
2. Outputs deselected.
3. At 25°C.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition(1)	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le VIN \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}(2)	Supply Current	V_{CC} = 3.6V, (–70)		20	40	mA
I_{CC2}(3)	Supply Current (Standby) TTL	V_{CC} = 3.6V, $\overline{E1}$ = V_{IH} or E2 = V_{IL}, f =0		15	300	µA
I_{CC3}(4)	Supply Current (Standby) CMOS	V_{CC} = 3.6V, $\overline{E1} \ge V_{CC}$ – 0.2V or E2 ≤ 0.2V, f = 0		0.4	15	µA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4			V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. Average AC current, Outputs open, cycling at t_{AVAV} minimum.
3. All other Inputs at $V_{IL} \le 0.8V$ or $V_{IH} \ge 2.0V$.
4. All other Inputs at $V_{IL} \le 0.2V$ or $V_{IH} \ge V_{CC}$ –0.2V.

OPERATION

The M68Z128 has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E1}$ = High or E2 = Low). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast READ/WRITE cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, and E2 as summarized in the Operating Modes table.

Table 6. Operating Modes

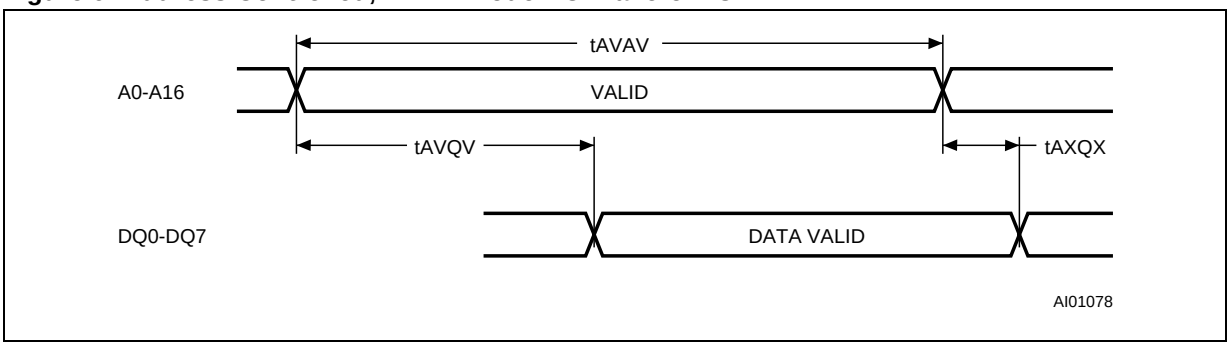
Operation	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	DQ0-DQ7	Power
READ	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	Active
READ	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Data Output	Active
WRITE	V_{IL}	V_{IH}	V_{IL}	X	Data Input	Active
Deselect	V_{IH}	X	X	X	Hi-Z	Standby
Deselect	X	V_{IL}	X	X	Hi-Z	Standby

Note: X = V_{IH} or V_{IL}.

READ Mode

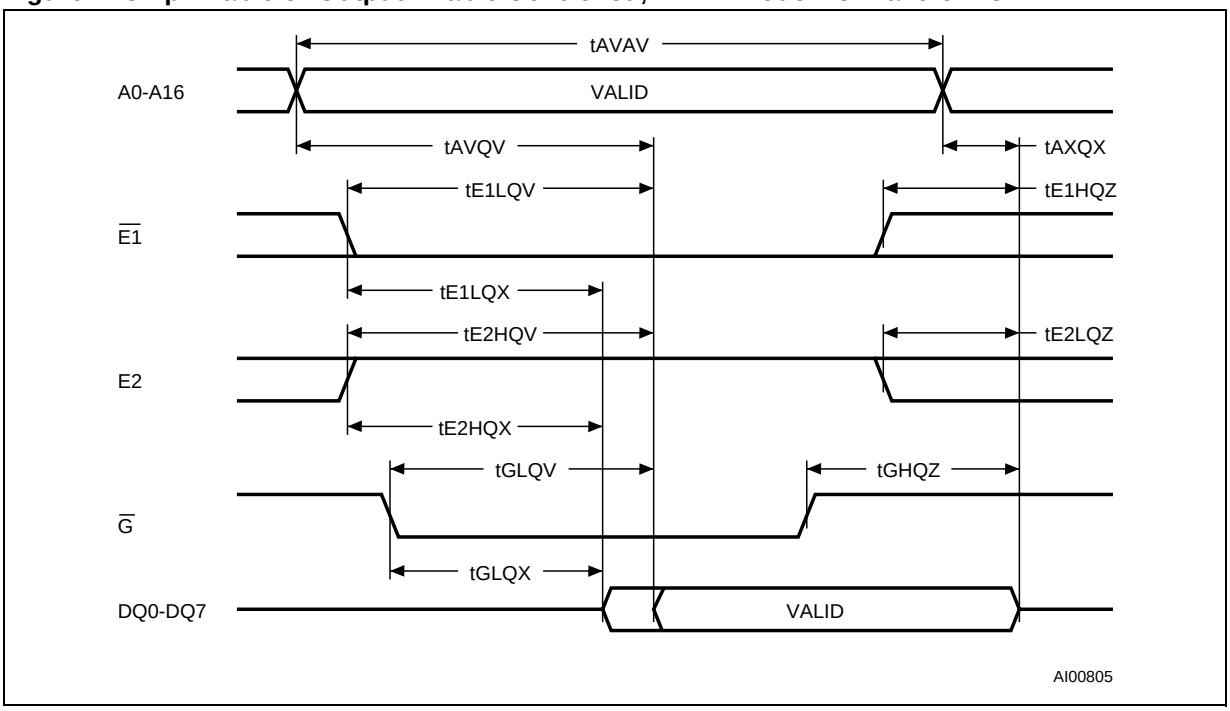
The M68Z128W is in the READ Mode whenever WRITE Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and both Chip Enables (E1 and E2) are asserted. This provides access to data from eight of the 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low, E1 is Low and E2 is High. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV}, t_{E2HQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{E1LQX}, t_{E2HQX} and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

Figure 6. Address Controlled, READ Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, +$\overline{G}$ = Low, $\overline{W}$ = High.

Figure 7. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms



Note: WRITE Enable ($\overline{W}$) = High.

Figure 8. Standby Mode AC Waveforms

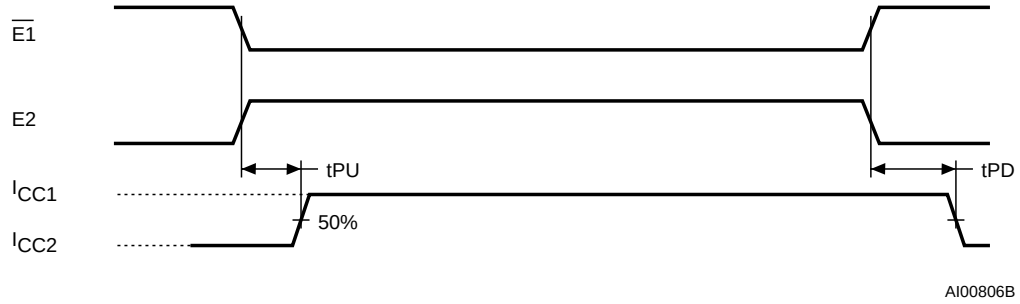


Table 7. READ and Standby Mode AC Characteristics

Symbol	Parameter[1]	M68Z128W		Unit
		–70		
		Min	Max	
t_{AVAV}	READ Cycle Time	70		ns
t_{AVQV}[2]	Address Valid to Output Valid		70	ns
t_{E1LQV}[2]	Chip Enable 1 Low to Output Valid		70	ns
t_{E2LQV}[2]	Chip Enable 2 Low to Output Valid		70	ns
t_{GLQV}[2]	Output Enable Low to Output Valid		35	ns
t_{E1LQX}[4]	Chip Enable 1 Low to Output Transition	10		ns
t_{E2LQX}[4]	Chip Enable 2 Low to Output Transition	10		ns
t_{GLQX}[4]	Output Enable Low to Output Transition	10		ns
t_{E1HQZ}[3,4]	Chip Enable 1 High to Output Hi-Z	0	25	ns
t_{E2HQZ}[3,4]	Chip Enable 2 High to Output Hi-Z	0	25	ns
t_{GHQZ}[3,4]	Output Enable High to Output Hi-Z	0	25	ns
t_{AXQX}[2]	Address Transition to Output Transition	10		ns
t_{PU}	Chip Enable Low to Power Up	0		ns
t_{PD}	Chip Enable High to Power Down		70	ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. C_L = 50pF (see Figure 5, page 5).
3. C_L = 5pF (see Figure 5, page 5).
4. At any given temperature and voltage condition, t_{EIHQZ} + t_{EZHQZ} is less than t_{EILQX} and t_{EZLQX}, t_{GHQZ} is less than t_{GLQX} for any given device.

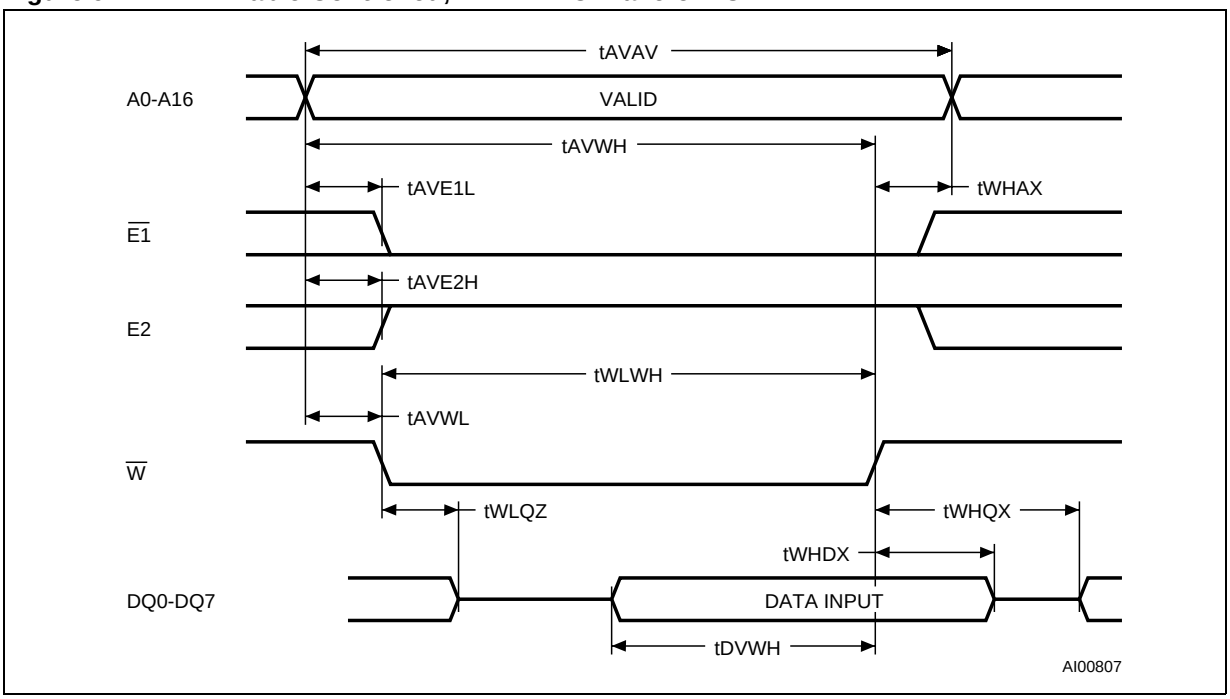
WRITE Mode

The M68Z128W is in the WRITE Mode whenever the $\overline{W}$ and $\overline{E1}$ pins are Low, with E2 High. Either the Chip Enable inputs ($\overline{E1}$ and E2) or the WRITE Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. WRITE begins with the concurrence of both Chip Enables being active with $\overline{W}$ low. Therefore, address setup time is referenced to WRITE Enable and both Chip Enables as t_{AVWL}, t_{AVE1L} and t_{AVE2H} respectively, and is determined by the latter occurring edge.

The WRITE Cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, or the falling edge of E2.

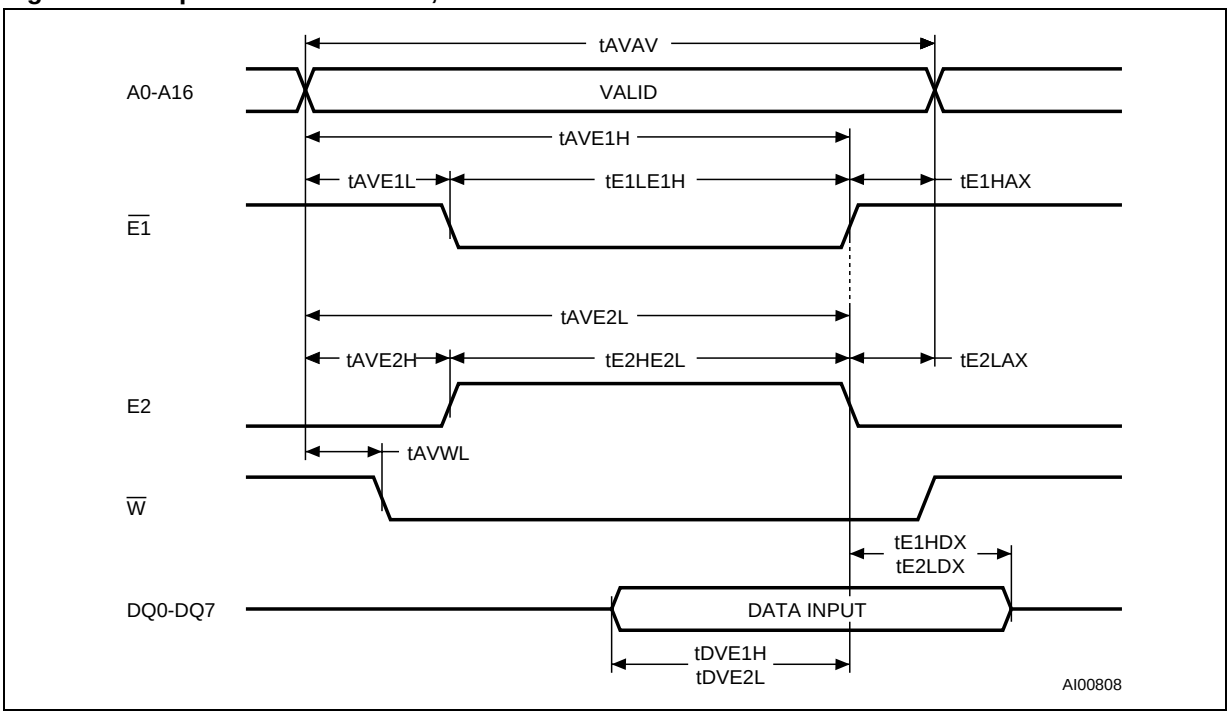
If the Output is enabled ($\overline{E1}$ = Low, E2 = High and $\overline{G}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of WRITE Enable, or for t_{DVE1H} before the rising edge of $\overline{E1}$ or for t_{DVE2L} before the falling edge of E2, whichever occurs first, and remain valid for t_{WHDX}, t_{E1HDX} or t_{E2LDX}.

Figure 9. WRITE Enable Controlled, WRITE AC Waveforms



Note: Output Enable ($\overline{G}$) = Low.

Figure 10. Chip Enable Controlled, WRITE AC Waveforms



Note: Output Enable ($\overline{G}$) = High.
If $\overline{E1}$ goes High or E2 goes Low simultaneously with $\overline{W}$ high, the output remains in a high-impedance state.

Table 8. WRITE Mode AC Characteristics

Symbol	Parameter[1]	M68Z128W		Unit
		–70		
		Min	Max	
t_{AVAV}	WRITE Cycle Time	70		ns
t_{AVWL}	Address Valid to WRITE Enable Low	0		ns
t_{AVWH}	Address Valid to WRITE Enable High	60		ns
t_{AVE1H}	Address Valid to Chip Enable 1 High	60		ns
t_{AVE2L}	Address Valid to Chip Enable 2 Low	60		ns
t_{WLWH}	WRITE Enable Pulse Width	55		ns
t_{WHAX}	WRITE Enable High to Address Transition	0		ns
t_{WHDX}	WRITE Enable High to Input Transition	0		ns
t_{WHQX}[3]	WRITE Enable High to Output Transition	0		ns
t_{WLQZ}[2,3]	WRITE Enable Low to Output Hi-Z		25	ns
t_{AVE1L}	Address Valid to Chip Enable 1 Low	0		ns
t_{AVE2H}	Address Valid to Chip Enable 2 High	0		ns
t_{E1LE1H}	Chip Enable 1 Low to Chip Enable 1 High	60		ns
t_{E2HE2L}	Chip Enable 2 High to Chip Enable 2 Low	60		ns
t_{E1HAX}	Chip Enable 1 High to Address Transition	0		ns
t_{E2HAX}	Chip Enable 2 Low to Address Transition	0		ns
t_{DVWH}	Input Valid to WRITE Enable High	30		ns
t_{DVE1H}	Input Valid to Chip Enable 1 High	30		ns
t_{DVE2H}	Input Valid to Chip Enable 2 Low	30		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. C_L = 5pF
3. At any given temperature and voltage condition, t_{WHQZ} is less than t_{WLQX} for any given device.

Figure 11. Low V_{CC} Data Retention AC Waveforms

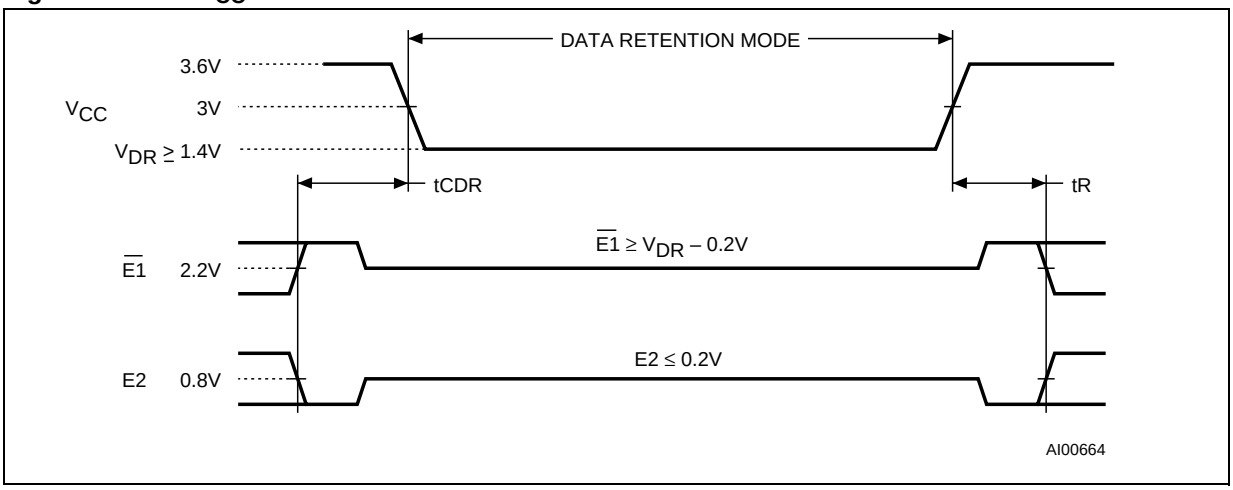


Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition(1)	Min	Typ	Max	Unit
I_{CCDR}(2)	Supply Current (Data Retention)	V_{CC} = 3V, $\overline{E1} \geq V_{CC} - 0.3V$ or $E2 \leq 0.3V$, f = 0		0.1	2	µA
V_{DR}(2)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CC} - 0.3V$ or $E2 \leq 0.3V$, f = 0	1.4			V
t_{CDR}(2,3)	Chip Disable to Power Down	$\overline{E1} \geq V_{CC} - 0.3V$ or $E2 \leq 0.3V$, f = 0	0			ns
t_{ER}(3)	Operation Recovery Time		t_{AVAV}			ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 2.7 to 3.6V (except where noted).
2. All other Inputs at $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$.
3. See Figure 11 for measurement points. Guaranteed but not tested. t_{AVAV} is READ Cycle time.

PART NUMBERING

Table 10. Ordering Information Example

Example: M68Z 128 W –70 N 1 TR

Device Type

M68Z

Device Function

128 = 1 Mbit (128Kb x 8)

Operating Voltage

W = 3.0V (+0.6 / –0.3V)

Speed

–70 = 70ns

Package

N = TSOP32 (8 x 20mm)

Temperature Range

1 = 0 to 70°C

Shipping Method for SOIC

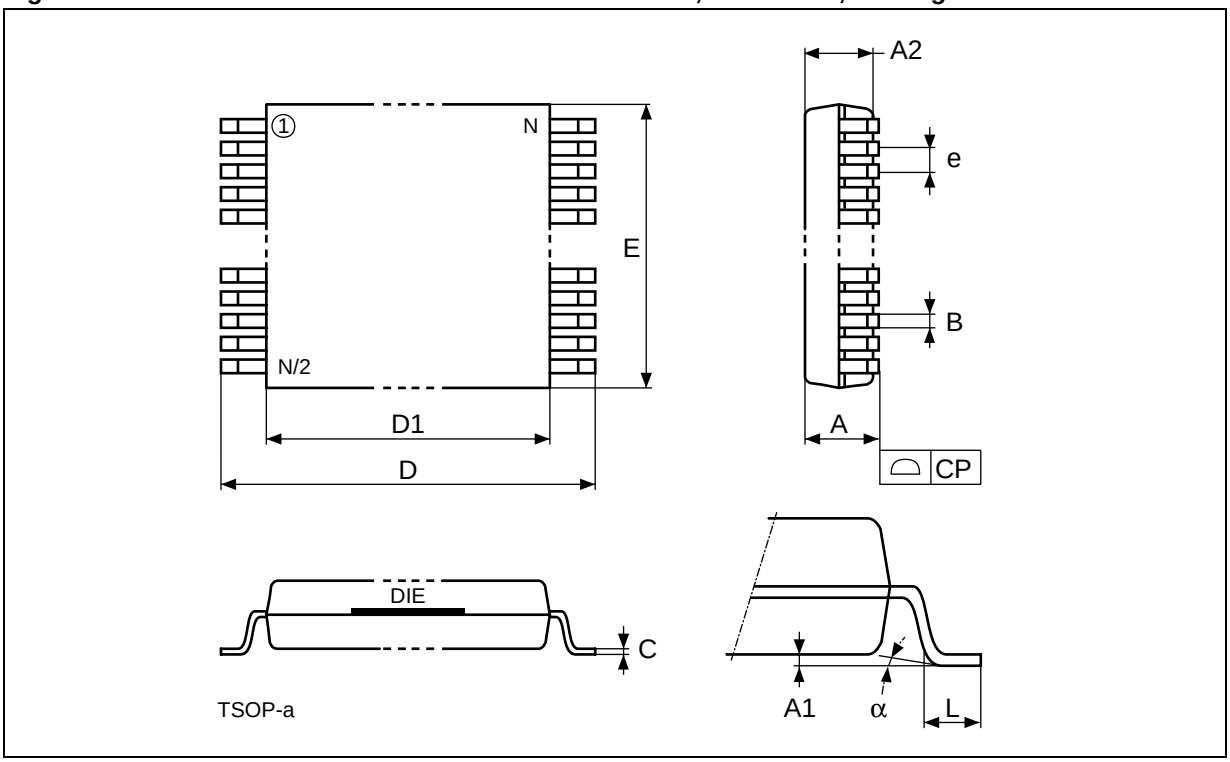
blank = Tubes

TR = Tape & Reel

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

PACKAGE MECHANICAL INFORMATION

Figure 12. TSOP32 – 32-lead Plastic Thin Small Outline, 8 x 20 mm, Package Outline



Note: Drawing is not to scale.

Table 11. TSOP32 – 32-lead Plastic Thin Small Outline, 8 x 20 mm, Package Mechanical Data

Symb	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
B		0.150	0.270		0.0059	0.0106
C		0.100	0.210		0.0039	0.0083
D		19.800	20.200		0.7795	0.7953
D1		18.300	18.500		0.7205	0.7283
e	0.500	–	–	0.0197	–	–
E		7.900	8.100		0.3110	0.3189
L		0.500	0.700		0.0197	0.0276
α		0°	5°		0°	5°
CP			0.100			0.0039
N	32			32		

REVISION HISTORY

Table 12. Document Revision History

Date	Revision Details
November 1999	First Issue
03/20/00	TSOP32 Package Mechanical Data changed (Table 11)
07/26/00	Ordering Information Scheme changed (Table 10)
09/21/00	I_{CCDR} Supply Current changed (Table 9)
04/04/01	Reformatted; temp./voltage info. added to tables (Table 4, 5, 7, 8, 9)
08/27/01	Change package to correct size in first page description (old template)
11/19/01	Correction of E2 Signal for TSOP Connections (Figure 3)
05/13/02	Add reflow time and temperature footnote (Table 2)