ADVANCED COMPONENTS PACKAGING

# 1 Gigabit Synchronous DRAM

## DPSD128MX8XKY5

**DESCRIPTION:**

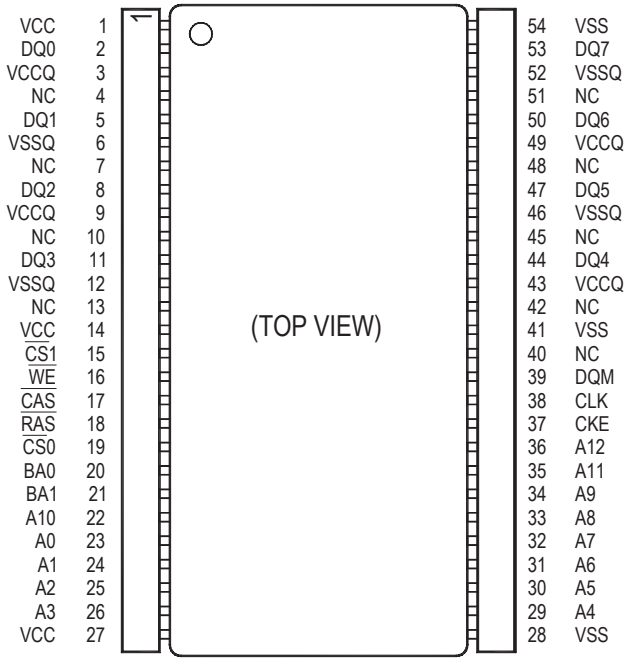
The Memory Stack™ series is a family of interchangeable memory devices. The 1 Gigabit Synchronous DRAM assembly utilizes the space saving LP-Stack™ technology to increase memory density. This stack is constructed with two 512Mb (64M x 8) SDRAMs.

This 1Gb LP-Stack™ has been designed to fit in the same footprint as the 512Mb (64M x 8) SDRAM TSOPII monolithic. This stack allows for system upgrade while providing an alternative low cost memory solution.

**FEATURES:**

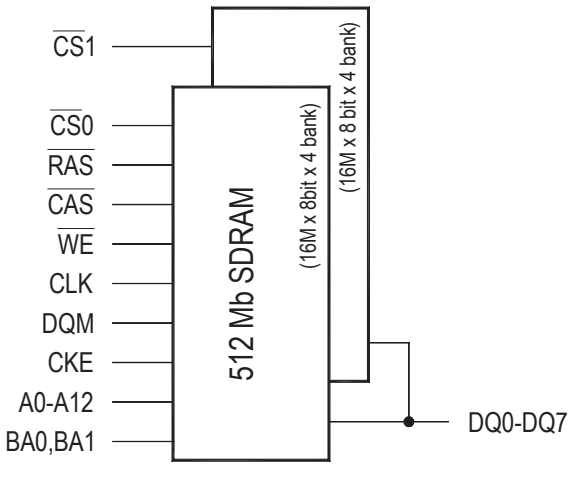
- Electrical characteristics meet semiconductor manufacturers' datasheets
- Memory organization:
  (2) 512Mb memory devices. Each device arranged as 64M x 8 bits (16M x 8 bits x 4 banks)
- Memory stack organization:
  128M x 8 bits (32M x 8 bits x 4 banks)
- JEDEC approved, 2 Rank stack pinout and footprint (with 2 CSs)
- Optimized for RDIMMs
- IPC-A-610, class 2, manufacturing standards
- Lead free manufacturing process
- Package: 54-Pin TSOPII stack

**PINOUT DIAGRAM**




| PIN NAMES | |
|---|---|
| A0-A12 | Row Address: A0-A12<br>Column Address: A0-A9, A11 |
| BA0, BA1 | Bank Select Address |
| DQ0-DQ7 | Data In/Data Out |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{WE}$ | Data Write Enable |
| DQM | Data Input/Output Mask |
| CKE | Clock Enable |
| CLK | System Clock |
| $\overline{CS0}$, $\overline{CS1}$ | Chip Selects |
| $V_{DD}/V_{SS}$ | Power Supply/Ground |
| $V_{DDQ}/V_{SSQ}$ | Data Output Power/Ground |
| NC | No Connect |

**FUNCTIONAL BLOCK DIAGRAM**



## ORDERING INFORMATION

| DP | SD | 128M | X | 8 | X | KY5 | - | DP | - | XX | X | XXX |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG | PACKAGE | | SUPPLIER | | MFR ID | MEMORY REVISION | CYCLE TIME |

| | |
|---|---|
| P12 | PC100 / CL2 |
| P13 | PC100 / CL3 |
| 12 | 12ns (83MHz) |
| 10 | 10ns (100MHz) |
| 08 | 8ns (125MHz) |
| 75 | 7.5ns (133MHz) CL3 |
| 75P2 | 7.5ns (133MHz) CL2 |
| 70 | 7ns (143MHz) CL3 |
| 70P2 | 7ns (133MHz) CL2 |
| 60 | 6ns (166MHz) CL2 |
| 55 | 5.5ns (183MHz) CL3 |

BLANK REVISION NOT SPECIFIED
n PER MANUFACTURER DIE REVISION

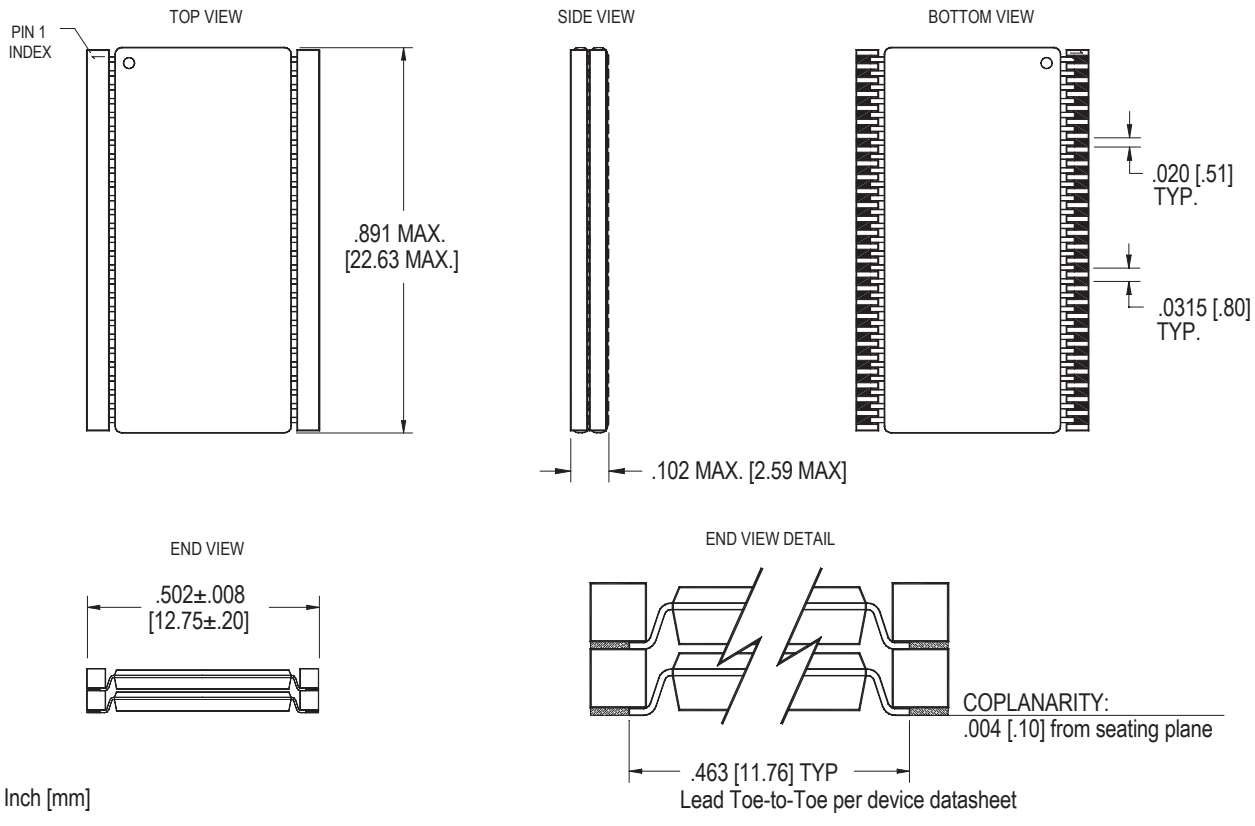
MANUFACTURER CODE *
SUPPLIER CODE *
STACKABLE TSOP
256 MEGABIT LVTTL BASED
MODULE WITHOUT SUPPORT LOGIC
SYNCHRONOUS DRAM

* Contact your sales representative for supplier and manufacturer codes.

**NOTE:**

1. AC Parameters of base memory are unchanged from device manufacturers' specifications.
2. DC Parameters may be affected by stacking. Please refer to application note 53A004-00 for further information.
3. For assembly and inspection procedures, refer to application note 53A001-00.
4. Maximum reflow temperature recommendation is 215°C.

## MECHANICAL DIAGRAM






DPAC TECHNOLOGIES
**DPAC Technologies** Products & Services for the Integration Age
7321 Lincoln Way, Garden Grove, CA 92841 **Tel** 714 898 0007 **Fax** 714 897 1772
www.dpactech.com Nasdaq: DPAC