64K

X40620

Dual Voltage CPU Supervisor with 64K Serial EEPROM

FEATURES

- **Dual Voltage Detection and Reset Assertion**
  - **—Three standard reset threshold settings. (3.1V/ 2.6V, 3.1V/1.7V, 2.9V/2.3V)**
  - **—Adjust low voltage reset threshold voltages using special programming sequence**
  - **—$\overline{\text{RESET}}$ signal valid down to V_{CC}=1V**
- **Watchdog Timer (150ms)**
- **Power On Reset (150ms)**
- **Low Power CMOS**
  - **—10µA typical standby current, watchdog on**
  - **—400µA typical standby current, watchdog off**
- **64kbit 2-Wire Serial EEPROM**
  - **—1MHz serial interface speed**
  - **—64-byte page write mode**
  - **—Self-timed write cycle**
  - **—5ms write cycle time (typical)**
- **2.5 to 3.7V Power Supply Operation**
- **8-Lead TSSOP package**

DESCRIPTION

The X40620 combines several functions into one device. The first is a dual voltage monitoring, power-on reset control, watchdog timer and 64Kbit serial EEPROM memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

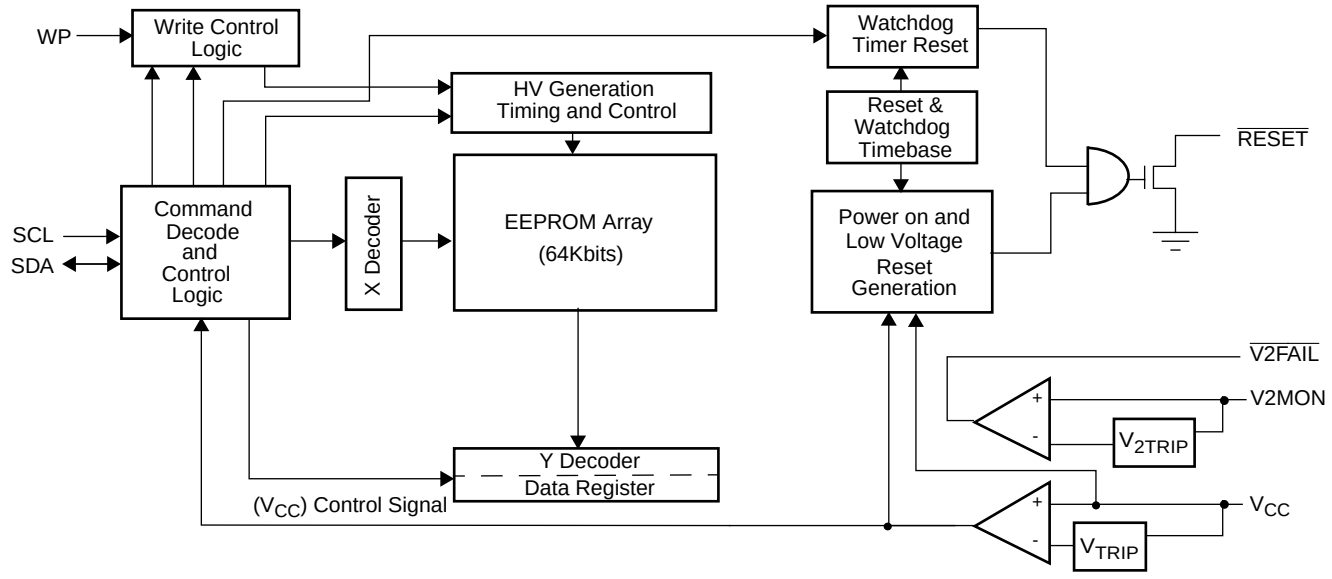
Applying voltage to V_{CC} activates the power on reset circuit which holds $\overline{\text{RESET}}$ active for a period of time. This allows the power supply and system oscillator to stabilize before the processor can execute code.

Low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the set minimum Vtrip point. $\overline{\text{RESET}}$ is active until V_{CC} returns to proper operating level and stabilizes.

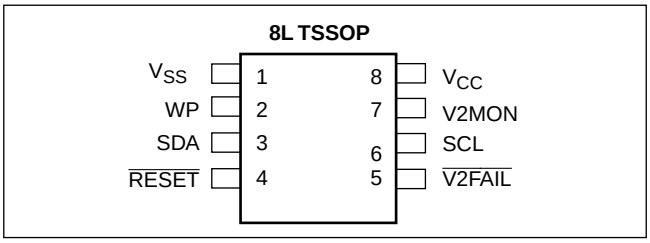
A second voltage monitor circuit (V2MON) tracks the unregulated supply to provide a power fail warning or monitors different power supply voltage. When the second monitored voltage drops below a preset $V2_{TRIP}$ voltage. $\overline{\text{V2FAIL}}$ is active until V2 returns to proper operating level and above the $V2_{TRIP}$ voltage.

Five common low voltage combinations are available, however, Xicor's unique circuits allows the threshold for either voltage monitor to be reprogrammed to meet special needs or to fine-tune the threshold for applications requiring higher precision.

BLOCK DIAGRAM



PACKAGE/PINOUTS



PIN NAMES

V_{SS}	Ground
SDA	Serial Data
V_{CC}	Power
SCL	Serial Clock
WP	Write Protect
V2MON	Voltage monitor input
$\overline{RESET}$	Low Voltage Detect Output
$\overline{V2FAIL}$	V2 Voltage Fail Output

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with other open drain or open collector outputs. An open drain requires the use of a pull-up resistor.

Write Protect (WP)

The WP pin should be tied HIGH at all time. (This WP pin is reserved for internal factory testing only).

Reset Output ($\overline{RESET}$)

$\overline{RESET}$ is an active LOW, open drain output which goes active whenever V_{CC} falls below the minimum Vtrip sense level. It will remain active until V_{CC} rises above the minimum Vtrip sense level for 150ms. $\overline{RESET}$ goes active if the Watchdog Timer is enabled and there is no start bit before the end of the selectable Watchdog time-out period. A serial start bit will reset the Watchdog Timer. $\overline{RESET}$ also goes active on power up at 1V and remains active for 150ms after the power supply stabilizes.

V2 Voltage Fail Output ($\overline{V2FAIL}$)

$\overline{V2FAIL}$ is an active LOW, open drain output which goes active whenever V2MON falls below the minimum V2trip sense level. It will remain active until V2MON rises above the minimum V2MON sense level.

DEVICE OPERATION

Power On Reset

Application of power to the X40620 activates a Power On Reset Circuit. This circuit goes active at 1V and pulls the $\overline{RESET}$ pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When V_{CC} exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{RESET}$ allowing the processor to begin executing code.

Low Voltage V_{CC} (V1) Monitoring

During operation, the X40620 monitors the V_{CC} level and asserts $\overline{RESET}$ if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{RESET}$ signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$ signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

When the internal low voltage detect circuitry senses that V_{CC} is low, the following happens:

– The $\overline{RESET}$ pin goes active.

– Communication to the device is interrupted and any command is aborted. If a serial nonvolatile store is in progress when power fails, the circuitry does not stop the nonvolatile store operation, but attempts to complete the operation.

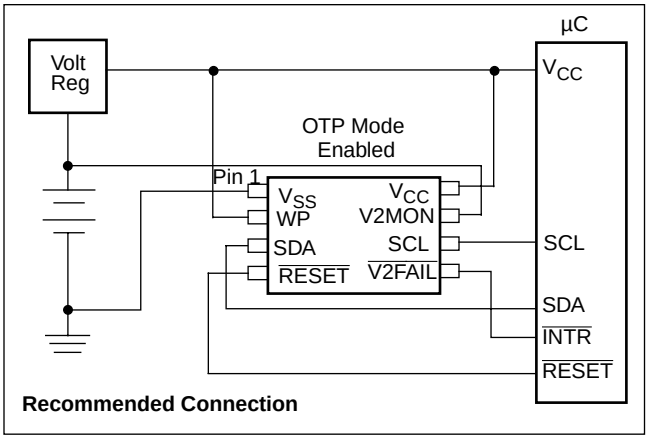
The low V_{CC} threshold is typically set to 3.1V for a 2.5 to 3.7V operating range.

LOW VOLTAGE V2 MONITORING

The X40620 also monitors a second voltage level and asserts $\overline{V2FAIL}$ if the voltage falls below a preset minimum $V2_{TRIP}$. The $\overline{V2FAIL}$ signal is either ORed with RESET to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure. The $\overline{V2FAIL}$ signal remains active until the V_{CC} drops below 1V. It also remains active until V2MON returns and exceeds $V2_{TRIP}$ by 0.2V

When the internal low voltage detect circuitry senses that V2MON is low, the $\overline{V2FAIL}$ pin goes active. Typically this would be used by the processor as an interrupt to stop the execution of the code or to do housekeeping in preparation for an impending power failure.

The $\overline{RESET}$ and $\overline{V2FAIL}$ signals remain active until V_{CC} voltage drops below 1V. $\overline{RESET}$ remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms. $\overline{V2FAIL}$ remains active until immediately after V2MON returns and exceeds it's minimum voltage.



Recommended Connection

Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the Start bit. The microprocessor must send a start bit periodically to prevent a $\overline{RESET}$ signal. The start bit must occur prior to the expiration of the watchdog time-out period. The watchdog timer period is set at 150msec.

SERIAL MEMORY OPERATION

There are two primary modes of operation for the X40620; READ and WRITE of the memory arrays.

The basic method of communication to the memory areas of the device is established by generating a start condition, then transmitting a command, followed by the address. The user must perform ACK Polling to determine the validity of the address, before starting a data transfer (see Acknowledge Polling.)

Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

If the X40620 is in a nonvolatile write cycle a "no ACK" (SDA=HIGH) response will be issued in response to loading of the command byte. If a stop is issued prior to the start of a nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

The basic sequence is illustrated in Figure 1.

After each transaction is completed, the X40620 will reset and enter into a standby mode.

Figure 1. X40620 Device Operation

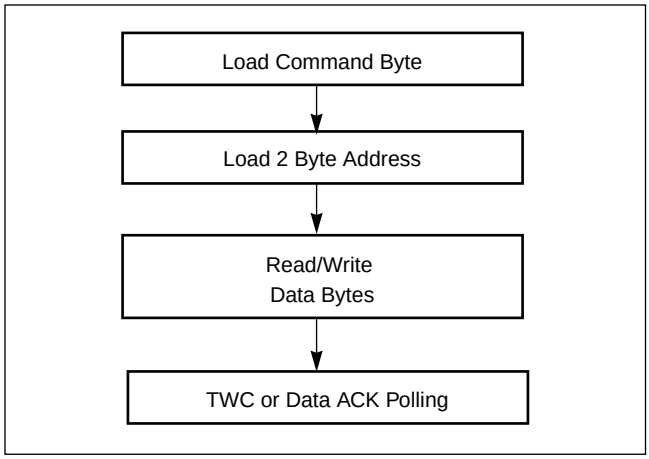


Figure 2. Set V_{TRIP} Level Sequence ($V_{CC} \geq V_{TRIP}$)

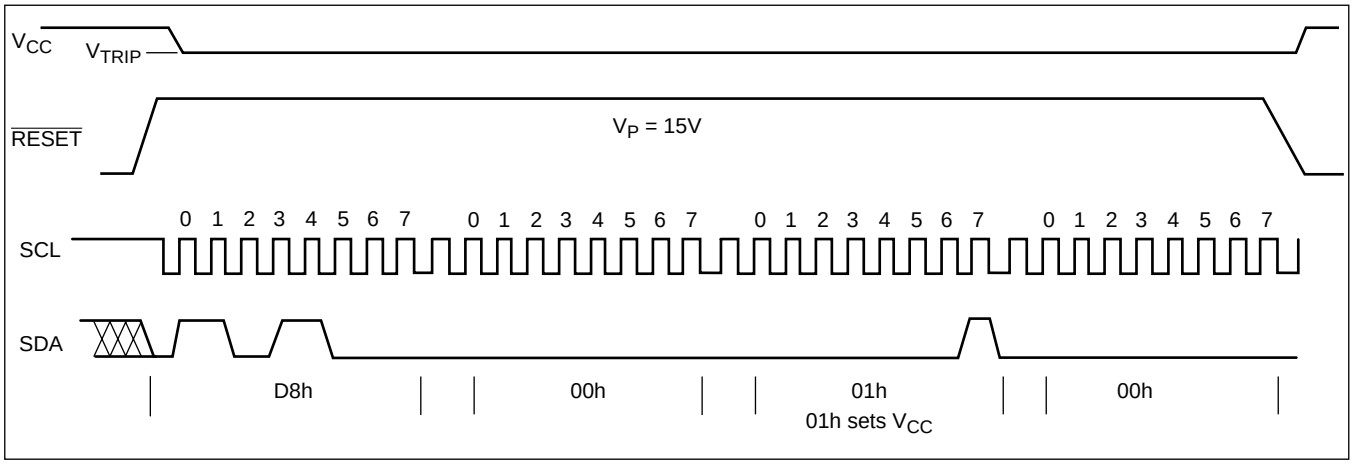


Figure 3. Set $V2_{TRIP}$ Level Sequence ($V_{CC} \geq V2_{TRIP}$)

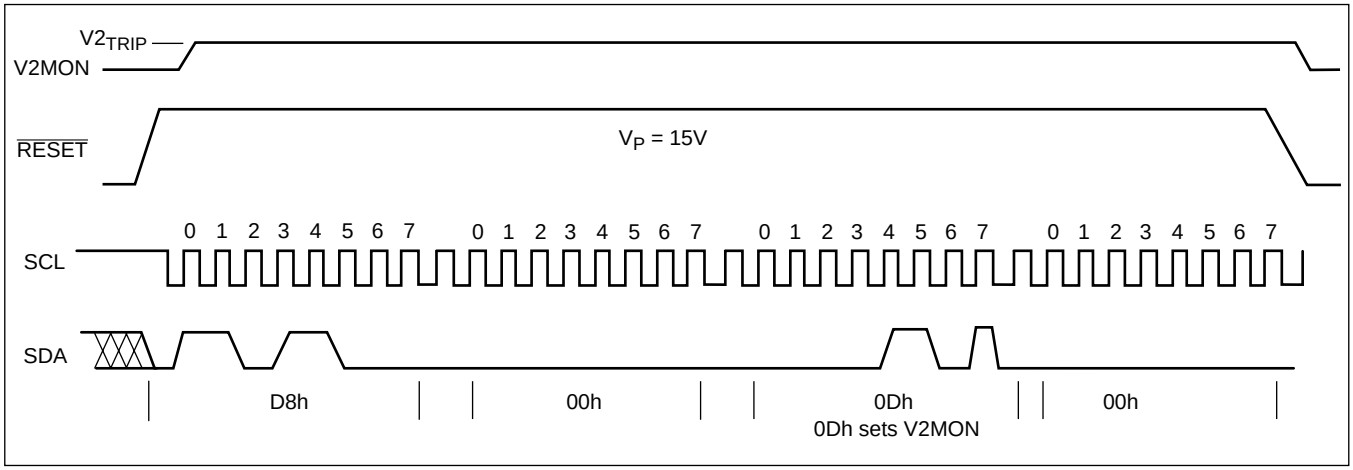


Figure 4. Reset V_{TRIP} Level Sequence (V_{CC} > 3V, WEL is set.)

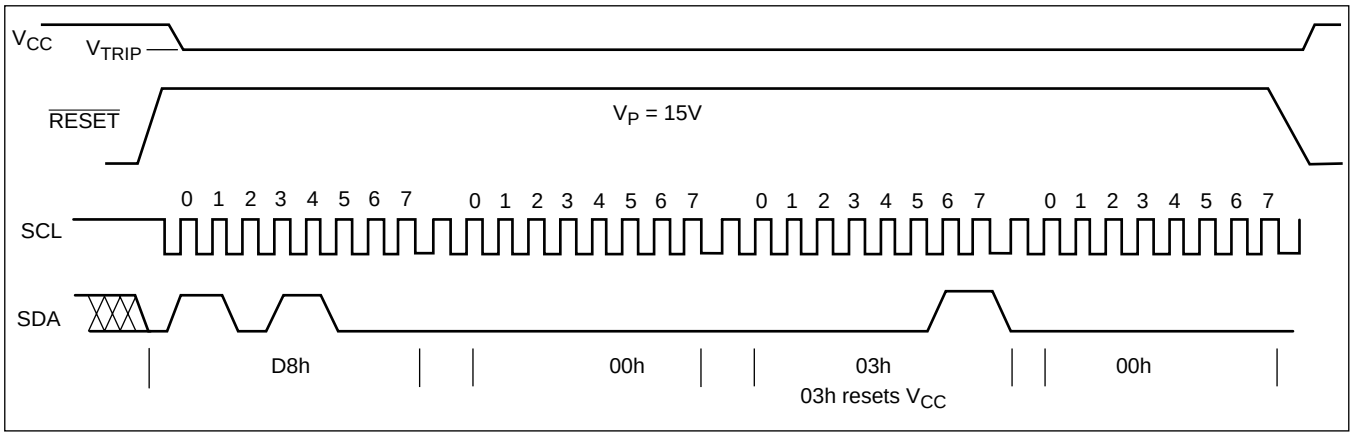
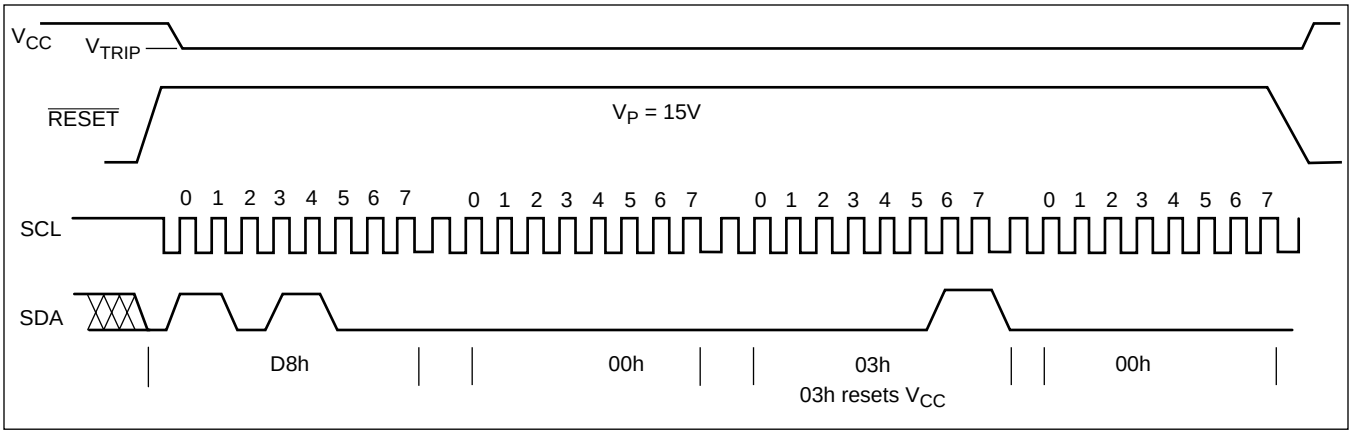


Figure 5. Reset $V2_{TRIP}$ Level Sequence (V_{CC} > 3V, WEL is set.)



V_{CC} AND V2MON THRESHOLD RESET PROCEDURE

The X40620 is shipped with standard V_{TRIP} and $V2_{TRIP}$ voltages. These values will not change over normal operating and storage conditions. However, in applications where the standard thresholds are not exactly right, or if higher precision is needed in the threshold value, the X40620 trip points may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP},$V2_{TRIP}$ to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

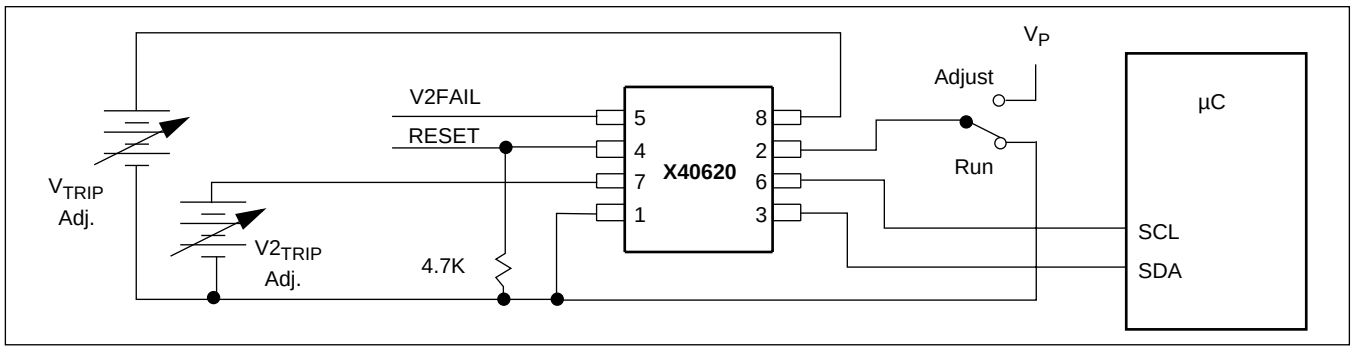
To set the new voltages, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin, the $V2_{TRIP}$ voltage to the V2MON pin, then tie the $\overline{RESET}$ pin to the programming voltage V_P. Then, write data 01h or 0Dh at address 00h to program V_{TRIP}, $V2_{TRIP}$ respectively. The stop bit following a valid write operation initiates the programming sequence. Bring $\overline{RESET}$ LOW to complete the operation. Note: this operation also writes 01h or 0Dh to address 00h.

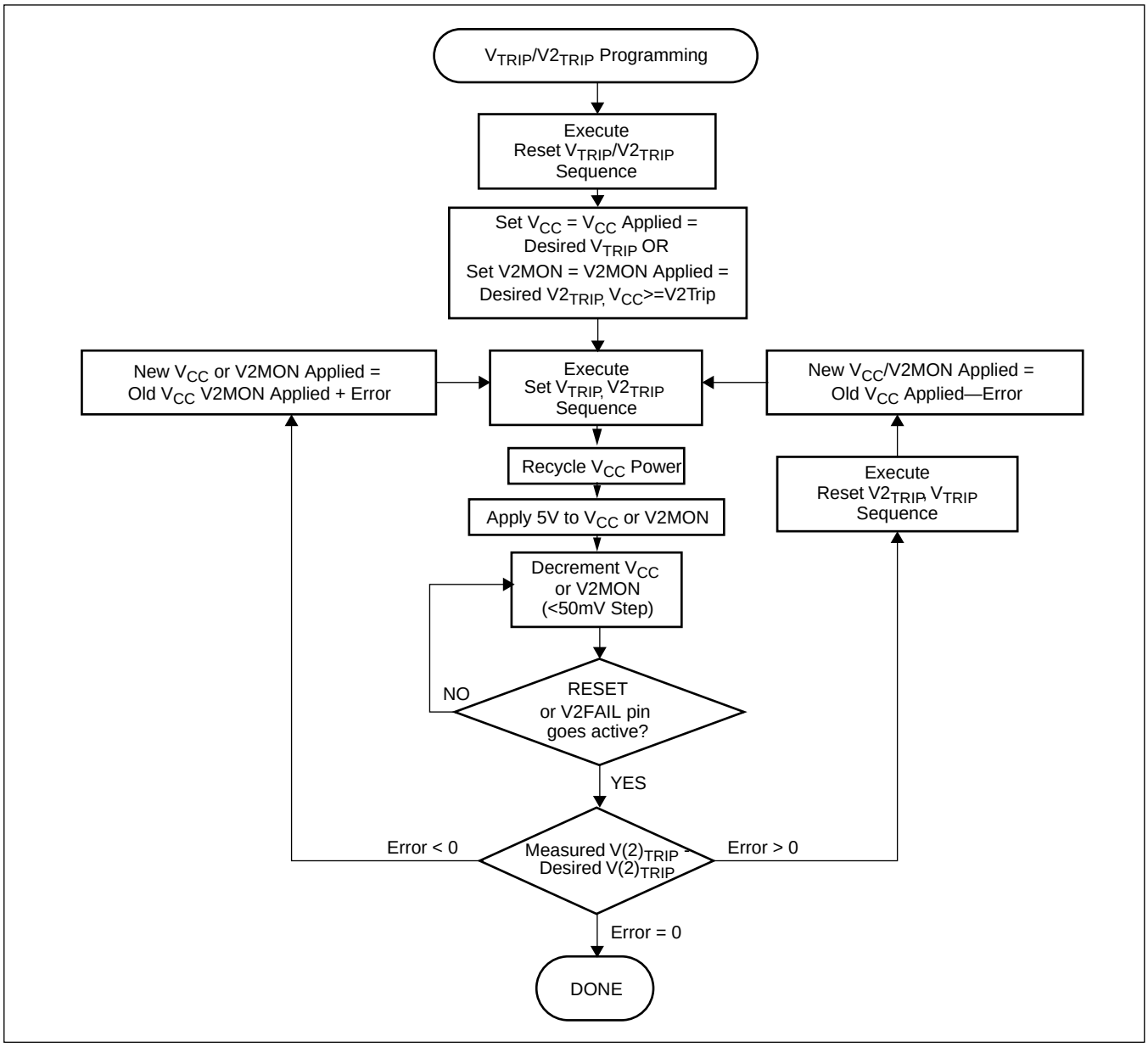
Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP}, the $V2_{TRIP}$ to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When the threshold is reset, the new level is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP}, $V2_{TRIP}$ voltage, apply the desired V_{TRIP} or $V2_{TRIP}$ threshold voltage to the V_{CC}or V2MON pin, respectively, and tie the $\overline{RESET}$ pin to the programming voltage V_P. Then write 03h or 0Fh to address 00h. The stop bit of a valid write operation initiates the programming sequence. Bring $\overline{RESET}$ LOW to complete the operation. Note: this operation also writes 03h or 0Fh to address 00h of the EEPROM array.

Figure 6. Sample V_{TRIP} Reset Circuit




$V_{TRIP}/V2_{TRIP}$ Programming
Execute Reset $V_{TRIP}/V2_{TRIP}$ Sequence
Set V_{CC} = V_{CC} Applied = Desired V_{TRIP} OR Set V2MON = V2MON Applied = Desired $V2_{TRIP}$, V_{CC}>=V2Trip
New V_{CC} or V2MON Applied = Old V_{CC} V2MON Applied + Error
Execute Set V_{TRIP}, $V2_{TRIP}$ Sequence
New V_{CC}/V2MON Applied = Old V_{CC} Applied—Error
Recycle V_{CC} Power
Execute Reset $V2_{TRIP}$, V_{TRIP} Sequence
Apply 5V to V_{CC} or V2MON
Decrement V_{CC} or V2MON (<50mV Step)
NO
RESET or V2FAIL pin goes active?
YES
Error < 0
Measured $V(2)_{TRIP}$ - Desired $V(2)_{TRIP}$
Error > 0
Error = 0
DONE

Device Protocol

The X40620 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as a receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X40620 will be considered a slave in all applications.

After each byte written to or read from the X40620, the address pointer is incremented by 1. This allows the user to read from the entire device after sending only a single address. It also allows an entire page to be written in one operation. An exception to this address incrementation occurs during a read. After reading address 1FFFh the device goes into an idle mode, so additional reads return all “1s”.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figure 7 and Figure 8.

Start Condition

All commands are preceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X40620 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

A start may be issued to terminate the input of a control byte or the input data to be written. This will reset the device and leave it ready to begin a new read or write command. A start bit generated while the part is outputting data is accepted as a start as long as the device is not outputting a ’zero’.

Stop Condition

All communications are be terminated by a stop condition. The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to reset the device during a command or data input sequence and will leave the device in the standby power mode. As with starts, stops are recognized while the device outputs data, as long as the data output is not a ‘zero’.

Figure 7. Data Validity

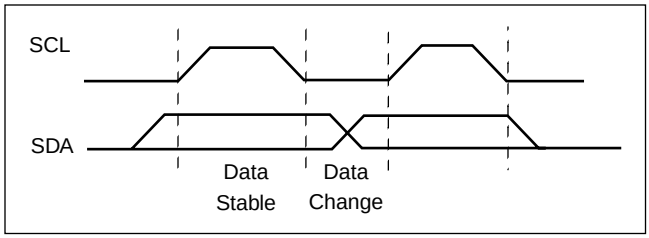
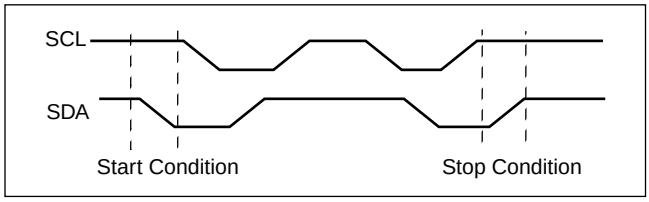


Figure 8. Definition of Start and Stop Conditions



Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

The X40620 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write condition have been selected, the X40620 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

Table 1. X40620 Instruction Set

1st Byte after Start	1st Byte after Command	2nd Byte after Command	Command Description
1100 1000	High Address	Low address	Memory Array Read
1101 1000	High Address	Low address	Memory Array Write

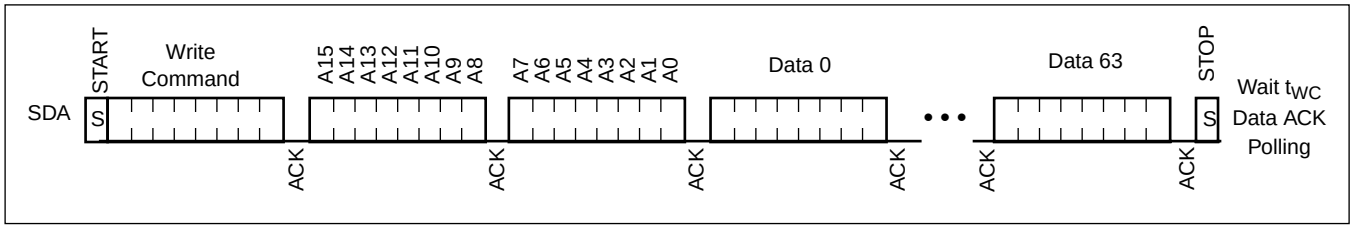
Notes: Illegal command codes will be disregarded. The part will respond with a “no-ACK” to the illegal byte and then return to the standby mode.

PROGRAM OPERATIONS

Memory Array Programming

The memory array program mode requires issuing the 8-bit Write command followed by the address and then the data bytes transferred as illustrated in Figure 9. Up to 64 bytes (or more) may be transferred. Sending more than 64 bytes results in data wrapping and over-writing previous data. After the last byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle.

Figure 9. Memory Array Programming



ACK Polling

Once a stop condition is issued to indicate the end of the host's write sequence, the X40620 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can begin immediately. This involves issuing the start condition followed by the new command code of 8 bits (1st byte of the protocol.) If the X40620 is still busy with the nonvolatile write operation, it will issue a "no-ACK" in response. If the nonvolatile write operation has completed, an "ACK" will be returned and the host can then proceed with the rest of the protocol.

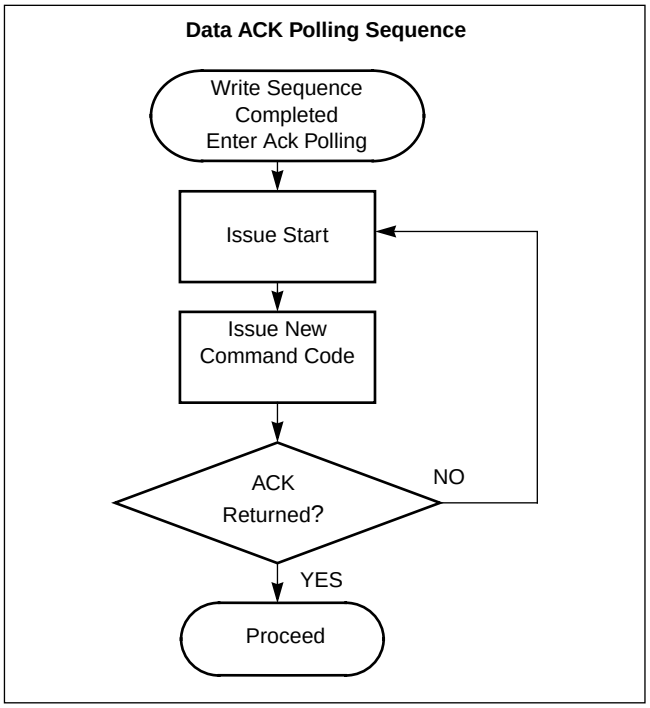
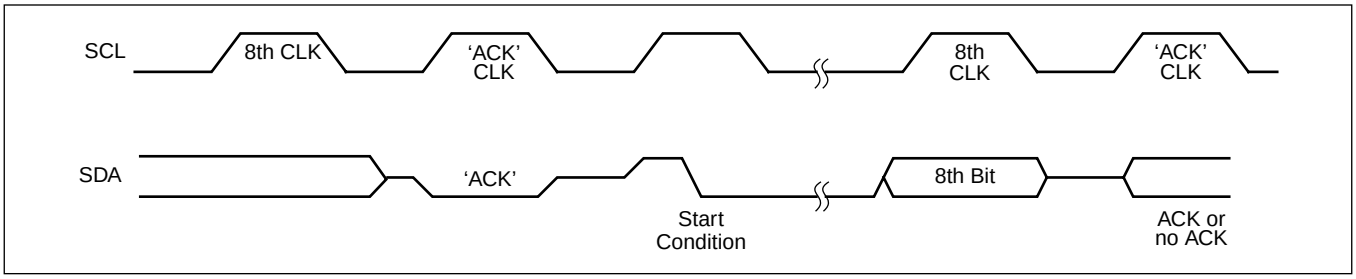


Figure 10. Acknowledge Polling



MEMORY READ OPERATIONS

Memory read operations are initiated in the same manner as write operations but with a different command code.

Random Read

The master issues the start condition, then a Read instruction, then issues the word address. Once the first byte has been read, another start can be issued followed by a new 8-bit address. See Figure 11.

Sequential Read

The host can read sequentially within the memory array after receiving the Read Command and an address within the address space. The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory array contents to be serially read during one operation. At the end of the address space (address 1FFFh) the device goes into an idle state and a new read sequence must be initiated to continue reading at another address. Refer to Figure 12 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, the host sends a stop condition with or without a preceding acknowledge.

Figure 11. Random Read

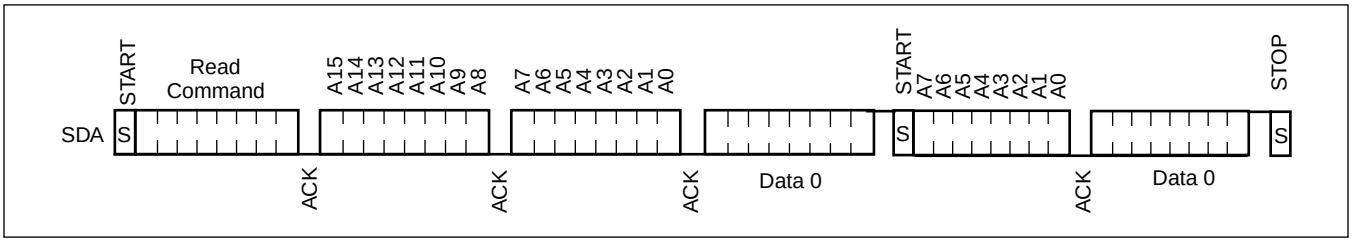
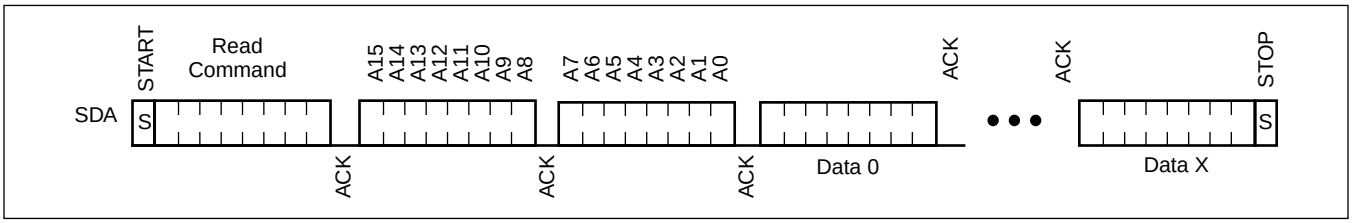


Figure 12. Sequential Read



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... –65°c to +135°C
Storage temperature .....–65°C to +150°C
Voltage on any pin with respect to V_{SS}..... –1V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds).....300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C

Device	Supply Voltage Limits
X40620	2.5V to 3.7V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

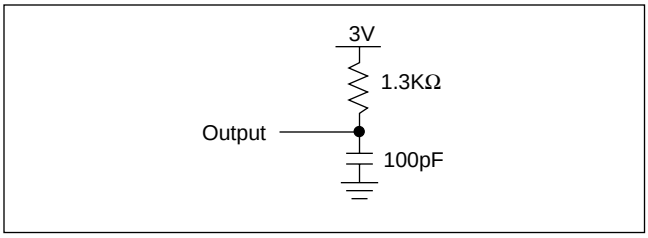
Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	f_{SCL} = 1MHz, $\overline{RESET}$ = $\overline{V2FAIL}$ = V_{CC} w/ pull up resistor V_{2MON} = V_{CC}
I_{CC2}(3)	V_{CC} Supply Current (Write)		3	mA	f_{SCL} = 1MHz, $\overline{RESET}$ = $\overline{V2FAIL}$ = V_{CC} w/ pull up resistor RST = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		50	µA	V_{IL} = V_{CC} x 0.1, V_{IH} = V_{CC} x 0.9 f_{SCL} = 1MHz, f_{SDA} = 400 KHz
I_{SB2}(1)	V_{CC} Supply Current (Standby)		1	µA	V_{SDA} = V_{SCL} = V_{2MON} = V_{CC} Other = GND or V_{CC}–0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL1}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	V_{CC} = 3.0V
V_{IH1}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	V_{CC} = 3.0V
V_{IL2}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.1	V	V_{CC} = 3.0V
V_{IH2}(2)	Input HIGH Voltage	V_{CC} x 0.9	V_{CC} + 0.5	V	V_{CC} = 3.0V
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

CAPACITANCE (T_A = +25°C, F = 1MHZ, V_{CC} = 3V)

Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (WP, SCL, V_{2MON})	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command after a read command prior to measurement
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5
Output load	100pF

AC CHARACTERISTICS

AC Specifications (Over the recommended operating conditions)

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
f_{SCL}	SCL Clock Frequency	0		1000	KHz
t_{IN}	Pulse width of spikes which must be suppressed by the input filter	10			ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.05		0.55	µs
t_{BUF}	Time the bus must be free before a new transmit can start	0.5			µs
t_{LOW}	Clock LOW Time	0.6			µs
t_{HIGH}	Clock HIGH Time	0.4			µs
$t_{SU:STA}$	Start Condition Setup Time	0.25			µs
$t_{HD:STA}$	Start Condition Hold Time	0.25			µs
$t_{SU:DAT}$	Data In Setup Time	100			ns
$t_{HD:DAT}$	Data In Hold Time	0			µs
$t_{SU:STO}$	Stop Condition Setup Time	0.25			µs
t_{DH}	Data Output Hold Time	0	100		ns
t_R	SDA and SCL Rise Time (10% to 90% of V_{CC})	10		100	ns
t_F	SDA and SCL Fall Time	10		100	ns

RESET AC SPECIFICATIONS

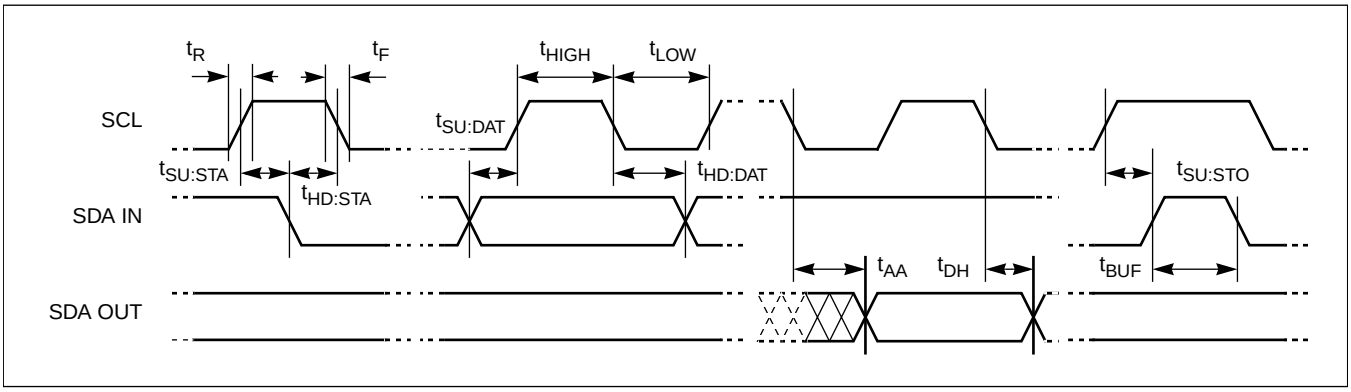
Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(1)	Write Cycle Time		5	10	mS

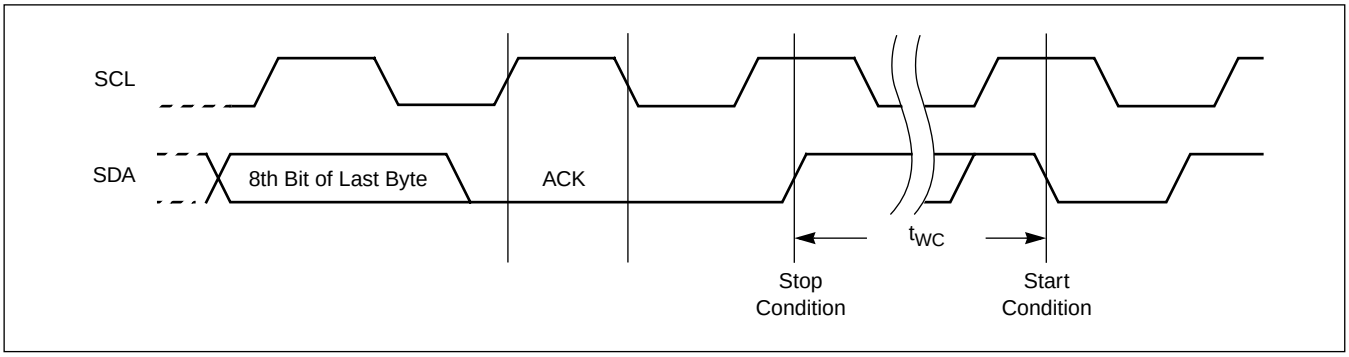
Notes: (1) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

TIMING DIAGRAMS

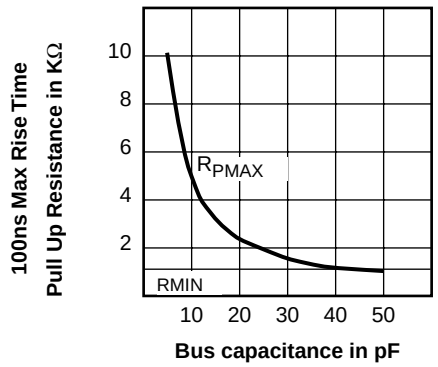
Bus Timing



Write Cycle Timing



GUIDELINES FOR CALCULATING TYPICAL VALUES OF BUS PULL UP RESISTORS



$$R_{MIN} = \frac{V_{CCMAX} - 0.4}{I_{OLMIN}} = 1100\Omega$$

$$V_{IH} = Vcc\left(1 - e^{\frac{-t_{RMAX}}{R_{PMAX}C_{BUS}}}\right)$$

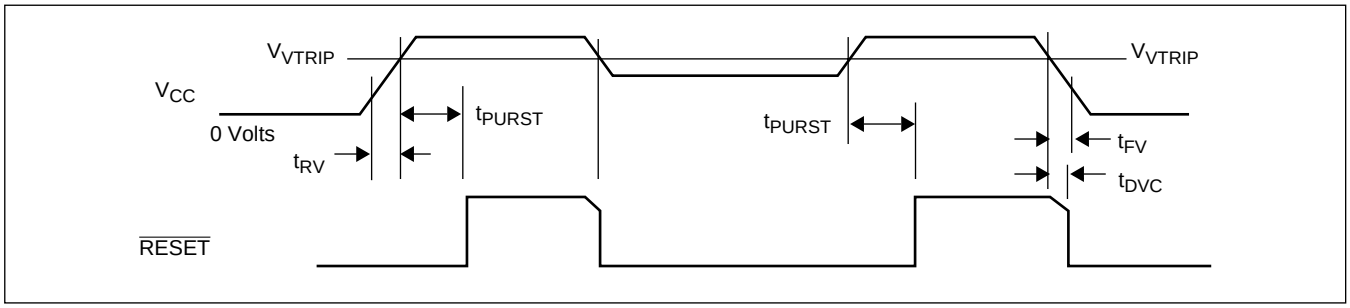
For $V_{IH} = 0.9V_{CC}$

$$R_{PMAX} = \frac{t_R}{2.3(C_{BUS})}$$

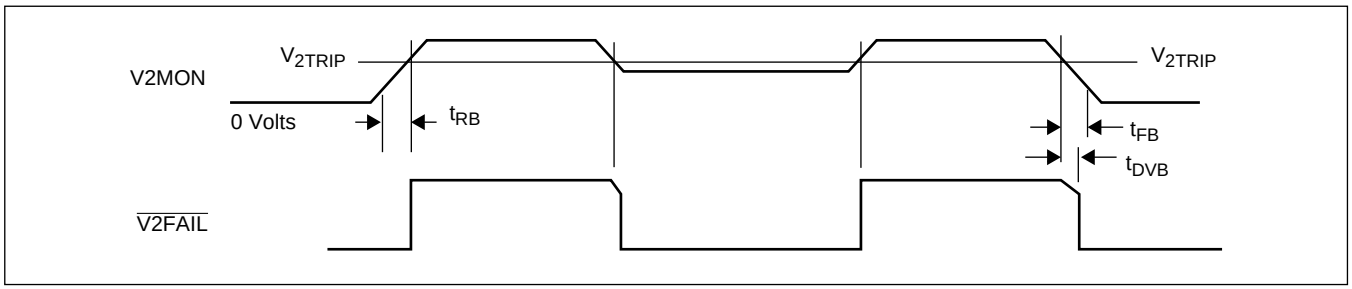
t_{RMAX} = maximum allowable SDA rise time

POWER-UP AND POWER-DOWN TIMING

$\overline{\text{RESET}}$ Output Timing



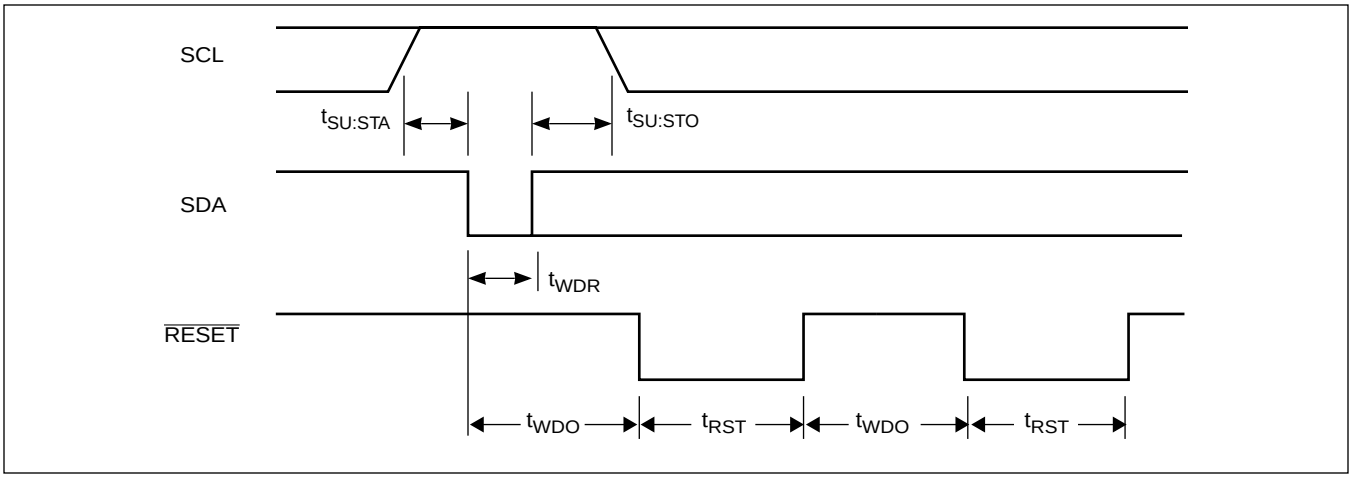
$\overline{\text{V2FAIL}}$ Output Timing



Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	$\overline{\text{RESET}}$ Trip Point Voltage	2.4	–	3.5	V
V_{2TRIP}	$\overline{\text{V2FAIL}}$ Trip Point Voltage	1.7	–	3.5	V
V_{TH}	V_{TRIP} Hysteresis (HIGH to LOW vs. LOW to HIGH V_{TRIP} voltage)		40		mV
V_{2TA}	V_{2TRIP} Hysteresis (HIGH to LOW vs. LOW to HIGH V_{TRIP} voltage)		40		mV
t_{PURST}	Power-up Reset Timeout	75	150	225	ms
t_{DVC}(5)	Detect V_{CC} Low Voltage to Reset Output (V_{CC} = 2.3V)			65	µs
t_{DVB}(5)	Detect V_{2MON} Low Voltage to Reset Output (V_{CC} = 2.5-3.7V)			100	µs
t_{FV}(5)	V_{CC} Fall Time	100			µs
t_{RV}(5)	V_{CC} Rise Time	100			µs
t_{FB}(5)	V_{2MON} Fall Time	500			ns
t_{RB}(5)	V_{2MON} Rise Time	500			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

Notes: (5) This parameter is periodically sampled and not 100% tested.
(6) Typical values not tested.

Start Bit vs. RESET Timing

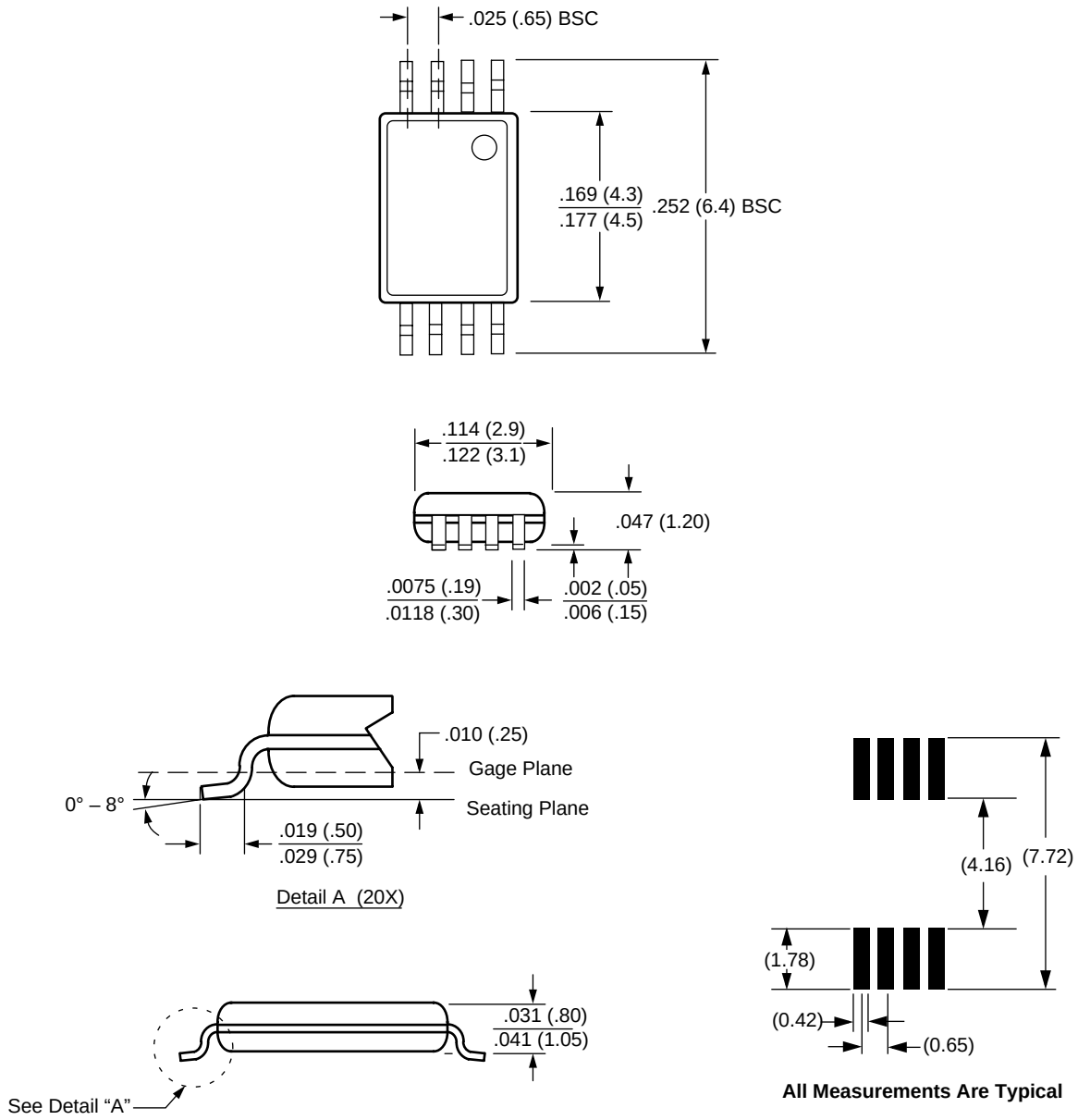


RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period	75	150	225	ms
t_{WDR}	SDA LOW duration (Reset the Watchdog)	400			ns
t_{RST}	Reset Timeout	75	150	225	ms

PACKAGING INFORMATION

8-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

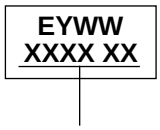
Ordering Information

V_{CC} Range	V_{TRIP}	V_{2TRIP}	Package	Operating Temperature Range	Part Number
2.5–3.7V	3.1	2.6	8L TSSOP	0°C–70°C	X40620V8-3.1
				-20°C–85°C	X40620V8E-3.1
2.5–3.7V	3.1	1.7	8L TSSOP	0°C–70°C	X40620V8-3.1A
				-20°C–85°C	X40620V8E-3.1A
2.5–3.7V	2.9	2.3	8L TSSOP	0°C–70°C	X40620V8-2.9
				-20°C–85°C	X40620V8E-2.9

Notes: Tolerance for V_{TRIP} and V_{2TRIP} are +/-5%

Part Mark Convention

8-Lead TSSOP



	V_{TRIP}	V_{2TRIP}	Temp
4062 AR =	3.1	2.6	0 to 70°C
4062 AS =	3.1	2.6	-20 to 85°C
4062 AT =	3.1	1.7	0 to 70°C
4062 AU =	3.1	1.7	-20 to 85°C
4062 AV =	2.9	2.3	0 to 70°C
4062 AW =	2.9	2.3	-20 to 85°C