Fast Logic

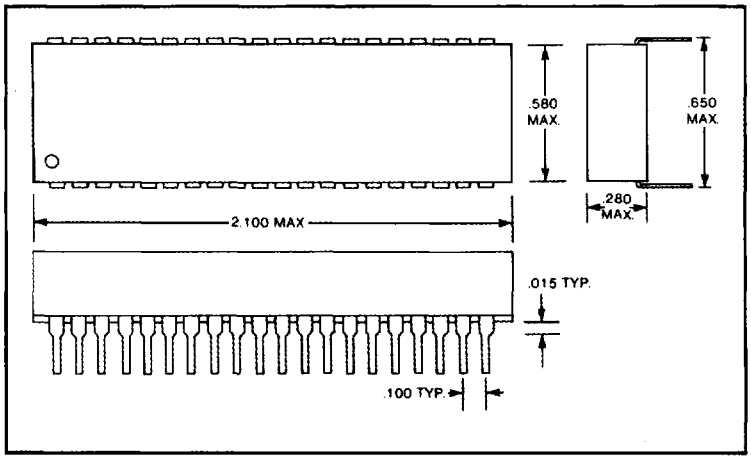
Programmable Pulse Generator

SERIES: PPG-38F
(8 Bit) TTL Interfaced

data delay devices, inc.

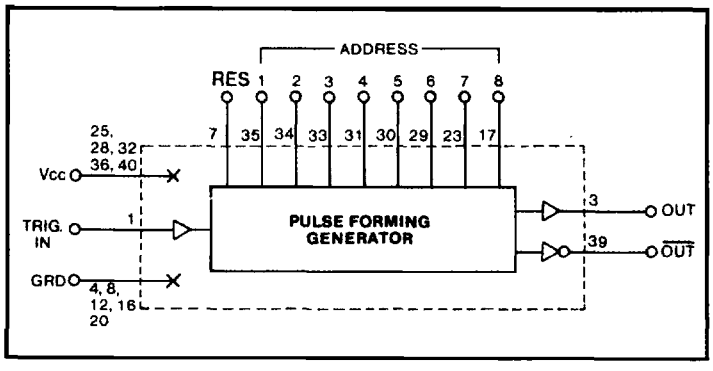
Features:

- Precise pulse width.
- Inverted & non-inverted outputs.
- 8 BIT address.
- .5 ns to 10 ns incremental steps.
- Rising-edge triggered.
- 40 pins DIP package.
- Low profile.



Specifications:

- **Trigger inherent delay T_{DO}** = 10 ns ± 2 ns.
- **Inherent pulse-width PW_0** = 17 ns ± 2 ns.
- **Pulse-width variation:** monotonic in one direction.
- **Programmed pulse-width tolerance:** ± 5% or 2 ns whichever is greater.
- **Supply voltage (Vcc):** 5 Vdc.
- **Operating temperature:** 0° C to 70° C.
- **Temperature coefficient:** 100 PPM/° C.
- **Supply current:**
  I_{CCL}: 150 ma.
  I_{CCH}: 42 ma.
- **DC parameters:** See TTL-Fast Schottky Logic Table on Page 6.



TRUTH TABLE

Address (Bit No.)								Enable RES	Pulse-Width Out
8	7	6	5	4	3	2	1		
0	0	0	0	0	0	0	0	0	T_0
0	0	0	0	0	0	0	1	0	T_1
0	0	0	0	0	1	1	1	0	T_7
0	0	0	0	1	0	0	0	0	T_8
0	0	0	0	1	1	1	1	0	T_{15}
0	0	0	1	0	0	0	0	0	T_{16}
0	0	0	1	1	1	1	1	0	T_{31}
0	0	1	0	0	0	0	0	0	T_{32}
0	0	1	1	1	1	1	1	0	T_{63}
0	1	0	0	0	0	0	0	0	T_{64}
0	1	1	1	1	1	1	1	0	T_{127}
1	0	0	0	0	0	0	0	0	T_{128}
1	1	1	1	1	1	1	1	0	T_{255}
ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	ϕ	1	0

0 = Logic 0 1 = Logic 1 ϕ = Don't care.
T_0 = Reference or inherent pulse-width of unit.
T_1 - T_{255} Multiplier of incremental pulse-width.

Part Number	Incremental Pulse-Width (ns)	Total Programmed Pulse-Width (ns)
PPG-38F-.5	.5 ± .3	127.5
PPG-38F-1	1 ± .5	255
PPG-38F-2	2 ± .5	510
PPG-38F-3	3 ± 1.0	765
PPG-38F-4	4 ± 1.0	1,020
PPG-38F-5	5 ± 1.5	1,275
PPG-38F-6	6 ± 1.5	1,530
PPG-38F-7	7 ± 1.5	1,785
PPG-38F-8	8 ± 2.0	2,040
PPG-38F-9	9 ± 2.0	2,295
PPG-38F-10	10 ± 2.0	2,550
PPG-38F-20	20 ± 2.0	5,100
PPG-38F-30	30 ± 2.0	7,650
PPG-38F-40	40 ± 2.0	10,200
PPG-38F-50	50 ± 2.5	12,750

Other customized units available.

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