mosaic

Mosaic Semiconductor Inc.

128K x 8 SRAM

MSM8128-020/025/35

Issue 1.2 : November 1993

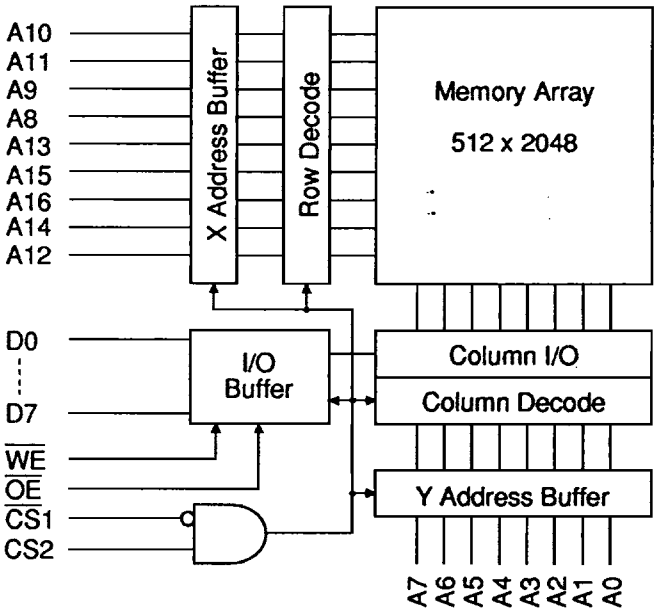
ADVANCE PRODUCT INFORMATION

131,072 x 8 CMOS High Speed Static RAM

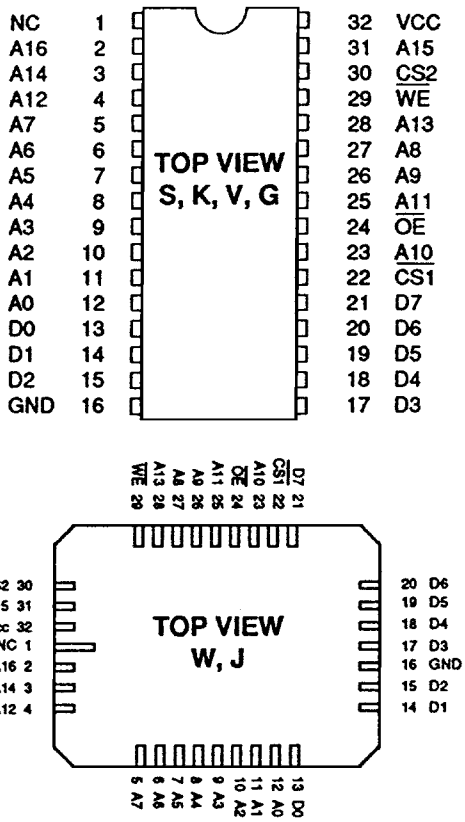
Features

Very Fast Access Times of 020/025/35 ns
JEDEC Standard 32 pin DIL footprint
VIL™ High Density Package Available
Low Power Standby 1.5mW (typ.)
Low Power Operation 475mW(typ.)
Completely Static Operation
3.0V Battery Back-up Capability.
Directly TTL compatible
Common data inputs & outputs
May be processed in accordance with MIL-STD-883

Block Diagram



Pin Definition



Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.6" Dual-in-Line (DIP)	S	Ceramic	JEDEC
32	0.4" Dual-in-Line (DIP)	K	Ceramic	JEDEC
32	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
32	Bottom Brazed Flat Pack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	W	Ceramic	JEDEC PENDING
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	JEDEC PENDING

Package dimensions and outlines are displayed on pages 6&7.
VIL is a trademark of Mosaic Semiconductor, US patent No. D316251

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5 to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V_T can be -3.0V pulse of less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	6.5	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (8128I)
	T_{AM}	-55	-	125	°C (8128M, MB, MC)

Notes : (1) V_{IL} can be -3.0V pulse of less than 30ns.

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-5	-	5	µA
Output Leakage Current	$I_{I/O}$	Outputs disabled, $0V \le V_{OUT} \le V_{CC}$	-5	-	5	µA
Operating Supply Current	I_{CC}	$\overline{CS1}$=V_{IL}, $\overline{CS2}$=V_{IH}, V_{CC}=MAX, f=MAX=1/t_{RC}	-	105	155	mA
StandbySupply Current	I_{SB}	$\overline{CS1}$=V_{IH}, $\overline{CS2}$=V_{IL}, V_{CC}=MAX, f=MAX=1/t_{RC}	-	17	40	mA
	I_{SB1}	$\overline{CS1} \ge V_{CC}$-0.2V, $\overline{CS2} \le$ 0.2V, V_{CC}=MAX				
		$V_{IL} \le V_{SS}$ +0.2V, $V_{IH} \ge V_{CC}$ -0.2V; f=0	-	0.3	10	mA
"L" version	I_{SB2}	Same as above			5	mA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Note: Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

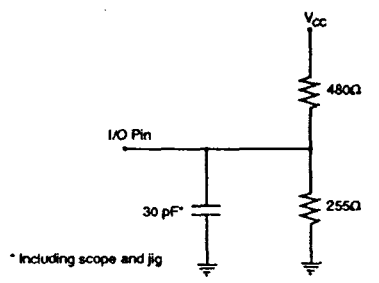
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
I/P Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{CC}=5V±10%

Output Load

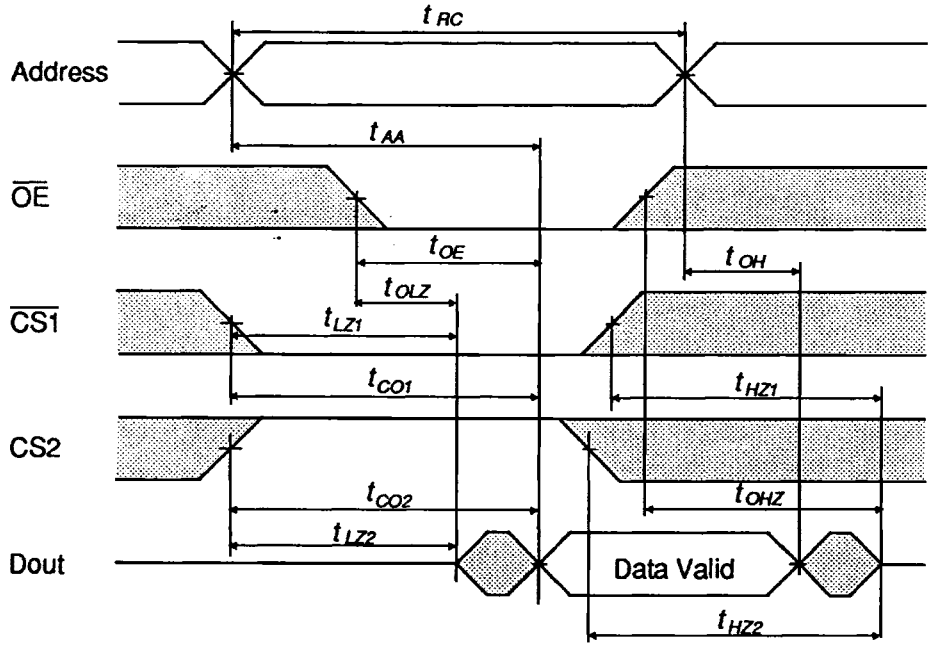


Electrical Characteristics & Recommended AC Operating Conditions

Read Cycle

Parameter	Symbol	-020 min	-020 max	-025 min	-025 max	-35 min	-35 max	Units
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Selection ($\overline{CS1}$) Access Time	t_{ACE1}	-	20	-	25	-	35	ns
Chip Selection ($\overline{CS2}$) Access Time	t_{ACE2}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	7	-	8	-	12	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection ($\overline{CS1}$) to O/P in Low Z[5]	t_{LZ1}	5	-	5	-	5	-	ns
Chip Selection ($\overline{CS2}$) to O/P in Low Z[5]	t_{LZ2}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselect ($\overline{CS1}$) to O/P in high Z[4,5]	t_{HZ1}	0	8	0	10	0	15	ns
Chip Deselect ($\overline{CS2}$) to O/P in high Z[4,5]	t_{HZ2}	0	8	0	10	0	15	ns
Output Disable to Output in High Z[4]	t_{OHZ}	0	6	-	10	-	12	ns

Read Cycle Timing Waveform [1]

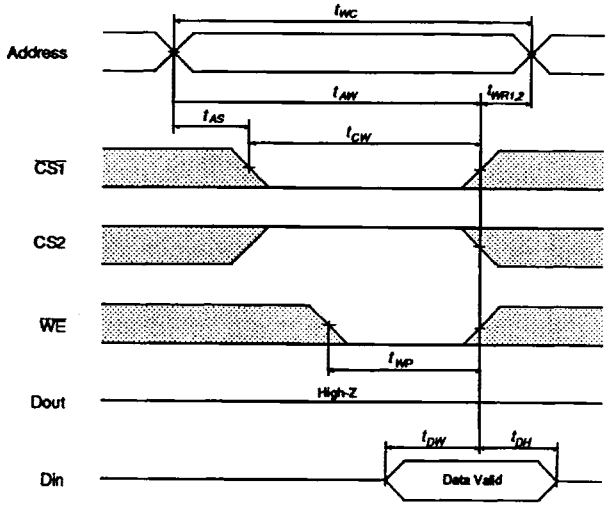


Notes:
(1) $\overline{WE}$ is High for Read Cycle.
(2) t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

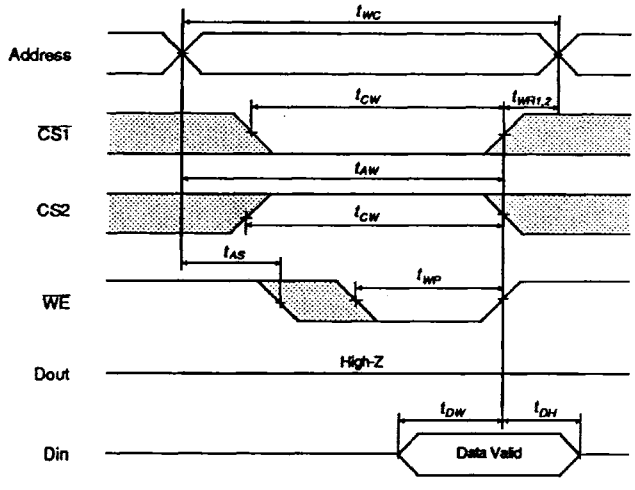
Write Cycle

Parameter	Symbol	-020 min	-020 max	-025 min	-025 max	-35 min	-35 max	Unit	Notes
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns	
Chip Selection to End of Write	t_{CW}	15	-	16	-	20	-	ns	
Address Valid to End of Write	t_{AW}	15	-	16	-	20	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	15	-	15	-	20	-	ns	
Write Recovery Time	t_{WR}	3	-	3	-	3	-	ns	
		5	-	5	-	5	-	ns	
Write to Output in High Z	t_{WHZ}	0	8	0	10	0	15	ns	(4,5)
Data to Write Time Overlap	t_{DW}	8	-	10	-	15	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns	

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



AC Characteristics Notes

Note: (1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

(2) $\overline{OE}$ is continuously high. ($\overline{OE}$=V_{IH})

(3) t_{WR} is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going high to the end of write cycle.

(4) Transition is measured ±500mV typical from steady state voltage, allowing for actual tester RC time constant.

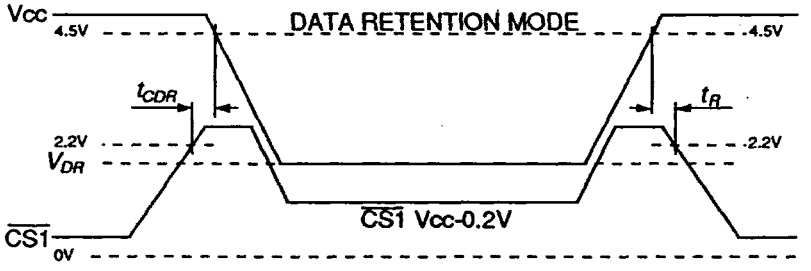
(5) At any given temperature and voltage condition, t_{HZ} is less than t_{LZ}, and t_{OHZ} is less than t_{OLZ}.

Low V_{CC} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

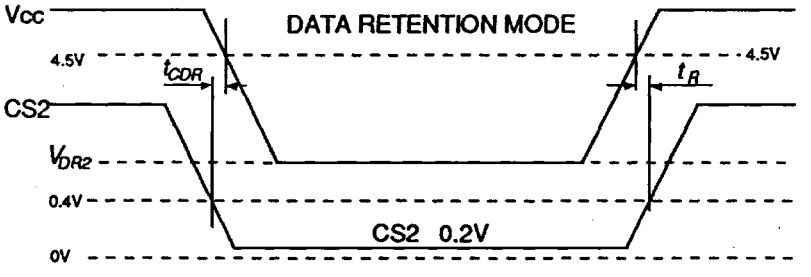
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$ ≥V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. V_{IN} ≥ 0V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, V_{IN} ≥ 0V, $\overline{CS1}$ ≥V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V.	-	-	1.5	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}	-	-	ms

Notes (1) CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer. If CS2 controls data retention mode, V_{IN} levels ($\overline{WE}$,$\overline{OE}$,$\overline{CS1}$,I/O) can be in the high impedance state. If $\overline{CS1}$ controls Data Retention mode, CS2 must be ≥ V_{CC} - 0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, $\overline{WE}$,$\overline{OE}$,I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform 1 ($\overline{CS1}$ controlled)

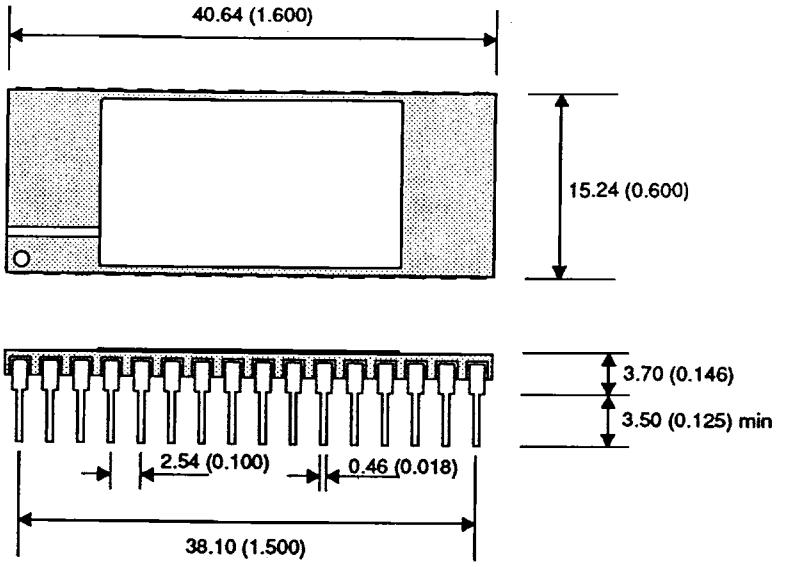


Low V_{CC} Data Retention Timing Waveform 2 (CS2 controlled)

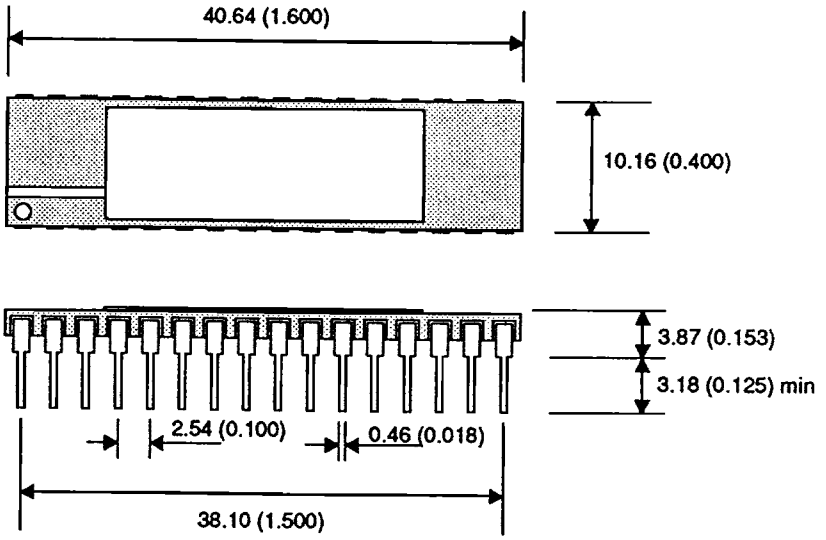


Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.01)

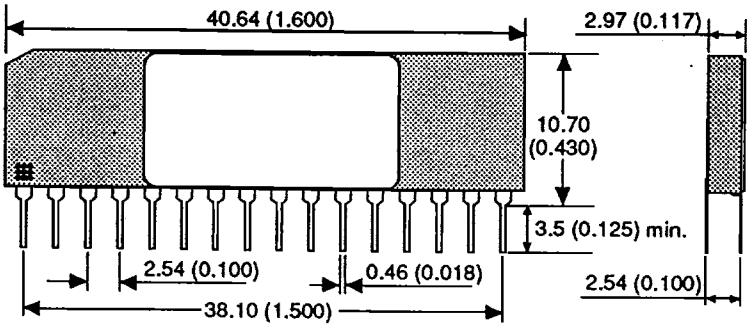
32 pin 0.6" Dual-in-Line (DIP) - 'S' Package



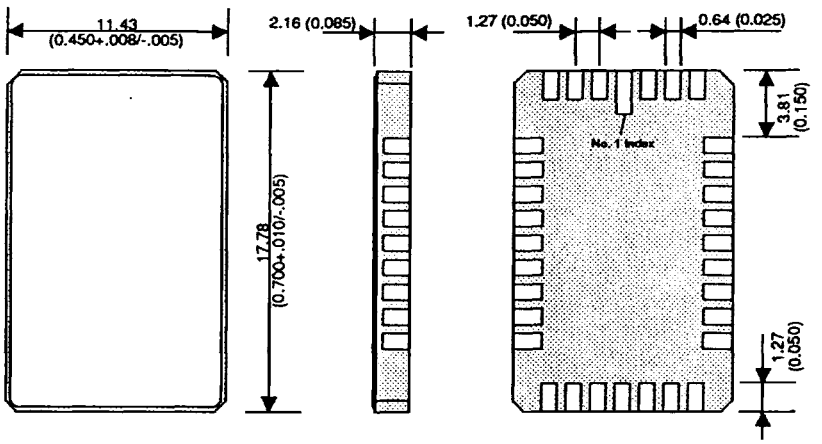
32 pin 0.4" Dual-in-Line (DIP) - 'K' Package



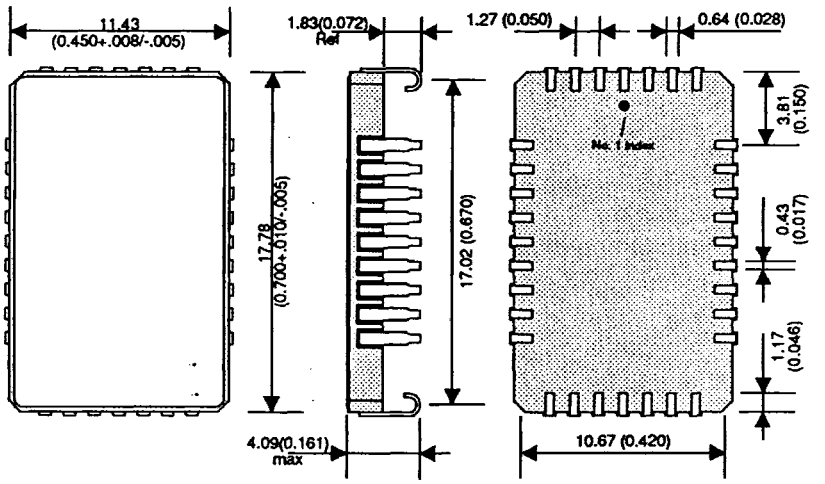
32 pin 0.1" Vertical-in-Line (VIL™) - 'V' Package



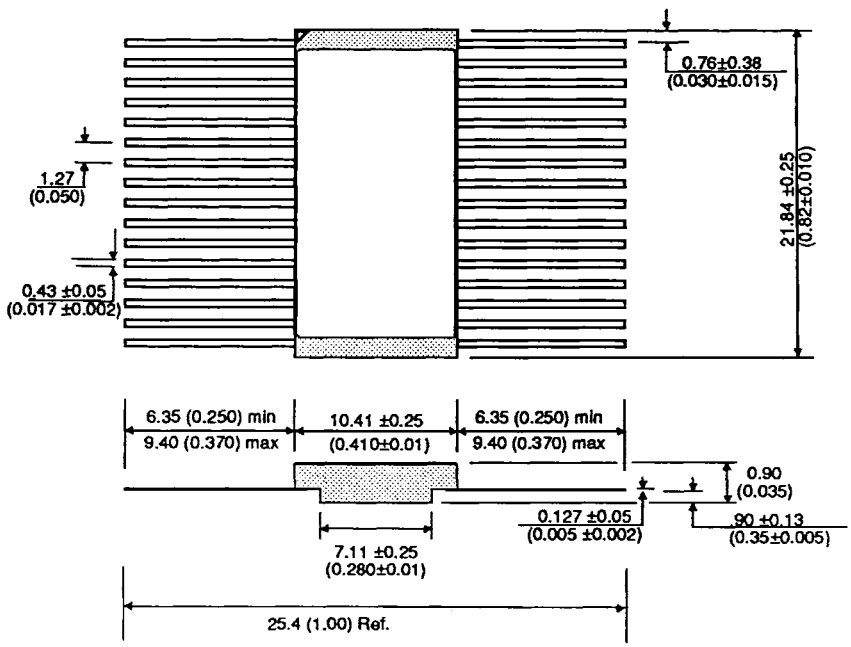
32 pin Extended Leadless Chip Carrier (LCC) - 'W' Package



32 pin Extended 'J' Leaded Chip Carrier (JLCC) - 'J' Package



32 pin Ceramic Flatpack - 'G' Package



Ordering Information

MSM8128SLMB-020

Speed	020	= 20 ns
	025	= 25 ns
	35	= 35 ns
Temp. range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Processed in accordance with MIL-STD-883, Method 5004 non-compliant.
	MC	= Compliant to MIL-STD-883
Power Consumption	Blank	= Standard Power
	L	= Low Power
Package	S	= 32 pin 0.6" DIP
	K	= 32 pin 0.4" DIP
	V	= 32 pin 0.1" VIL
	G	= 32 lead Flatpack
	W	= 32 pad LCC
	J	= 32 Extended JLCC

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

mosaic
Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058