M5M5278P,J-20,-25,-35,-25L,-35L
M5M5278FP-25,-35,-25L,-35L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5278 is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M5278P,J-20 ····· 20ns(max)
  M5M5278P,J,FP-25,-25L···· 25ns(max)
  M5M5278P,J,FP-35,-35L···· 35ns(max)
- Low power dissipation Active ····· 300mW(typ)
  Stand by(-20,-25,-35) ····· 5mW(typ)
  Stand by(-25L,-35L) ····· 50μW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select($\overline{S}$)input
- Output enable ($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

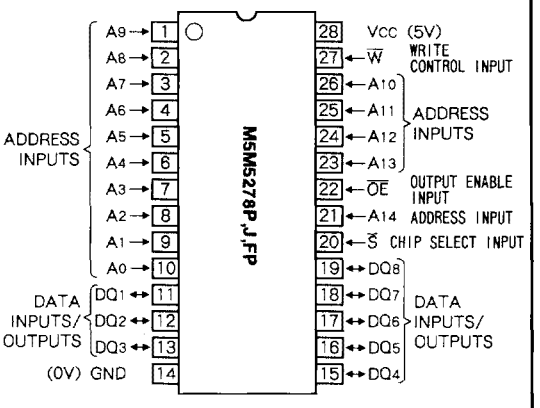
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)



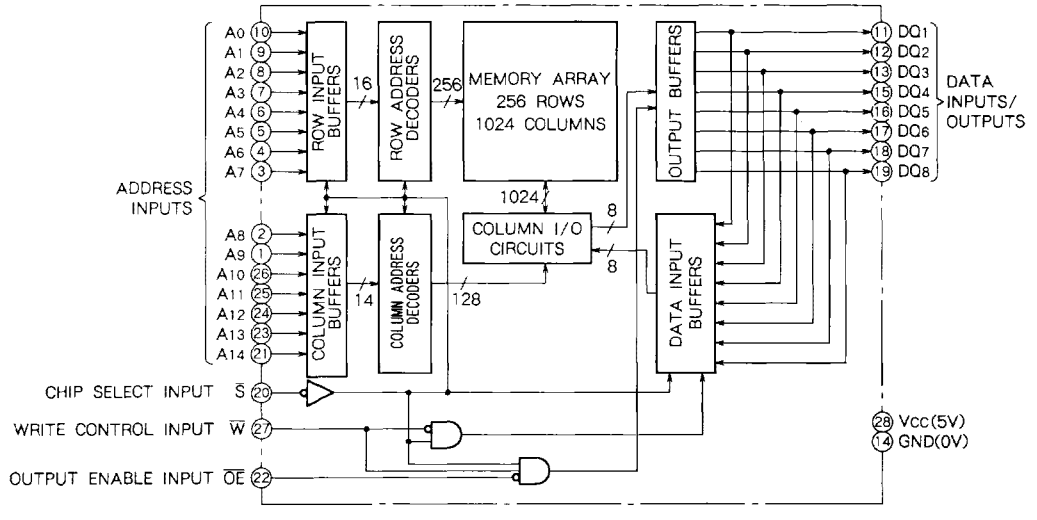
Outline 28P4Y(DIP)
28P0J(SOJ)
28P2W-C(SOP)

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating(high-impedance)state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M5M5278P,J-20,-25,-35,-25L,-35L
M5M5278FP-25,-35,-25L,-35L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input/output	Icc
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H : VIH L : VIL X : VIH or VIL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	− 3.5* ~7	V
VI	Input voltage		− 3.5* ~7	V
Vo	Output voltage		− 3.5* ~7	V
Pd	Maximum power dissipation		1	W
Topr	Operation temperature		0~70	℃
Tstg(bias)	Storage temperature(bias)		− 10~85	℃
Tstg	Storage temperature		− 65~150	℃

* Pulse width ≦ 20ns, In case of DC : − 0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
VIH	High-level input voltage			2.2		Vcc+0.3	V
VIL	Low-level input voltage			− 0.5*		0.8	V
VOH	High-level output voltage	IOH = − 4mA		2.4			V
VOL	Low-level output voltage	IOL = 8mA				0.4	V
II	Input current	VI = 0~Vcc				2	μA
| IOZ |	Off-state output current	VI(S) = VIH, Vo = 0~Vcc				10	μA
ICC1	Supply current from Vcc	VI(S) = VIL Output open	AC(20ns cycle)			140	mA
			AC(25ns cycle)			130	
			AC(35ns cycle)			120	
			DC		60	90	
ICC2	Stand by current	VI(S) = VIH	AC(20,25,35ns cycle)			40	mA
			Other VI≧VIH or ≦VIL			30	
ICC3	Stand by current	VI(S) = Vcc − 0.2V Other VI≦0.2V or VI≧Vcc − 0.2V	-20, -25, -35		1	10	mA
			-25L, -35L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* − 0.3V in case of AC (Pulse width ≦ 20ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
CI	Input capacitance	VI = GND, VI = 25mVrms, f = 1MHz			5	pF
Co	Output capacitance	Vo = GND, Vo = 25mVrms, f = 1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· VIH = 3V, VIL = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· VIH = 2.4V, VIL = 0.6V
Output timing reference levels ··· VOH = 2.0V, VOL = 0.8V
Output loads ····· Fig.1, Fig.2

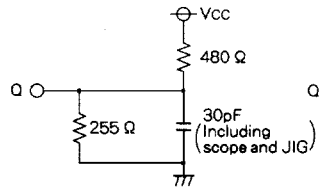


Fig.1 Output load

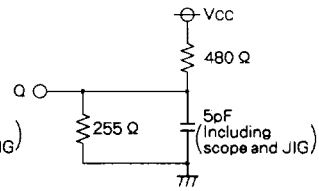


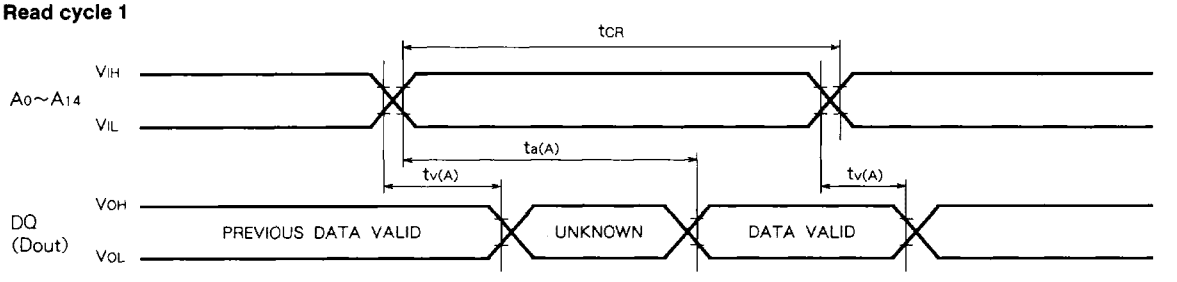
Fig. 2 Output load for ten, tdis

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5278-20		M5M5278-25, -25L		M5M5278-35, -35L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	20		25		35		ns
$t_{a(A)}$	Address access time		20		25		35	ns
$t_{a(S)}$	Chip select access time		20		25		35	ns
$t_{a(OE)}$	Output enable access time		10		12		15	ns
$t_{v(A)}$	Data valid time after address change	3		5		5		ns
$t_{en(S)}$	Chip selection to output active($\overline{S}$)	3		5		5		ns
$t_{en(OE)}$	Chip selection to output active($\overline{OE}$)	0		0		0		ns
$t_{dis(S)}$	Output disable time from($\overline{S}$)	0	8	0	10	0	10	ns
$t_{dis(OE)}$	Output disable time from($\overline{OE}$)	0	8	0	10	0	10	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		20		25		35	ns

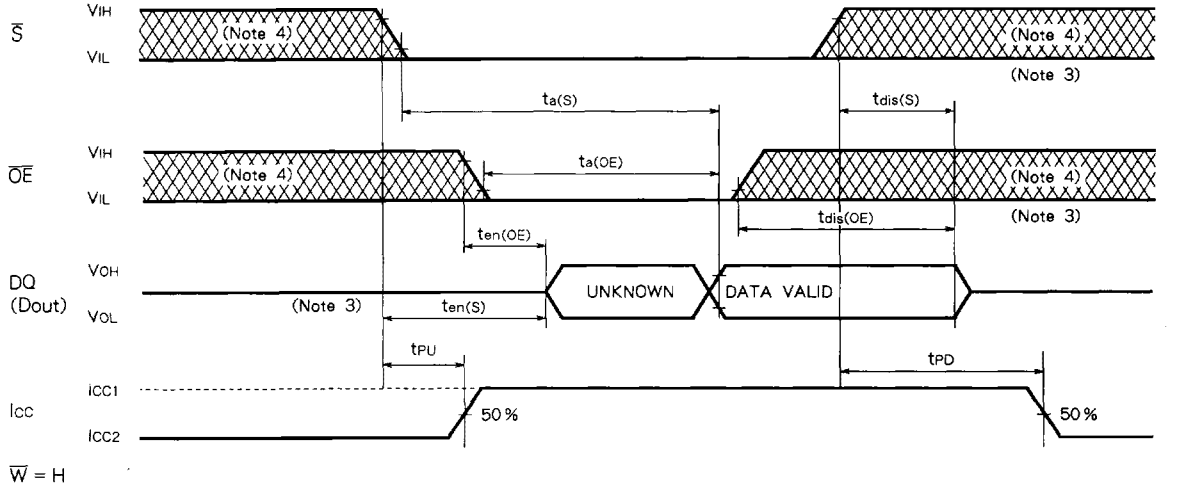
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{W}$ = H $\overline{S}$ = L $\overline{OE}$ = L

Read cycle 2 (Note 2)



$\overline{W}$ = H

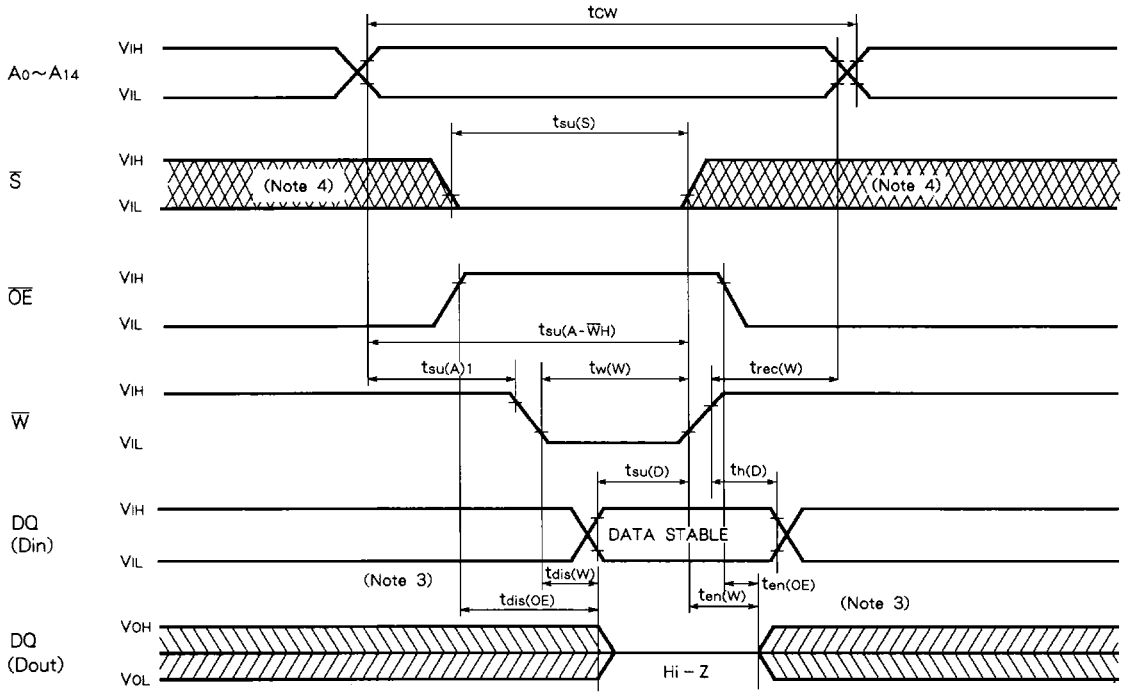
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure2.
4. Hatching indicates the state is don't care.

(4) WRITE CYCLE

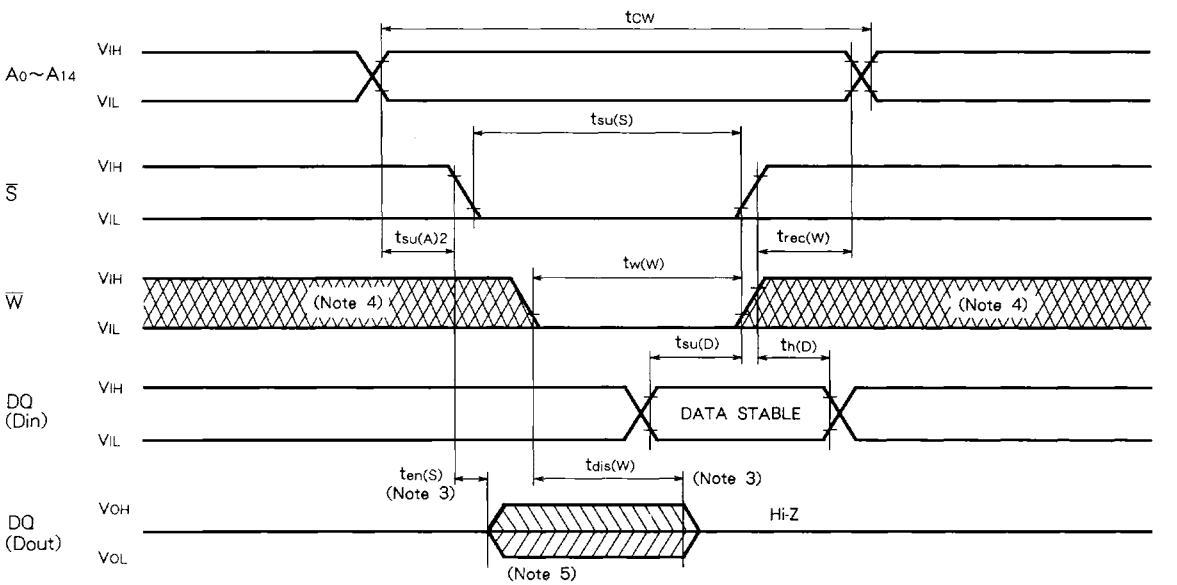
Symbol	Parameter	Limits						Unit
		M5M5278-20		M5M5278-25, -25L		M5M5278-35, -35L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	20		25		35		ns
$t_{su(S)}$	Chip select setup time	15		20		30		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S}$)	0		0		0		ns
$t_{w(W)}$	Write pulse width	15		20		25		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	8		10		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$	0	8	0	10	0	10	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$	0	8	0	10	0	10	ns
$t_{en(W)}$	Output enable time from $\overline{W}$	0		0		0		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	15		20		30		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 5. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.

POWER DOWN CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geq V_{CC} - 0.2V$ $V_I \geq V_{CC} - 0.2V$ or $0V \leq V_I \leq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time			0			ns
$t_{rec(PD)}$	Power down recovery time		-25L	25			ns
			-35L	35			
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3.0V				50	μA
		V_{CC} = 5.5V				100	

Note 6. This is only M5M5278P, J, FP-25L, -35L.

TIMING WAVEFORM FOR POWER DOWN