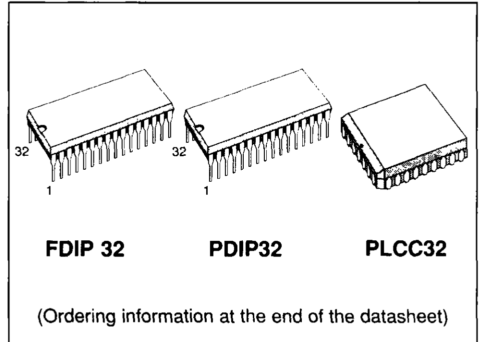
256K (32 x 8) CMOS FLASH MEMORY

ADVANCE DATA

- FLASH ELECTRICAL CHIP ERASE IN 1 SECOND RANGE.
- PRESTO F PROGRAMMING TYPICAL BYTE PROGRAM TIME : 100 µs.
- 12 V VPP SUPPLY.
- 100 TO 10.000 ERASE/PROGRAM CYCLES.
- VERY FAST ACCESS TIME : 100 ns.
- LOW POWER CONSUMPTION : Maximum standby current : 100 µA.
- COMMAND REGISTER ARCHITECTURE FOR MICROPROCESSOR / MICROCONTROLLER COMPATIBLE WRITE INTERFACE.
- JEDEC STANDARD BYTE-WIDE EPROM PINOUTS.



(Ordering information at the end of the datasheet)

DESCRIPTION

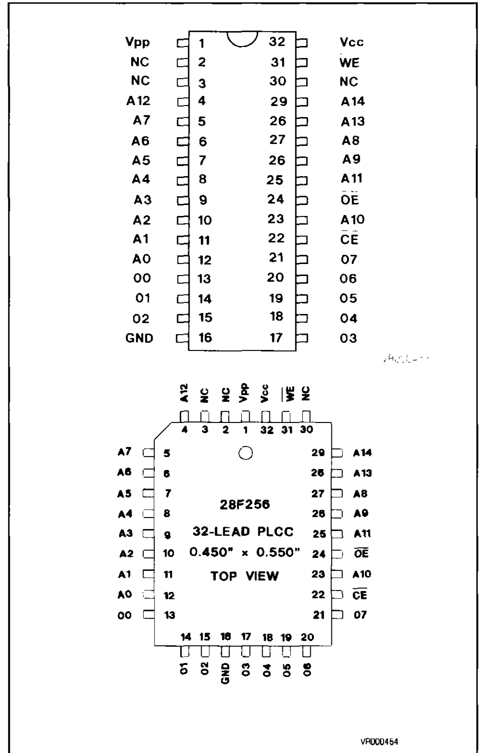
SGS-THOMSON Microelectronics M28F256 FLASH Memory is an Electrically Chip-erasable and Reprogrammable non-volatile memory. Higher functionality and flexibility than EPROM come from the ability to be Chip-erased and reprogrammed in a test socket, in a PROM programmer socket, on board, or In-system. The M28F256 is suitable for applications where EEPROM functionality is not suitable or not cost effective, or for replacement of UV EPROM when UV erasure is impractical or time consuming. Pin assignment conforms to JEDEC standards for byte wide EPROMs. The High performance access time allows interface with most microcontrollers and microprocessors.

PIN NAMES

A0-A14	ADDRESS INPUT
O0-O7	DATA INPUT/OUTPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{PP}	ERASE/PROGRAM power supply
V_{CC}	5V ± 10 % POWER SUPPLY
GND	GROUND
NC (1)	NO INTERNAL CONNECTION

(1) Pin may be driven or left floating.

Figure 1: Pin Configuration



This is advance information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2 : M28F256 Block Diagram

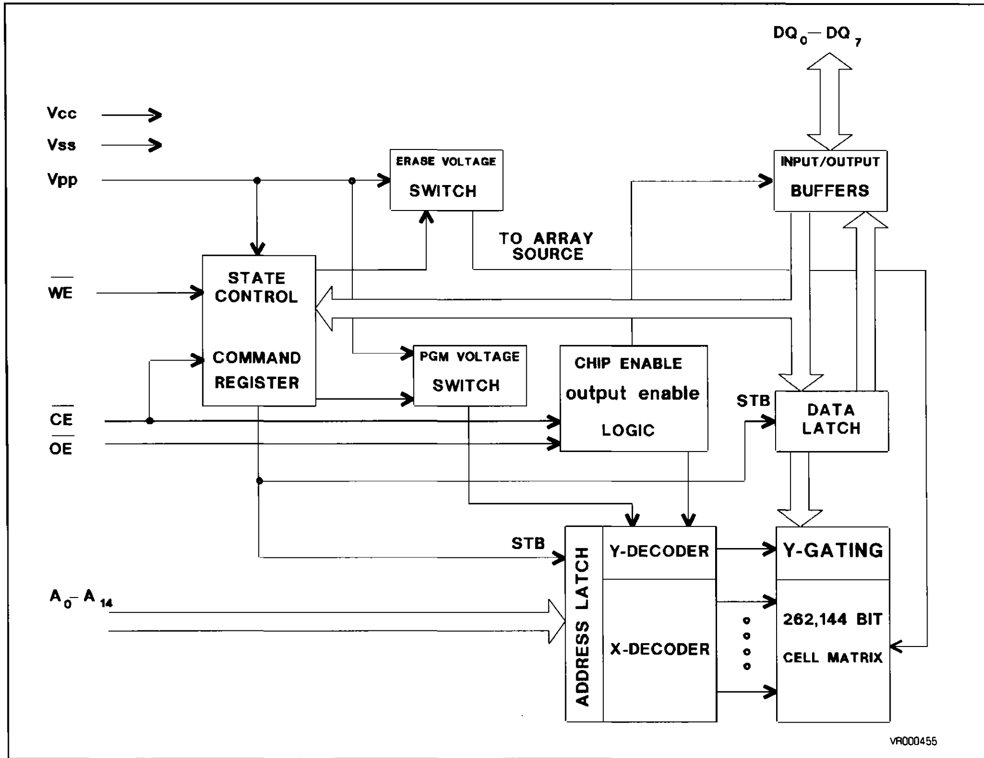


Table 3 : Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	Input or Output voltages with respect to ground	-0.6 to 7.0	V
V_{PP}	Supply voltage with respect to ground	-0.6 to 14	V
VA9	Voltage on A9 with respect to ground	-0.6 to 13.5	V
V_{CC}	Supply voltage with respect to ground	-0.6 to 7.0	V
T_{bias}	Temperature Range under Bias	-10 to 80	°C
T_{stg}	Storage temperature range	-65 to 125	°C
TR_{op}	Operating Temperature during Read	0 to 70	°C
TEP_{op}	Operating Temperature during Erase / Program	0 to 70	°C

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4 : Bus Operation

PINS / OPERATIONS		V_{PP} (1)	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	O0-O7
READ ONLY	READ	V_{PPL}	A0	A9	V_{IL}	V_{IL}	V_{IH}	DATA OUT
	OUTPUT DISABLE	V_{PPL}	X (7)	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY	V_{PPL}	X	X	V_{IH}	X	X	TRI STATE
	MANUFACTURER SIGNATURE (2)	V_{PPL}	VIL	V_{SI} (3)	V_{IL}	V_{IL}	V_{IH}	DATA = 20
	DEVICE SIGNATURE (2)	V_{PPL}	V_{IH}	V_{SI}	V_{IL}	V_{IL}	V_{IH}	DATA = A1 OR A8
READ/ WRITE	READ	V_{PPH}	A0	A9	VIL	V_{IL}	V_{IH}	DATA OUT (4)
	OUTPUT DISABLE	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	TRI STATE
	STANDBY (5)	V_{PPH}	X	X	V_{IH}	X	X	TRI STATE
	WRITE	V_{PPH}	A0	A9	V_{IL}	V_{IH}	V_{IL}	DATA IN (6)

Notes :
(1) V_{PP} Low may be ground, a no connect with a resistor tied to ground, or < 8 volts. V_{PP} High is the programming voltage specified for the device. When $V_{PP} = V_{PPL}$ memory content can be read but not written or erased.
(2) Manufacturer and Device electronic Signature can be accessed also through Command Register (see table 5) Device code A8 requires $V_{PPH} = 12V \pm 5\%$. Device code A1 requires $V_{PPH} = 12.75V \pm 0.25V$. All other addresses low.
(3) $11.5V < V_{SI} < 13V$.
(4) When $V_{PP} = V_{PPH}$ read operation can be array data or Electronic Signature.
(5) When $V_{PP} = V_{PPH}$ Standby current is $I_{CC} + I_{PP}$ (Standby).
(6) Refer to table 5 for Data In during write.
(7) X can be V_{IL} or V_{IH}.

DEVICE OPERATION

PRINCIPLE

The added functionality of FLASH as compared to EPROM, is Electrical Erasure and Reprogramming. In order to manage this new functionality a command register is introduced. Some device functions are addressed via the command register, some not, depending on the V_{PP} pin voltage. When V_{PP} pin is at low voltage (< 8V), the M28F256 is a READ only memory. The command register is disabled. Manipulations of the external memory control pins yield the standard EPROM read, output disable, electronic signature and standby operations. Raising V_{PP} pin to High voltage, enables the command register for READ/WRITE operations. In addition, read, output disable, standby, electronic signature, ERASE and WRITE operations are allowed. At $V_{PP} = V_{PPH}$ the operating modes are addressed through the use of the command register.

Table 4 summarizes the Bus operations : at $V_{PP}=V_{PPL}$ only Read operations are allowed, at $V_{PP}=V_{PPH}$ Read operations and Erase/Write operations are allowed.

OPERATION MODES DESCRIPTION

A- OPERATION MODES WITH V_{PP} AT LOW VOLTAGE (< 8V)

READ MODE

The M28F256 has two control pins, both of which must be logically active in order to obtain data at the outputs.

Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Fig 7 illustrates read timing waveforms.

STANDBY MODE

The M28F256 has a standby mode which reduces the maximum active current from 30mA to 0.1mA. The device is placed in Standby mode by applying a high signal to the $\overline{CE}$ input. When in Standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input .

OUTPUT DISABLE

With $\overline{OE}$ at High level V_{IH}, output pins are placed in a high impedance state.

ELECTRONIC SIGNATURE

The Electronic Signature mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for use by programming equipment

to automatically match the device to be programmed or erased with its corresponding programming or erasing algorithm. This mode is activated by applying high voltage on address line A9 (11.5V - 13V) and by applying V_{IL} to $\overline{CE}$ and $\overline{OE}$. Two identifier bytes may then be sequenced from the outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode.

Byte 0 (A0=V_{IL}) represents the manufacturer code and byte 1 (A0=V_{IH}) represents the device identifier code. For the SGS-THOMSON Microelectronics M28F256, these two identifiers are given here below and can be read on outputs O0 to O7.

WRITE MODE

When V_{PP} is at low voltage, memory contents can not be written or erased. Write/Erased operations can only be accomplished via the command register when V_{PPH} is applied on V_{PP} pin.

ELECTRONIC SIGNATURE

IDENTIFIER	PINS									
	A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX
MANUFACTURER CODE	V_{IL}	0	0	1	0	0	0	0	0	20
DEVICE IDENTIFIER	V_{IH}	1	0	1	0	0	0	0	1	A1
	V_{IH}	1	0	1	0	1	0	0	0	A8

Notes : (1) A9 = 12.0V ± 0.5V ; $\overline{CE}$ = $\overline{OE}$ = V_{IL} ; V_{PP} = V_{PPL} ; A1 to A8= V_{IL} ; A10 to A14 = V_{IL}.
(2) Device code is either A8 if device requires V_{PP} = 12V ± 5% or A1 if device requires V_{PP} = 12.75V ± 0.25V.

Table 5 : COMMAND DEFINITIONS

COMMAND	BUS CYCLES REQ'D	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Operation (1)	Address (2)	Data (3)	Operation (1)	Address (2)	Data (3)
Read Memory	1	Write	X	00H			
Read Electronic Signature (4)	1	Write	X	90H	Read	IA	ID
Setup Erase/Erase (5)	2	Write	X	20H	Write	X	20H
Erase Verify (5)	2	Write	EA	A0H	Read	X	EVD
Setup program/Program (6)	2	Write	X	40H	Write	PA	PD
Program verify (6)	2	Write	X	C0H	Read	X	PVD
Reset (7)	2	Write	X	FFH	Write	X	FFH

Notes: (1) Bus operations are defined in table 4.
(2) IA = identifier address ; 0000H for manufacturer code and 0001H for device.
(3) EA = address of memory location to be read during erase verify.
PA = address of memory location to be programmed.
(4) ID = data read from location IA during electronic signature ; 20H = manuf ; A1H or A8H = device.
PD = data to be programmed at location PA. EVD = data read during from location EA during erase verify.
PVD Data read from location PA during program verify.
(5) See fig. 6 for erase algorithm.
(6) See fig. 4 for programming algorithm.
(7) The second bus cycle must be followed by the desired command register write.

B - OPERATION MODES WITH V_{PP} AT V_{PPH} - COMMAND REGISTER

At V_{PP} = V_{PPH}, Read/Write operations are enabled. Device operations are selected by writing specific data patterns into the command register using standard microprocessor write timings. The register contents are inputs for an internal state machine which controls erase and programming circuitry. Some commands require one write cycle, while others require two. The register is a latch used to store these commands and the data and address needed to execute the command.

(Note that the command register does not occupy an addressable memory location).

With this architecture, the device expects the first write cycle to be a command and does not corrupt data at specified address. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is low. Addresses are latched on the falling edge of $\overline{WE}$, while data are latched on the rising edge of $\overline{WE}$ pulse. Table 5 contains the list of register commands. The three high order register bits R7, R6 and R5 encode the control function. All other register bits R4-R0 must be at zero. Only exception is the reset command, when FFH is written into the command register. Register bits R7-R0 correspond to data inputs D7-D0. Note that when V_{PP} is at low voltage, the contents of the command register default to 00H enabling Read-Only operations. The command register is only alterable when V_{PP} is at high voltage. The system designer may choose to make the V_{PP} switchable or to make the V_{PP} constantly available. In the case of switchable V_{PP}, when V_{PP} is removed, the device defaults to Read Only memory. In the case of constantly available V_{PP}, all memory functions are performed via the command register.

READ MODE WITH V_{PP} = V_{PPH}

At V_{PP} = V_{PPH}, memory contents can be addressed via the read command 00H. Read mode is initiated by writing 00H into the command register. The microprocessor read cycles retrieve the array data. The device remains enabled for read operations until the command register contents are altered. The default contents of the command register upon power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. When V_{PP} is "Hardwired", the device powers-up and remains enabled for read operations until the command register contents are changed.

Refer to AC Read characteristics and waveforms for timing parameters (Fig 7,Table 9).

ELECTRONIC SIGNATURE WITH V_{PP} = V_{PPH}

In order for the M28F256 to be erased and programmed by the local CPU and thus to supplement the traditional PROM programming methodology, the manufacturer and device signature codes can be read via the command register. The operation is initiated by writing 90H to the register. Following the command write, a read cycle from address 0000H returns the manufacturer code of 20H. A read cycle from address 0001H returns the device code of A1 or A8. To terminate the operation, it is necessary to write another valid command into the register.

SET UP ERASE/ERASE MODE

Before erasure it is necessary to program all bytes to the same level (data 00H). Setup erase is a command-only operation that prepares the device for electrical erasure of all bytes in the array. The setup erase is performed by writing 20H to the command register. To begin chip erasure, the erase command (20H) must again be written to the register. The erase operation begins on the second command's rising edge of the $\overline{WE}$ pulse and terminates with the rising edge of the next $\overline{WE}$ pulse (i.e Erase Verify command). This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased. Refer to A.C Erase characteristics and waveforms for timing parameters (Fig 6, Fig 5, Table 10).

ERASE VERIFY MODE

The erase command erases all the bytes of the array in parallel. After each erase operation, all bytes must be verified to see if they are erased. The erase verify operation is initiated by writing A0H to the command register. The address of the byte to be verified must be supplied because the device latches this address on the falling edge of the $\overline{WE}$ and the actual command on the rising edge. The register write with the erase verify command terminates the erase operation. The device applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all the bits of the byte are erased. If the location is erased the erase verify operation is repeated for the next location. The command must be written before each byte verification to latch the byte address.This process continues for each byte of the array until a byte does not return FFH or the last address is accessed.

In the case where the data returned is not FFH , another setup Erase/Erase operation is performed. The verification starts then from the address of the last verified byte. Once the last address is accessed, erasure is complete and the erase verify is terminated by writing a valid command to the command register. See Fig.6, 6bis for Erase algorithm, Fig.5 for waveforms and Table 10 for erase timings.

SET UP PROGRAM/PROGRAM

Writing 40H to the command register performs the setup operation. The next WE pulse operation causes a transition to an active programming operation. The device latches address and data on the falling and rising edge of WE pulse respectively. The rising edge of this second WE pulse also begins programming operation. The programming operation is stopped on the next rising edge of WE used to write the program verify command into the command register. See A.C programming characteristics and waveforms for programming timings (Fig 4 ,Table 10).

PROGRAM VERIFY MODE

Flash memory device programs on a byte by byte basis. After each programming operation, the byte just programmed must be verified. The program verify command (C0H) stops programming and sets up verification. The device executes the command on the rising edge of WE. The program verify command prepares the device for verification of the byte last programmed. No new address information is latched. The device applies an internally generated margin voltage to the byte. After a 6µs delay the data is read at the address programmed and compared to the programmed data. Reading valid data indicates that the byte programmed successfully. See Fig.4 for programming algorithm, Fig.3 for waveforms and Table 10 for programming timings.

COMMAND REGISTER RESET

This command is used to safely abort erase- and program-command sequences. The reset operation is performed by writing twice the code FFH to the command register. The memory content is not altered. A valid command must be written to place the device in the desired state.

STANDBY MODE

If during Erasure, Programming, or Program/Erase verification, the device is deselected, it draws active current until operation is terminated.

PRESTO F PROGRAMMING ALGORITHM

Programming with PRESTO F consists in applying a sequence of 100 µs program pulses to each byte until a correct verify occurs. 25 programming operations are allowed for each byte. Each programming operation consists in a set-up program command through the command register (code 40H) ; the programming is then performed. Then a program verify command is written into the command register (code C0H) and read is performed which compares data output with data expected. During Programming and Verify operation a MARGIN MODE circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. Figure 4 illustrates the PRESTO F programming algorithm.

PRESTO F ERASE ALGORITHM

Erasing with PRESTO F erase algorithm allows to erase electrically the entire memory in a reliable way. The algorithm starts by first programming all the bytes to 00H in order to perform an uniform erasure. This step is accomplished by using the PRESTO F Programming algorithm. All bytes being in the same state (00H), a set-up erase command is written into the command register (code 20H) followed by the erase command (code 20H). Erase is then performed. Erase verify command is written to the command register (code A0H), and data of the address to be verified is compared to FFH. The erase verify begins at address 0000H and continues until the last address is accessed or until the comparison of data to FFH fails. The address of the last byte verified can be stored and a new erase operation is performed. The erase verify then starts from the stored address location or from address 0000H. Figure 6 illustrates the PRESTO F erase algorithm.

Table 6 : OPERATING CONDITIONS

Symbol	Parameters	Ranges	Units
TA	Operating Temperature READ only operations ERASE/WRITE operations	 0 to 70 0 to 70	 °C °C
V_{CC}	Supply Voltage	4.5 to 5.5	V

Table 7 : DC CHARACTERISTICS

Symbol	Parameters	Limits		Units	Test Condition
		min	max		
I_{LI}	Input Leakage current		±1	µA	V_{CC} = V_{CC}max Vin = 0 to V_{CC}
I_{LO}	Output Leakage current		±10	µA	V_{CC} = V_{CC}max Vout = 0 to V_{CC}
I_{CCS1}	V_{CC} standby current TTL		1	mA	V_{CC} = V_{CC}max $\overline{CE}$ = V_{IH}
I_{CCS2}	V_{CC} standby current CMOS		100	µA	V_{CC} = V_{CC}max $\overline{CE}$ = V_{CC} ±0.2V
I_{PPS}	V_{PP} Leakage current		±10	µA	V_{PP} = V_{PPL}
I_{CC1}	V_{CC} active read current		30	mA	V_{CC} = V_{CC}max $\overline{CE}$ = V_{IL} f = 5 MHz Iout = 0mA
I_{CC1}	V_{CC} active read current		50	mA	V_{CC} = V_{CC}max $\overline{CE}$ = V_{IL} f = 10 MHz Iout = 0mA
I_{CC2}	V_{CC} programming current		30	mA	Programming in progress
I_{CC3}	V_{CC} erase current		30	mA	Erasure in progress
I_{PP2}	V_{PP} programming current		30	mA	V_{PP} = V_{PPH} programming in progress
I_{PP3}	V_{PP} erase current		30	mA	V_{PP} = V_{PPH} erasure in progress
V_{IL}	Input low voltage	-0.5	0.8	V	
V_{IH}	Input high voltage TTL	2	V_{CC}+0.5	V	
	Input high voltage CMOS	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output low voltage		0.45	V	V_{CC} = V_{CC}min I_{OH} = 2.1 mA
V_{OH}	Output high voltage CMOS	4.1		V	V_{CC} = V_{CC}min I_{OH} = -100 µA
	Output high voltage TTL	V_{CC} -0.8		V	V_{CC} = V_{CC}min I_0 = -2,5 mA
V_{PPH}	V_{PP} during Write/Read operations	11.4 12.5	12.6 13	V	Code A1H V_{PP} > +12V device Code A8H V_{PP} =12.75V Device
V_{PPL}	V_{PP} during read only operations	0	8	V	
V_{PPDV}	V_{PPH} difference between Erase/Program and Verify		0.2	V	V_{PP} = 12V Device
V_{SI}	A9 electronic signature voltage	11.5	13	V	A9 = V_{SI}

Note : Operating temperature is for Commercial Range.

DESIGN CONSIDERATIONS

TWO LINE OUTPUT CONTROL

Because Flash memories are usually used in large memory arrays, the M28F256 features a 2 line control function which accommodates the use of multiple memory connections. The two line control function allows :

a)the lowest possible memory power dissipation,
b)complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, CE should be decoded and used as the primary device selecting function, while OE should be made a common connection to all devices in the array and connected to the read line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode .

POWER SUPPLY DECOUPLING

The power switching characteristics of the M28F256 require careful decoupling of the devices. Supply current I_{CC} has three segments that are of interest to the system designer : the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of CE. The magnitude of this transient current peak is dependent on capacitive and inductive loading of the device, at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and GND, and V_{PP} and GND. This should be a High frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be placed near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effect of the printed-circuit-board traces.

POWER UP/DOWN SEQUENCING

The M28F256 is designed to offer protection against accidental erasure and programming caused by spurious system level signals that may exist during power transitions. The M28F256 powers up in its read only mode. With its command register two step command sequences are necessary to alter memory contents. While these precautions are sufficient in most applications, it is recommended that V_{CC} reachs its steady-state value before raising V_{PP} above V_{CC}+2V. In addition upon power down V_{PP} should be below V_{CC} + 2 V, before lowering V_{CC}.

In addition, upon powering-down, V_{PP} should be below V_{CC}+2V before lowering V_{CC}.

Table 8 : CAPACITANCE TA = 25°C, f = 1 MHz

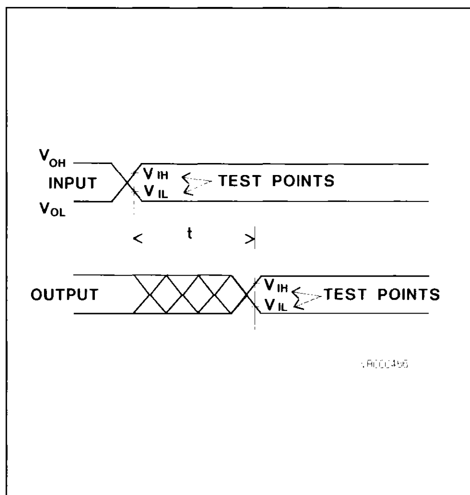
Symbol	Parameter	Test condition	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	12	pF

Note : (1) this parameter is only sampled and not 100% tested.

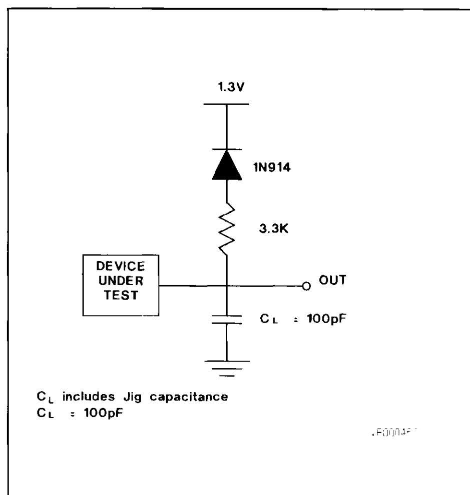
AC TEST CONDITIONS

Input Rise and Fall Times (10 % to 90 %)	10 ns
Input pulse Levels	V_{OH} and V_{OL}
Input timing reference Levels	V_{IL} and V_{IH}
Output timing Reference Levels	V_{IH} and V_{IL}

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. Testing : Inputs are driven at V_{OH} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

Table 9 : A.C CHARACTERISTICS Read Only Operations

Symbol	Characteristic	M28F256-100		M28F256-120		M28F256-150		M28F256-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{ACC}	Address to output delay		100		120		150		200	ns
T_{CE}	$\overline{CE}$ to output delay		100		120		150		200	ns
T_{OE}	$\overline{OE}$ to output delay		45		60		70		75	ns
T_{DF}	OE high to output float		30		30		35		45	ns
T_{OH}	Output hold from Address, $\overline{CE}$, or $\overline{OE}$ change (1)	0		0		0		0		ns
T_{WR}	Write recover time before read	6		6		6		6		µs
T_{CEL}	$\overline{CE}$ low to output in low Z	0		0		0		0		ns
T_{CDF}	$\overline{CE}$ high to output in high Z		40		40		55		60	ns
T_{OEL}	$\overline{OE}$ low to output in low Z	0		0		0		0		ns

(1) whichever occurs first.

Table 10 : A.C. CHARACTERISTICS Write/Erase/Program Operations (1)

Symbol	Characteristic	M28F256-100		M28F256-120		M28F256-150		M28F256-200		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{WC}	Write cycle time	100		120		150		200		ns
T_{AS}	Address setup time	0		0		0		0		ns
T_{AH}	Address hold time	40		50		60		75		ns
T_{DS}	Data setup time	50		50		50		50		ns
T_{DH}	Data hold time	10		10		10		10		ns
T_{WHGL}	Write recover time before read	6		6		6		6		µs
T_{GHWL}	Read recover time before write	0		0		0		0		µs
T_{CS}	$\overline{CE}$ setup time	20		20		20		20		ns
T_{CH}	$\overline{CE}$ hold time	0		0		0		0		ns
T_{WP}	Write pulse width	40		40		50		60		ns
T_{WPH}	Write pulse width high	40		40		50		60		ns
T_{WHWH1}	Duration of programming operation	95	150	95	150	95	150	95	150	µs
T_{WHWH2}	Duration of erase operation	9.5	10.5	9.5	10.5	9.5	10.5	9.5	10.5	ms
T_{VPEL}	V_{PP} setup to $\overline{CE}$ low	100		100		100		100		ns
T_{ELEH}	Alternate write pulse width	40		40		50		60		ns

Notes : (1) Refer to read timing table for read timing characteristics during Write/Read operations.

Figure 3 : A.C. Waveforms for Programming Operations

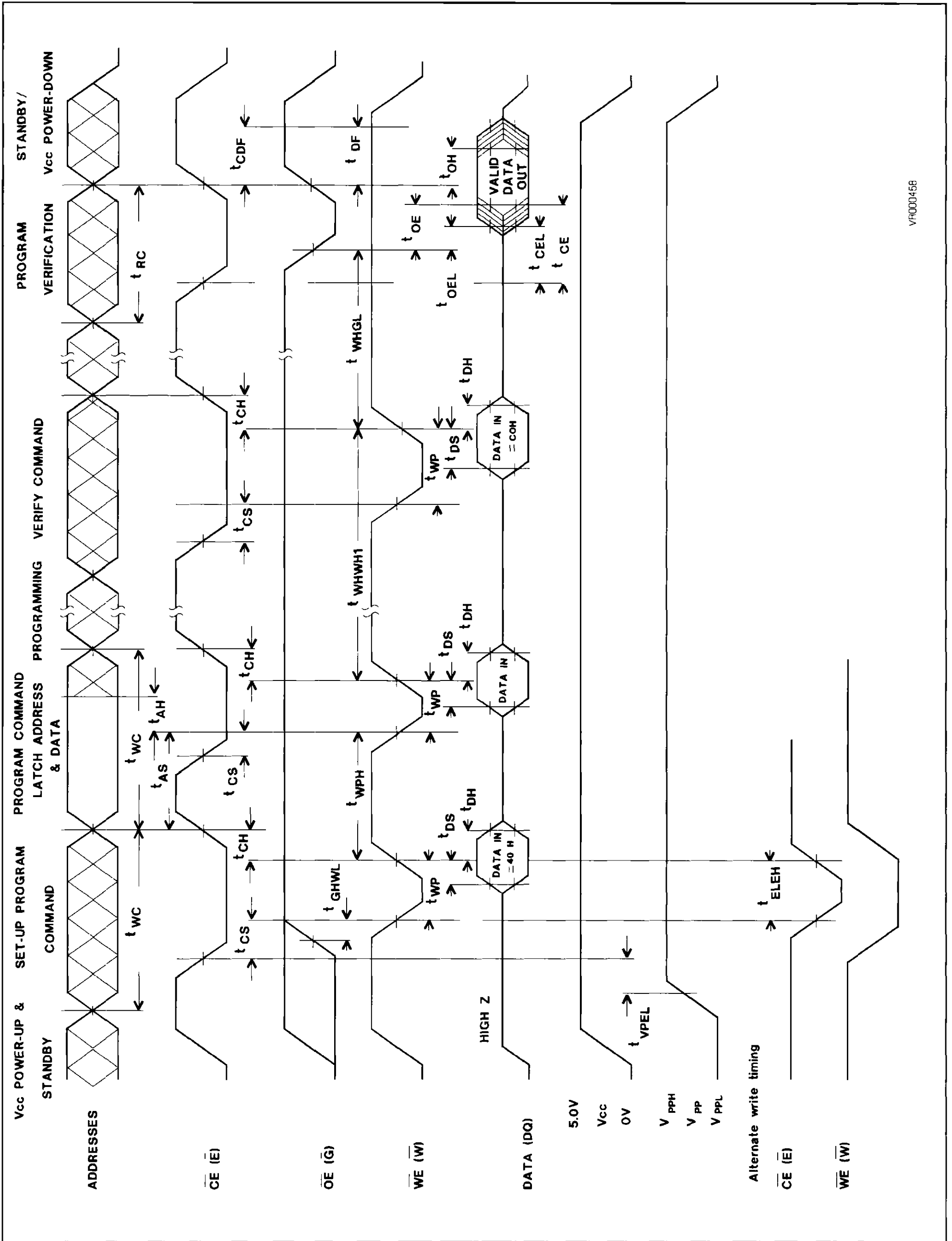
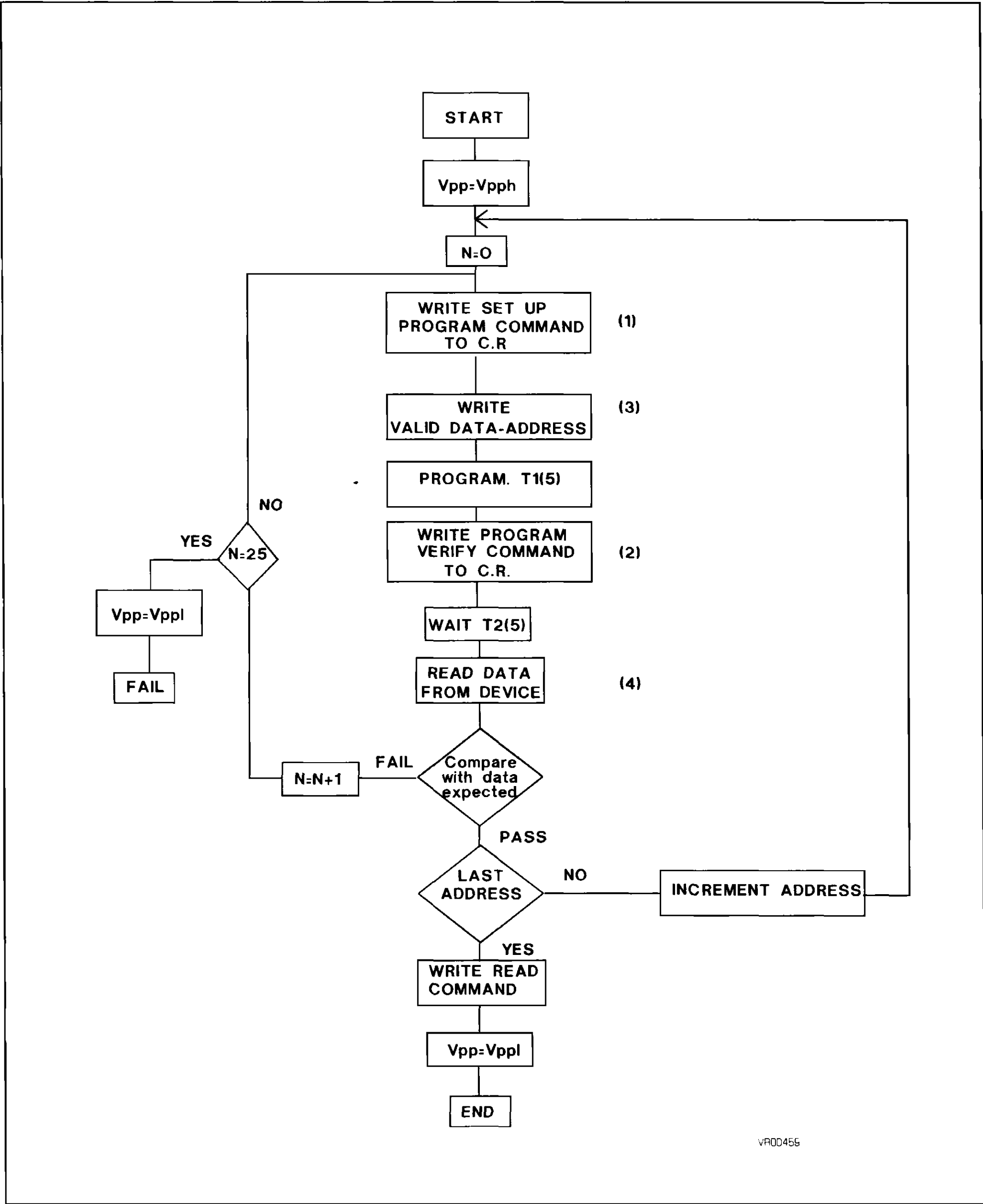


Figure 4 : Presto F Programming Algorithm



Notes :
(1) C.R. = Command Register.
(2) STOPS program generation - program verify command is only performed after byte programming.
(3) Second bus cycle of the setup Program/Program command (See Table 5 and Fig 4) starts programming operation.
(4) Second bus cycle of the program verify command (See Table 5 and Fig 4).
(5) T1 = 100µs, T2 = 6µs

Figure 5 : A.C. Waveforms for Erase Operations

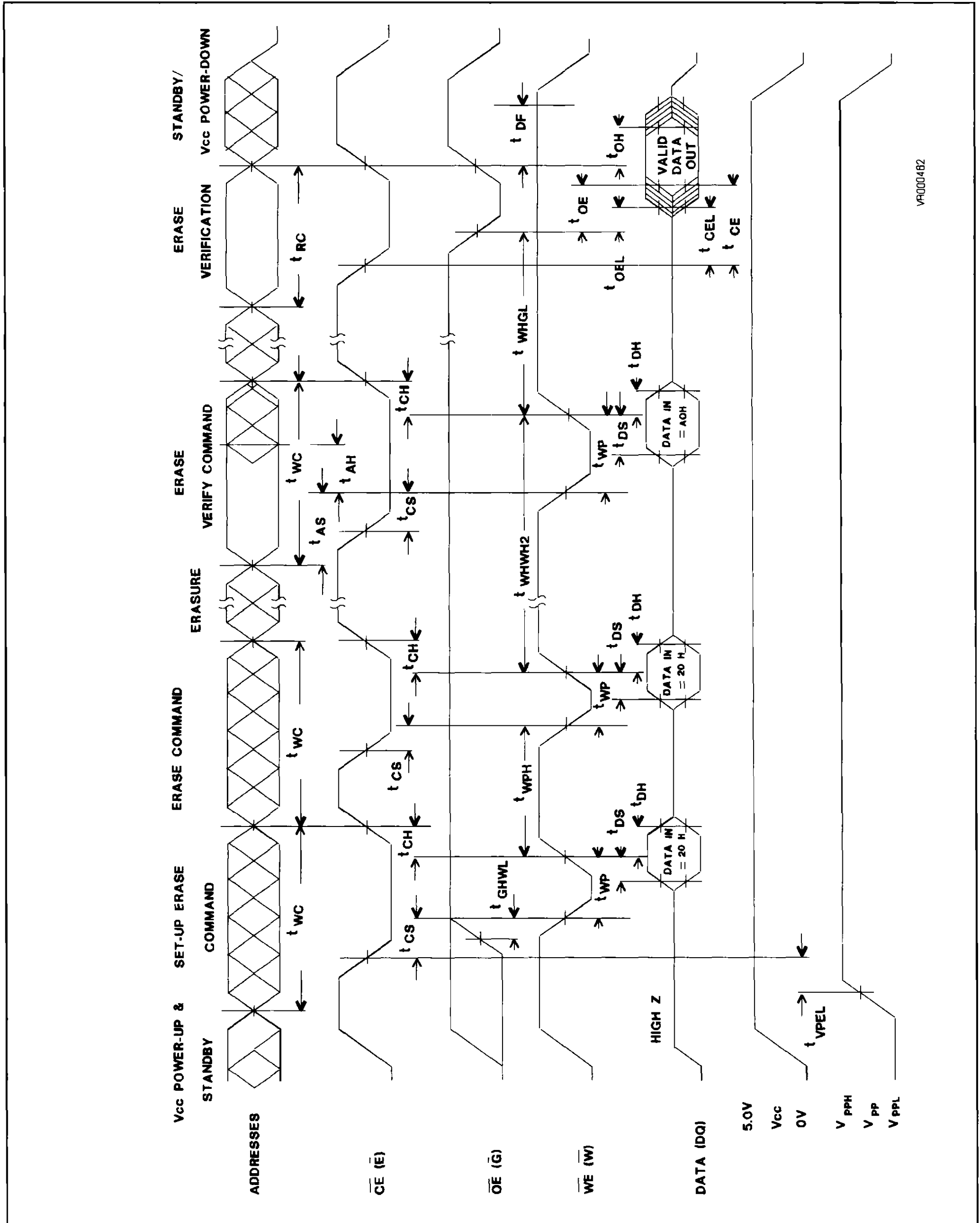
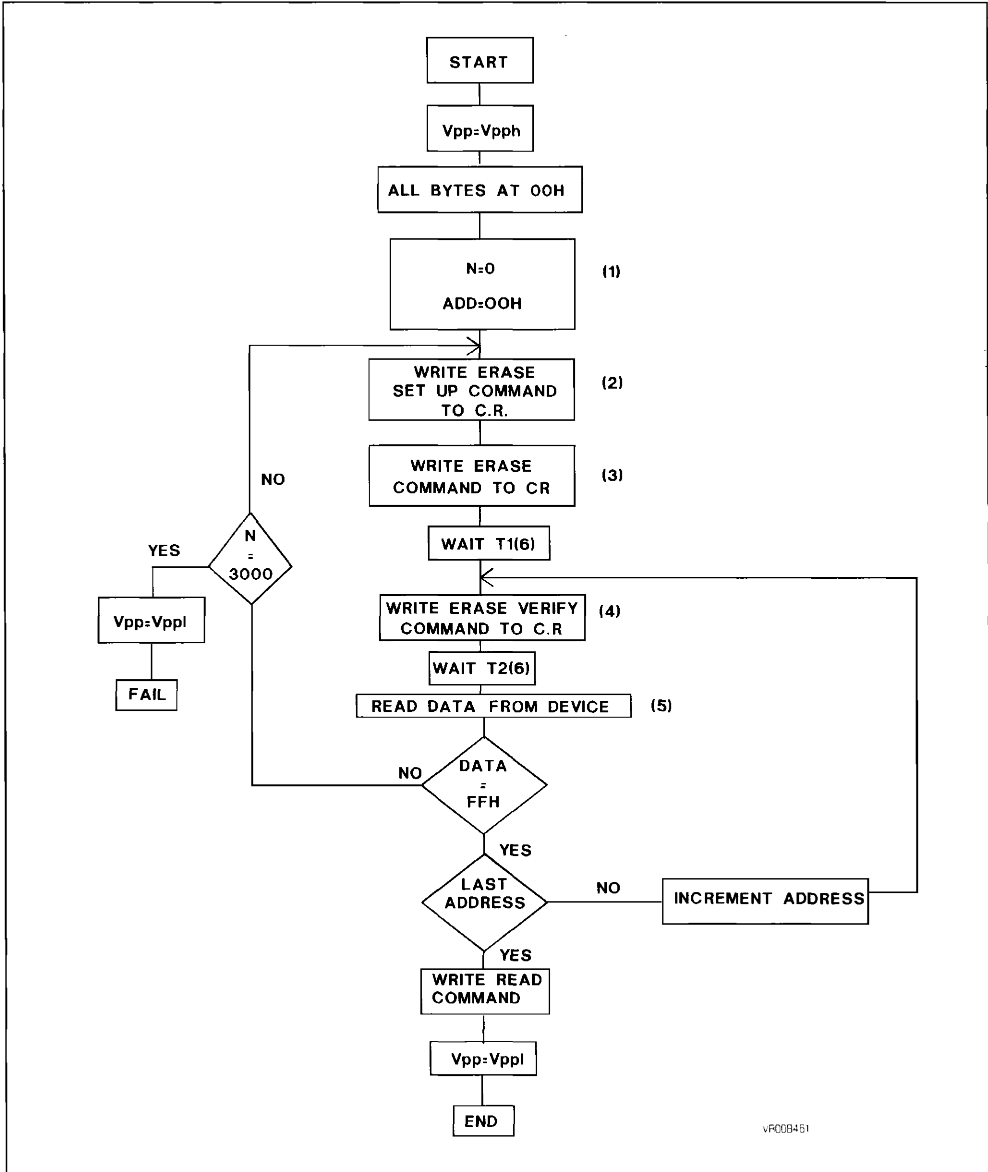
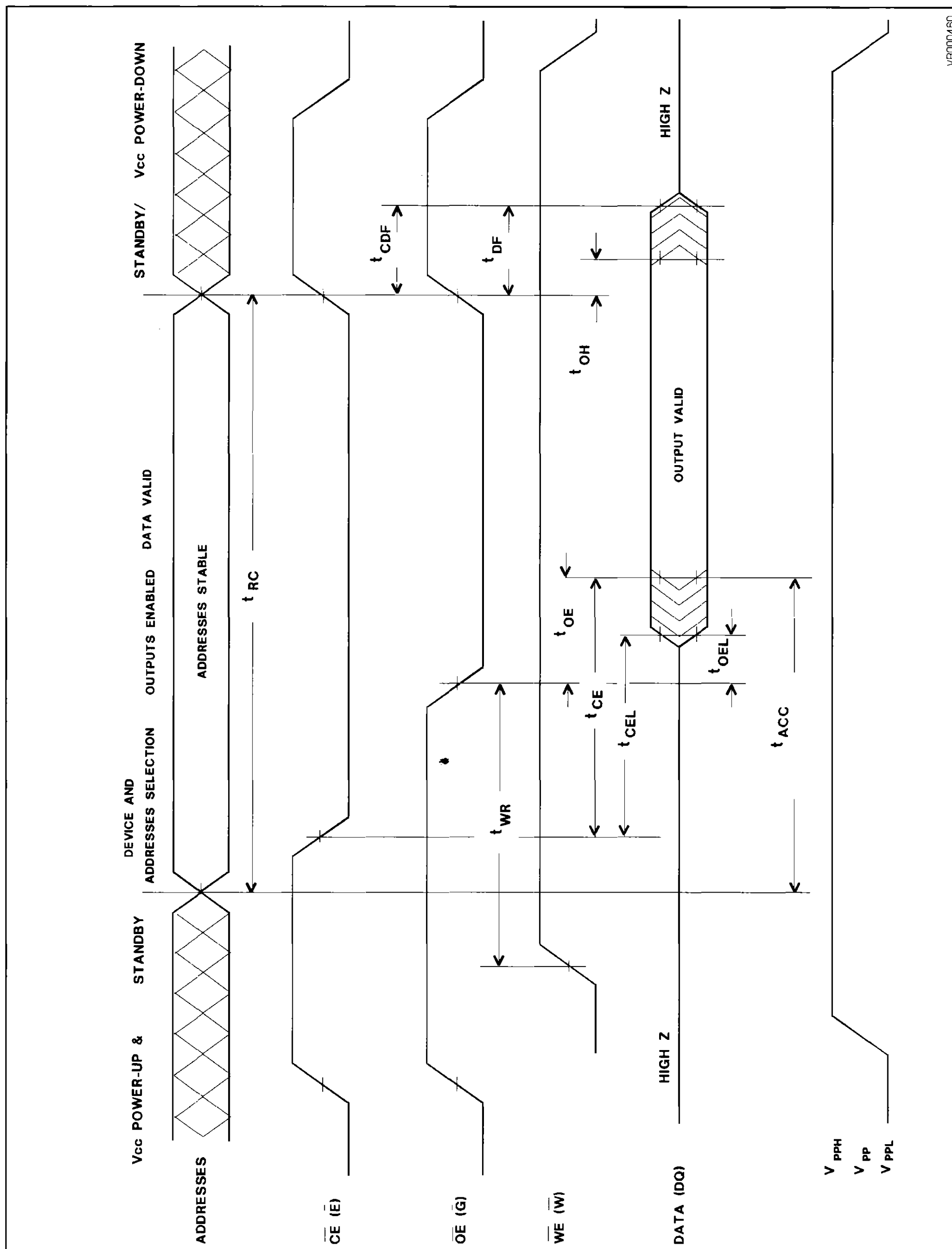


Figure 6 : Presto F Erase Algorithm



Notes :
- (1) N = Pulse Count.
- (2) CR = Command Register.
- (3) Second Bus Cycle of Setup Erase/Erase command (see Table 5 and Fig. 5).
- (4) Address = byte to verify. Erase verify is only performed after chip Erasure.
- (5) Second bus cycle of Erase verify command.
- (6) T1 = 10ms, T2 = 6µs.

Figure 7 : A.C. Waveforms for Read Operations



PACKAGE MECHANICAL DATA

Figure 8 : 32 PIN CERAMIC DUAL IN LINE FREAT SEAL

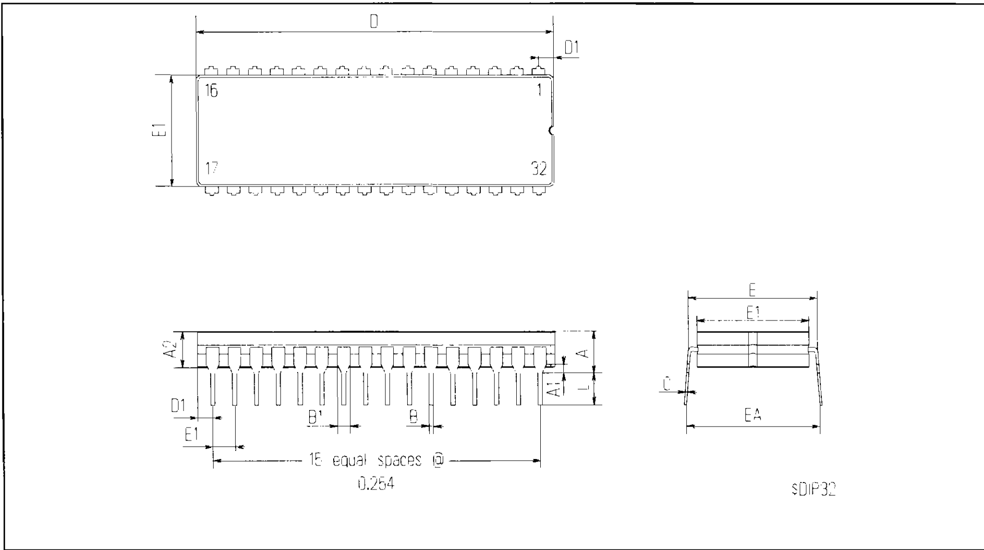
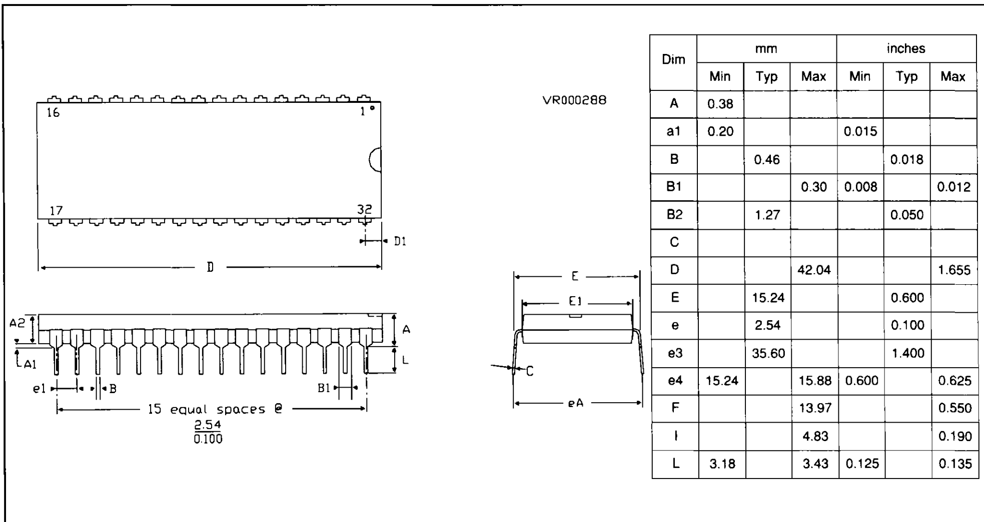


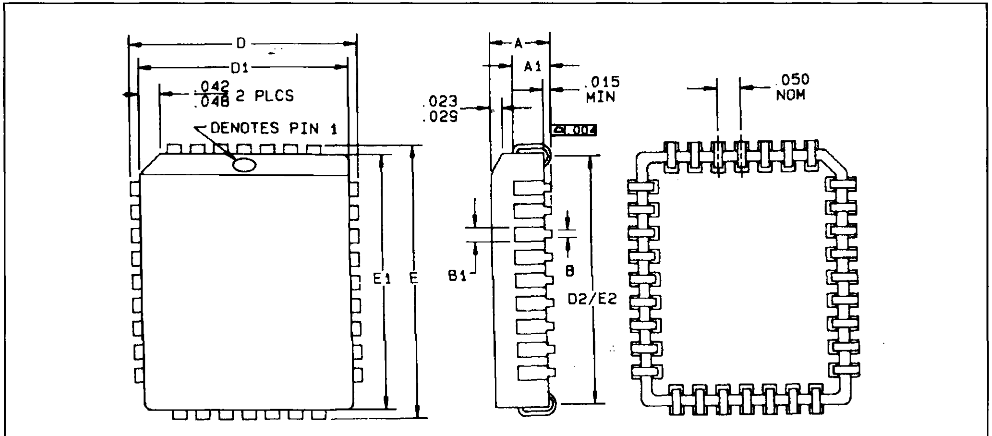
Figure 9 : 32 PIN PLASTIC DUAL IN LINE



Dim	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.38					
a1	0.20			0.015		
B		0.46			0.018	
B1			0.30	0.008		0.012
B2		1.27			0.050	
C						
D			42.04			1.655
E		15.24			0.600	
e		2.54			0.100	
e3		35.60			1.400	
e4	15.24		15.88	0.600		0.625
F			13.97			0.550
I			4.83			0.190
L	3.18		3.43	0.125		0.135

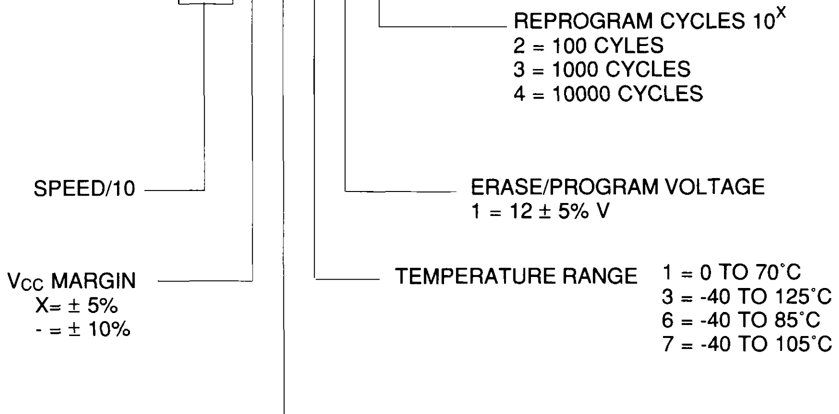
SGS-THOMSON MICROELECTRONICS

Figure 10 : 32 PIN PLCC



ORDERING INFORMATION

M	2	8	F	2	5	6	-	1	2	X	C	1	1	2



PACKAGE
C = PLCC
B = PLASTIC DIL
F = CERAMIC FRIT SEAL