32Mb (2M x 16 bit) UtRAM

Document Title

2Mx16 bit Multiplexed Synchronous Burst Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial - Design target	December 19, 2006	Preliminary
0.1	Revised - Inserted package dimension	January 11, 2007	Preliminary

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2M x 16 bit Multiplexed Synchronous Burst Uni-Transistor CMOS RAM

GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need bigger & faster memory capacity to handle the multi-media data. SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market. UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature. K1B3216B8E is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous page read and asynchronous write), the NOR flash like synchronous operation (synchronous burst read and asynchronous write) and the fully synchronous operation (synchronous burst read and synchronous burst write). These three operation modes are defined through the mode register setting. The device also supports the special features for the standby power saving. Those are the Partial Array Refresh(PAR) mode, Deep Power Down(DPD) mode and internal TCSR (Temperature Compensated Self Refresh). The optimization of output drive strength is possible through the mode register setting to adjust for the different data loadings. Through this drive strength optimization, the device can minimize the noise generated on the data bus during read operation.

FEATURES

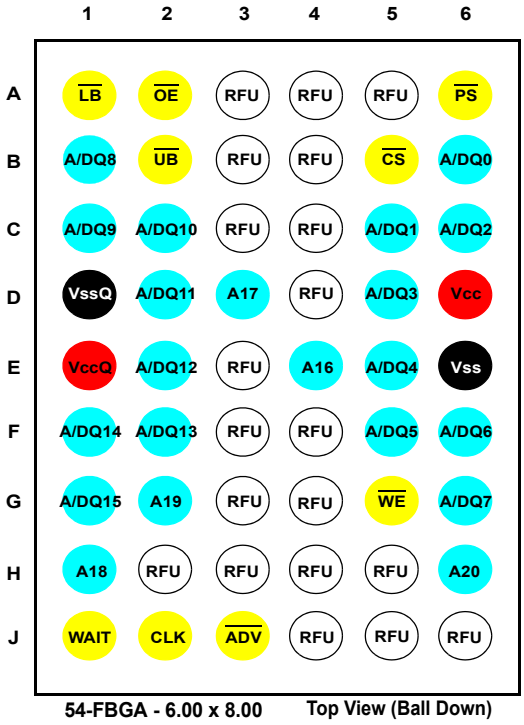
- Process technology: CMOS
- Organization: 2M x 16 bit
- Multiplexed Address and Data bus
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports MRS (Mode Register Set)
  - Software set up
- Supports power saving modes
  - PAR (Partial Array Refresh)
  - DPD (Deep Power Down)
  - Internal TCSR (Temperature Compensated Self Refresh)
- Supports driver strength optimization
- K1B3216B8E supports
  - Asynchronous read/ Asynchronous write
  - Synchronous burst read / Asynchronous write
  - Synchronous burst read / Synchronous burst write
- Synchronous burst operation
  - Max. clock frequency : 104MHz
  - Fixed and Variable read latency
  - 4 / 8 / 16 / 32 and Continuous burst
  - Wrap / No-wrap
  - Latency :4(Variable) @ 104MHz
    3(Variable) @ 80MHz
    2(Variable) @ 66MHz
  - Burst stop
  - Burst read suspend
  - Burst write data masking

PRODUCT FAMILY

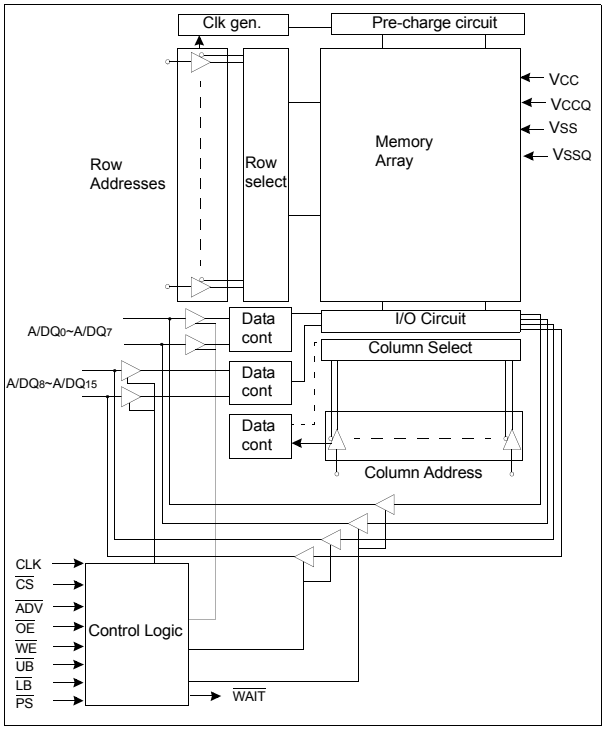
Product Family	Operating Mode[1)]	Operating Temp.	Vcc Range	Speed	Current Consumption	
					Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)
K1B3216B8E-I	Mode 1 Mode 2 Mode 3	Industrial(-40~85°C)	1.7~1.95V	104MHz	TBD < 85°C TBD < 40°C	TBD

1) Mode 1: Asynchronous read/ Asynchronous write
Mode 2: Synchronous burst read/ Asynchronous write
Mode 3: Synchronous burst read/ Synchronous burst write

PIN DESCRIPTIONS & FUNCTION BLOCK DIAGRAM



54-FBGA - 6.00 x 8.00 Top View (Ball Down)

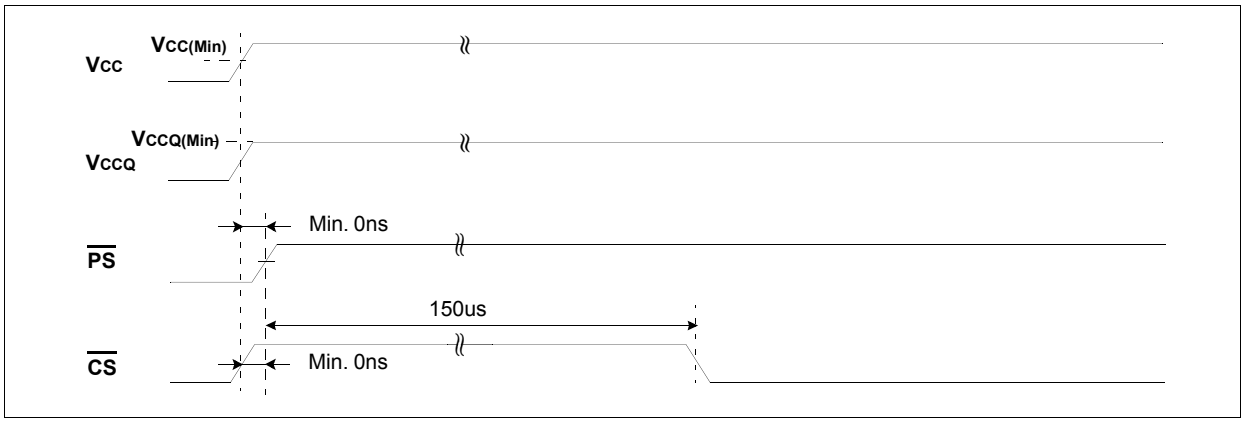


TERMINOLOGY DESCRIPTION

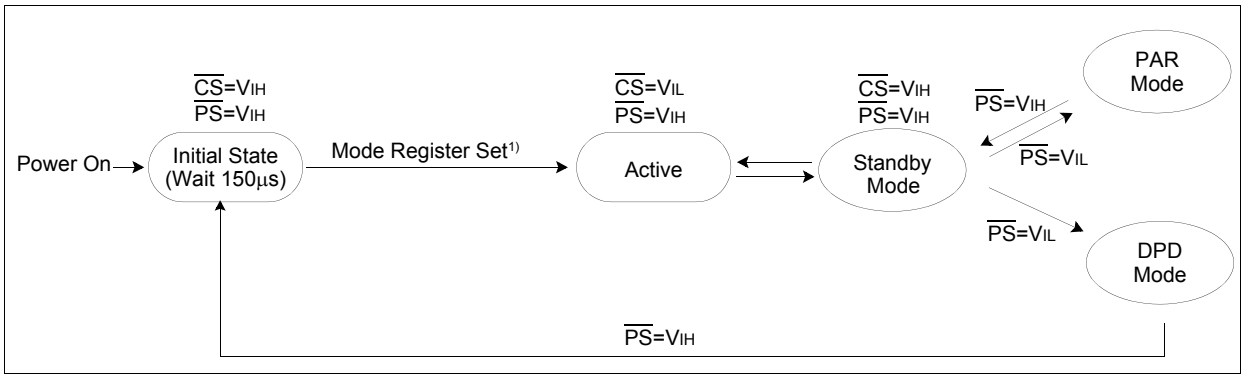
Name	Function	Type	Description
CLK	Clock	Input	Synchronizes the memory to the system operating frequency during synchronous operations. Commands are referenced to CLK.
$\overline{ADV}$	Address Valid	Input	Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of $\overline{ADV}$ during asynchronous READ and WRITE operations.
$\overline{PS}$	Mode Register set	Input	$\overline{PS}$ low enables either PAR or DPD to be set.
$\overline{CS}$	Chip Select	Input	$\overline{CS}$ low enables the chip to be active $\overline{CS}$ high disables the chip and puts it into standby mode or deep power down mode.
$\overline{OE}$	Output Enable	Input	Enables the output buffers when LOW. when $\overline{OE}$ is HIGH, the output buffers are disabled.
$\overline{WE}$	Write Enable	Input	$\overline{WE}$ low enables the chip to start writing the data
$\overline{LB}$	Lower Byte ($I/O_{0\sim7}$)	Input	$\overline{UB}$ ($\overline{LB}$) low enables upper byte (lower byte) to allow data Input/output from I/O buffers.
$\overline{UB}$	Upper Byte ($I/O_{8\sim15}$)	Input	
A16~A20	Address 16 ~ Address 20	Input	Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles.
A/DQ0~A/DQ15	Address and Data Inputs / Outputs	Input/Output	Address and Data I/Os: These pins are multiplexed address/ data bus.
Vcc	Voltage Source	Power	Device Power supply. Power supply for device core operation.
VccQ	I/O Voltage Source	Power	I/O Power supply. Power supply for input/output buffers.
Vss	Ground Source	GND	Ground for device core operation
VssQ	I/O Ground Source	GND	Ground for input/output buffers
$\overline{WAIT}$	Valid Data Indicator	Output	The $\overline{WAIT}$ signal is output signal indicating the status of the data on the bus whether or not it is valid. $\overline{WAIT}$ is asserted when a burst crosses a word-line boundary. $\overline{WAIT}$ is asserted and should be ignored during asynchronous and page mode operations.

POWER UP SEQUENCE

After V_{CC} and V_{CCQ} reach minimum operating voltage(1.7V), drive $\overline{CS}$ High first and then drive $\overline{PS}$ High. Then the device gets into the Power Up mode. Wait for minimum 150μs to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.
Mode1 (Asynchronous read/ Asynchronous write) is set up after power up, but this mode is not always guaranteed.



MODE STATE MACHINE



1) Refer to MRS(Mode Register Set).

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Power supply voltage relative to Vss	V_{CC}, V_{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	VCC	1.7	1.8	1.95	V
Power supply voltage(I/O)	VCCQ	1.7	1.8	1.95	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	VCCQ-0.4	-	V_{CCQ}+0.2[2]	V
Input low voltage	V_{IL}	-0.2[3]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CCQ} +1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions			Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CCQ}			-1	-	1	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{PS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to V_{CCQ}			-1	-	1	µA
Average Operating Current(Async)	I_{CC2}[6]	Cycle time=70ns, I_{IO}=0mA[4], 100% duty, $\overline{CS}$=V_{IL}, $\overline{PS}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}			-	-	TBD	mA
Average Operating Current(Sync)	I_{CC3}	Burst Length 4, Latency 5, 104MHz, I_{IO}=0mA[4], Address transition 1 time, $\overline{CS}$=V_{IL}, $\overline{PS}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}			-	-	TBD	mA
Output Low Voltage	V_{OL}	I_{OL}=0.2mA			-	-	0.2	V
Output High Voltage	V_{OH}	I_{OH}=-0.2mA			1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1]	$\overline{CS}$≥V_{CCQ}-0.2V, $\overline{PS}$≥V_{CCQ}-0.2V, Other inputs=Vss or V_{CCQ} (Toggle is not allowed)[5]	< 40°C		-	-	TBD	µA
			< 85°C		-	-	TBD	µA
Partial Refresh Current	I_{SBP}[2]	$\overline{PS}$≤0.2V, $\overline{CS}$≥V_{CCQ}-0.2V, Other inputs=Vss or V_{CCQ} (Toggle is not allowed)[5]	< 40°C	1/2 Block	-	-	TBD	µA
				1/4 Block	-	-	TBD	
			< 85°C	1/2 Block	-	-	TBD	µA
				1/4 Block	-	-	TBD	
Deep Power Down Current	I_{SBD}	$\overline{PS}$≤0.2V, $\overline{CS}$≥V_{CCQ}-0.2V, Other inputs=Vss or V_{CCQ} (Toggle is not allowed)[5]	< 85°C		-	-	TBD	µA

1. I_{SB1} is measured after 60ms after $\overline{CS}$ high. CLK should be fixed at high or at Low.
2. Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).
3. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle below 40°C.
4. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.
5. V_{IN}=0V; all inputs should not be toggle.
6. Clock should not be inserted between $\overline{ADV}$ low and $\overline{WE}$ low during Write operation.

MRS (MODE REGISTER SET)

The mode registers store the values for the various modes to make UtRAM suitable for a various applications through MRS. The mode registers have lots of fields and each field consists of several options. Refer to the Table below for detailed Mode Register Setting. A19~A20 addresses are "Don't care" in Mode Register Setting.

MRS CODE

MRS code consists of 12 categories and several options in each category. RARS, PARA, PAR and DPD are related to power saving, BL, WC, Latency, Wrap, WP, MS and IL are related to bus operation and DS is related to device output impedance.

Mode Register Setting according to field of function

Address	A18	A17~A16	A/DQ15~A/DQ14	A/DQ13	A/DQ12	A/DQ11~A/DQ9	A/DQ8	A/DQ7~A/DQ5	A/DQ4	A/DQ3	A/DQ2	A/DQ1~A/DQ0
Function	IL	DS	MS	WP	Wrap	Latency	WC	BL	DPD	PAR	PARA	PARS

Initial Latency		Driver Strength			Mode Select		
A18	IL	A17	A16	DS	A/DQ15	A/DQ14	MS
0	**Fixed**	0	0	Full Drive	0	0	**Mode 1**(Async. Read / Async. Write)
1	Variable	0	1	**1/2 Drive**	0	1	Mode 2 (Sync. Burst Read / Async. Write)
		1	0	1/4 Drive	1	0	Mode 3 (Sync. Burst Read / Sync. Burst Write)

$\overline{WAIT}$ Polarity		Wrap		Latency Count				$\overline{Wait}$ Configuration		Burst Length			
A/DQ13	WP[1)]	A/DQ12	Wrap	A/DQ11	A/DQ10	A/DQ9	Latency	A/DQ8	WC	A/DQ7	A/DQ6	A/DQ5	BL
0	**Low Enable**	0	**Wrap**	1	0	0	2	0	**One clock prior**	0	1	0	4 word
1	High Enable	1	No-Wrap	0	0	0	3	1	At data	0	1	1	8 word
				0	0	1	4			1	0	0	**16 word**
				0	1	0	**5**			1	0	1	32 word
				0	1	1	6			1	1	1	Continuous[2)]
				1	0	1	7						
				1	1	0	8						
				1	1	1	9						

Deep Power Down		Partial Array Refresh		PAR Array		PAR Size		
A/DQ4	DPD	A/DQ3	PAR	A/DQ2	PARA	A/DQ1	A/DQ0	PARS
0	DPD Enable	0	PAR Enable	0	Bottom Array	0	0	Full Array
1	**DPD Disable**	1	**PAR Disable**	1	Top Array	1	0	1/2 Array
						1	1	1/4 Array

[Note]
- A19~A20 addresses are "Don't care" & reserved for future use.
- The modes are set automatically to default modes which are Async. Read and Async. Write/ DPD disable / PAR disable after power up or DPD exit.

- Mode Change Rules.
  Mode1(2) to Mode3 : 1 dummy write(to any address with any data) is necessary before setting Mode3
  * Dummy write: Dummy write timing is just the same with normal write timing. It is necessary because 'Late write' is applied to Asynchronous write as in Mode1(2).
  * Late write: The data that is latched in previous write cycle is written in the address that is also latched in previous write cycle when Write starts. And current data and address are latched when Write ends. ($\overline{WE}$ high or $\overline{CS}$ high, whichever comes first)

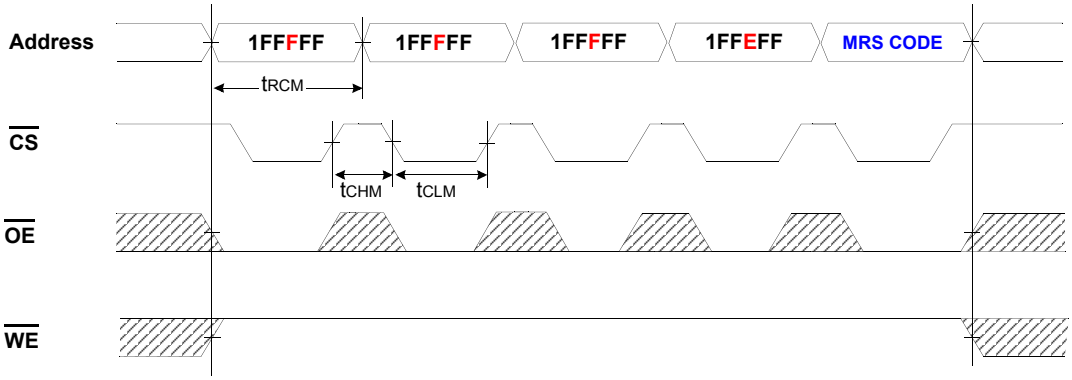
  Mode3 to Mode1(2) : 1 dummy write is necessary before setting Mode1(2)
  * Dummy write: The data and the address should be the same with those which are used during Mode1(2) to Mode3 transition.

1) WP[0]; The data is available when $\overline{WAIT}$ signal is High. All the timings in this spec are illustrated based on this mode.
   WP[1]; The data is available when $\overline{WAIT}$ signal is Low.
2) Refresh command will be denied during continuous operation. $\overline{CS}$ low should not be longer than tBC(max. 2.5us)

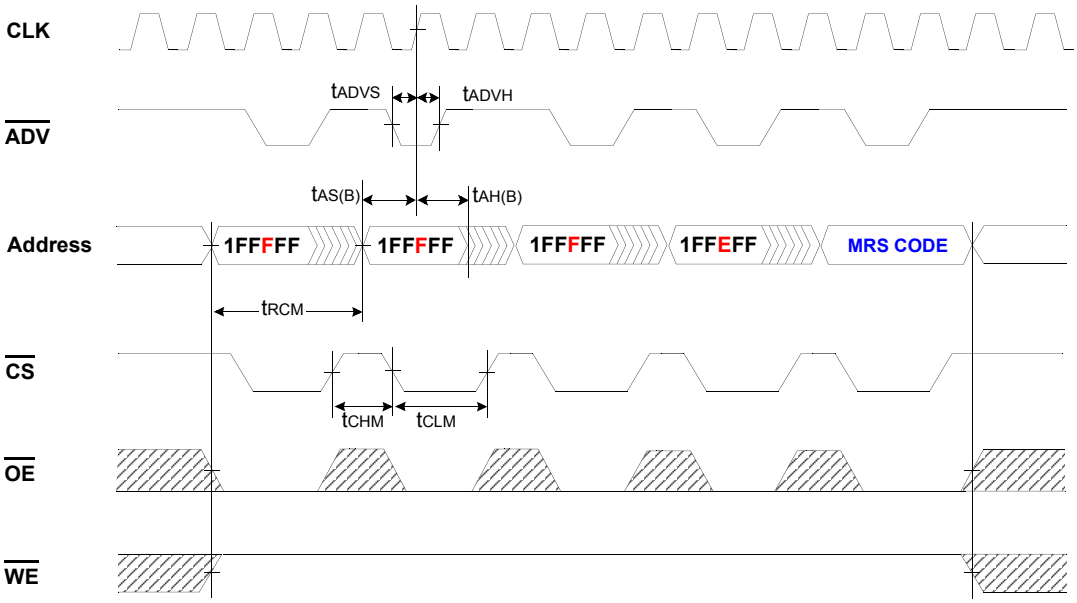
MRS TIMING WAVEFORM (SOFTWARE)

Software MRS timing consists of 5 Read cycles. Each cycle is normal Read cycle. $\overline{CS}$ pin should be toggling between cycles. 1st, 2nd and 3rd cycle should be 1FFFFF(h), 4th cycle should be 1FFEFF(h) and 5th cycle should be MRS code

Asynch. Mode Clock, $\overline{ADV}$, $\overline{UB}$ and $\overline{LB}$ = Don't care, $\overline{WAIT}$=High-Z, $\overline{PS}$=V_{IH}



Synch. Mode $\overline{UB}$ and $\overline{LB}$ = Don't care, $\overline{PS}$=V_{IH}



Note) Above timing and address condition should not be used in the normal operation. The above condition should be used only for the mode register setting purpose.

AC CHARACTERISTICS

Parameter List	Symbol	Min	Max	Units	Parameter List	Symbol	Min	Max	Units
$\overline{ADV}$ setup time to clock	t_{ADVS}	3	-	ns	Read cycle time	t_{RCM}	70	-	ns
$\overline{ADV}$ hold time from clock	t_{ADVH}	2	-	ns	$\overline{CS}$ high time	t_{CHM}	10	-	ns
Address setup time to clock	$t_{AS(B)}$	3	-	ns	$\overline{CS}$ low time	t_{CLM}	60	-	ns
Address hold time from clock	$t_{AH(B)}$	2	-	ns					

PAR (Partial Array Refresh) mode A/DQ[3]~A/DQ[0]

User can select half array, a fourth array as active memory array. The active memory array is periodically refreshed(data stored), whereas the disabled array is not going to be refreshed and so the previously stored data will be invalid. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the MRS.

PAR mode execution;

1) Mode Register Setting into PAR enable(A/DQ3=0)
   DPD enabled setting(A/DQ4=0) has higher priority to PAR enabled setting(A/DQ3=0). A/DQ4=1 is necessary to use PAR mode.
2) PAR mode Enter; keep $\overline{PS}$ signal at V_{IL} for longer than 0.5μs during standby mode (Mode Register: A/DQ4=1 & A/DQ3=0).
3) PAR mode Exit; The device returns to the standby mode when $\overline{PS}$ signal goes to V_{IH} during PAR mode.
   * Mode register values are not changed after the device has been to PAR mode.

DPD (Deep Power Down) mode A/DQ[4]

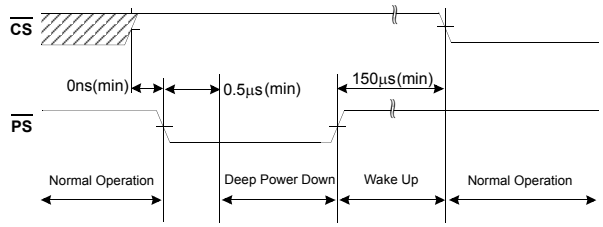
The deep power down mode disables all the refresh related activities. This mode can be used when the system needs to save power. The data become invalid when DPD mode is executed.

DPD mode execution ;

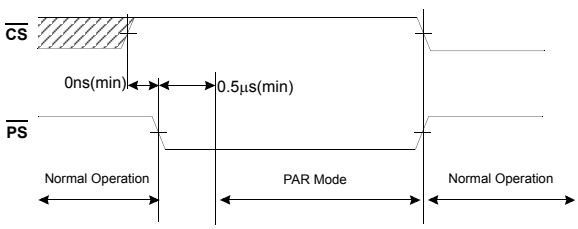
1) Mode Register Setting into DPD enable(A/DQ4=0)
2) DPD mode Enter; keep $\overline{PS}$ signal at V_{IL} for more than 0.5μs during standby mode (Mode Register: A/DQ4=0).
3) DPD mode Exit; The device returns to initial State when $\overline{PS}$ signal goes to V_{IH} during DPD mode. Wake up sequence is needed for the device to do normal operation.

* Mode register values are initialized to default value after the device has been to DPD mode.
  Default modes are Async. Read and Async. Write / DPD disable / PAR disable.

DPD MODE EXECUTION and EXIT



PAR MODE EXECUTION and EXIT



STANDBY MODE CHARACTERISTICS

Power Mode	Address (Bottom Array)[2]	Address (Top Array)[2]	Memory Cell Data	Standby[3] (I_{SB1}, <40°C)	Standby[3] (I_{SB1}, <85°C)	Wait Time(μs)
Standby(Full Array)	000000h ~ 1FFFFFh	000000h ~ 1FFFFFh	Valid[1]	TBD	TBD	0
Partial Refresh(1/2 Block)	000000h ~ 0FFFFFh	100000h ~ 1FFFFFh	Valid[1]	TBD	TBD	0
Partial Refresh(1/4 Block)	000000h ~ 07FFFFh	180000h ~ 1FFFFFh	Valid[1]	TBD	TBD	0
Deep Power Down	000000h ~ 1FFFFFh		Invalid	TBD	TBD	150

1. Only the data in the selected blocks are valid
2. PAR Array can be selected through Mode Register Set
3. Standby mode is supposed to be set up after at least one active operation after power up.
   I_{SB1} is measured after 60ms from the time when standby mode is set up.

Burst Length A/DQ[7]~A/DQ[5] & Wrap A/DQ[12]

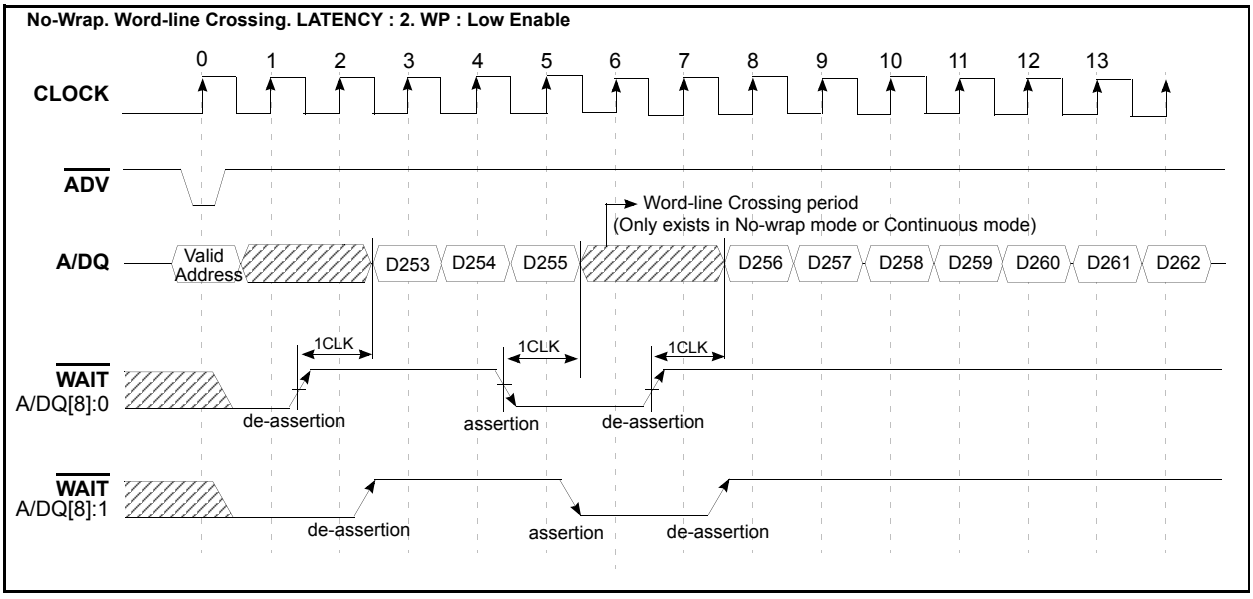
The device supports 4 word, 8 word, 16 word, 32 word and Continuous burst read or write. and Wrap & No-Wrap are supported for Burst sequence.

Burst Address Sequence(Decimal)					
Mode	**Start**	**4 word**	**8 word**	**16 word**	**32 word**
WRAP	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31 - 0
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31 - 0 - 1
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31- 0 - 1 - 2
	~		~	~	~
	7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7 - 8 - 9 - 10- 11- 12 ~ 2 - 3 - 4 - 5 - 6
	~			~	~
	15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20 ~ 10- 11- 12- 13- 14
	~				~
	31				31- 0 - 1 - 2 - 3 - 4 ~ 25-26-27-28-29-30
No-WRAP	0	0-1-2-3	0- 1- 2- 3- 4- 5- 6 -7	0- 1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-4	1- 2- 3- 4- 5- 6- 7- 8	1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31-32
	2	2-3-4-5	2- 3- 4- 5- 6- 7- 8- 9	2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31-32-33
	3	3-4-5-6	3- 4- 5- 6- 7- 8- 9-10	3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17-18	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31-32-33-34
	~		~	~	~
	7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7 - 8 - 9 - 10-11-12 ~ 33-34-35-36-37-38
	~			~	~
	15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-18-19-20 ~ 41-42-43-44-45-46
	~				~
	31				31-32-33-34-35-36 ~ 57-58-59-60-61-62

1. Continuous Burst mode needs to meet tBC(max. 2.5us) parameter.

$\overline{\text{WAIT}}$ Configuration A/DQ[8] & $\overline{\text{WAIT}}$ Polarity A/DQ[13]

The $\overline{\text{WAIT}}$ signal is output signal indicating the status of the data on the bus whether or not it is valid. $\overline{\text{WAIT}}$ configuration is to decide the timing when $\overline{\text{WAIT}}$ asserts or desserts. $\overline{\text{WAIT}}$ asserts (or desserts) one clock prior to the data when A/DQ8 is set to 0. ($\overline{\text{WAIT}}$ asserts (or desserts) at data clock when A/DQ8 is set to 1). $\overline{\text{WAIT}}$ polarity is to decide the $\overline{\text{WAIT}}$ signal level at which data is valid or invalid. Data is valid if $\overline{\text{WAIT}}$ signal is high when A/DQ13 is set to 0. (Data is valid if $\overline{\text{WAIT}}$ signal is low when A/DQ13 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; A/DQ[13]:0 and A/DQ[8]:0.
Below timing shows $\overline{\text{WAIT}}$ signal's movement when word boundary crossing happens in No-wrap mode.

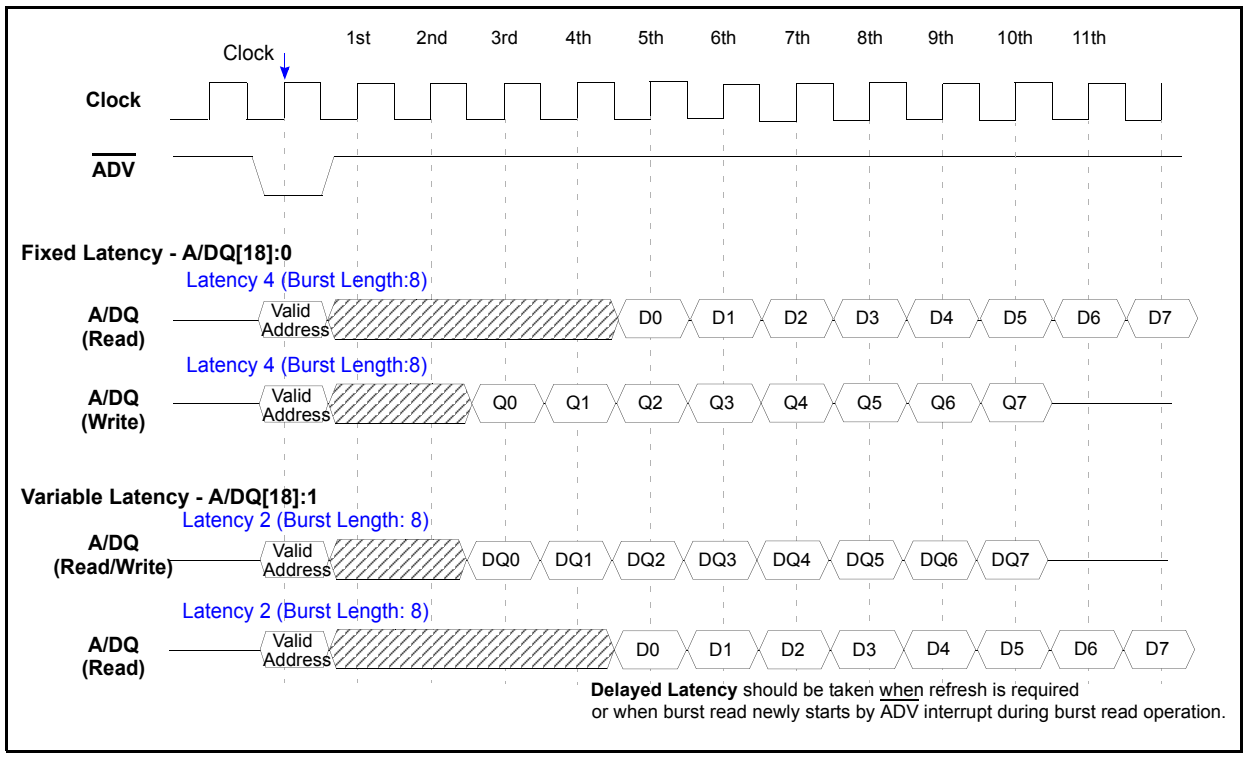


Latency A/DQ[11]~A/DQ[9]

The Latency stands for the number of clocks before the first data available from the burst command.

Item	Upto 66MHz		Upto 80MHz		Upto 104MHz	
	Fixed	Variable	Fixed	Variable	Fixed	Variable
Latency Set(A/DQ11:A/DQ10:A/DQ9)	4(0:0:1)	2(1:0:0)	5(0:1:0)	3(0:0:0)	7(1:0:1)	4(0:0:1)
Read Latency(min)	4	2 / 4[1)]	5	3 / 5[1)]	7	4 / 7[1)]
1st Read data fetch clock	5th	3rd / 5th[1)]	6th	4th / 6th[1)]	8th	5th / 8th[1)]
Write Latency(min)	2	2	3	3	4	4
1st Write data loading clock	3rd	3rd	4th	4th	5th	5th

1) **Delayed Latency** should be taken when refresh is required or when burst read newly starts by $\overline{ADV}$ interrupt during burst read operation.



Driver Strength A/DQ[17]~A/DQ[16]

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength.

Driver Strength	Full	1 / 2	1 / 4
IMPEDANCE(typ.)	40Ω	90Ω	150Ω

1. Impedance values are typical values, not 100% tested.

OPEARTION MODE (A/DQ[15]~A/DQ[14])

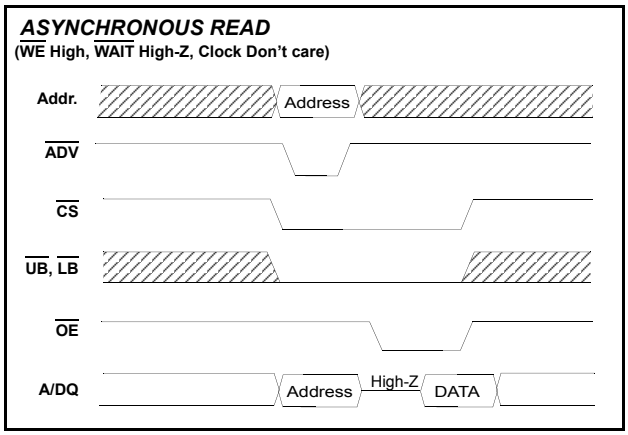
MODE1. ASYNCHRONOUS READ / ASYNCHRONOUS WRITE MODE

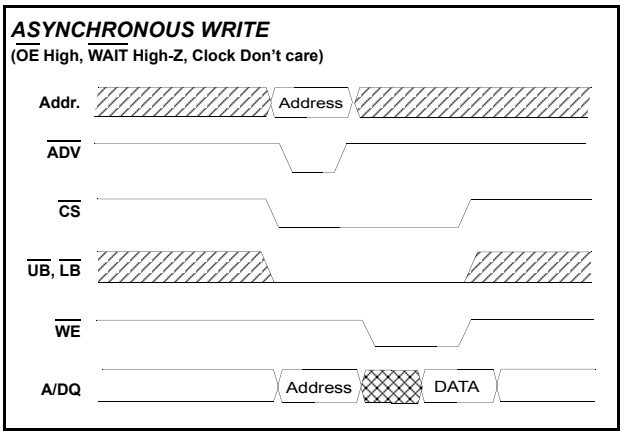
Asynchronous read operation

Asynchronous read operation starts when $\overline{CS}$, $\overline{OE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. First data come out after random access time(tAA) but second, third and fourth data come out after page access time(tPA) when using the page addresses (A/DQ0, A/DQ1). $\overline{PS}$ and $\overline{WE}$ should be de-asserted during read operation. Clock is don't care during read operation and $\overline{WAIT}$ is Hi-Z.

Asynchronous write operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. $\overline{PS}$ and should be de-asserted during write operation. Clock, $\overline{OE}$ are don't care during write operation and $\overline{WAIT}$ signal is Hi-Z.





FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{ADV}$	A/DQ0~15	A16 ~ A20	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	X[1)]	Deselected	Standby
L	H	H	X[1)]	X[1)]	H	High-Z	X[1)]	Output Disabled	Active
L	X[1)]	X[1)]	H	H	X[1)]	High-Z	X[1)]	Output Disabled	Active
L	H	H	H	H	⎍	Add. Input	Add. Input	Address Input	Active
L	L	H	L	H	H	Dout	X[1)]	Lower Byte Read	Active
L	L	H	H	L	H	Dout	X[1)]	Upper Byte Read	Active
L	L	H	L	L	H	Dout	X[1)]	Word Read	Active
L	H	L	L	H	H	Din	X[1)]	Lower Byte Write	Active
L	H	L	H	L	H	Din	X[1)]	Upper Byte Write	Active
L	H	L	L	L	H	Din	X[1)]	Word Write	Active

1. X means "Don't care". X should be low or high state.
2. In asynchronous mode, Clock is ignored. Clock should be low or high state.
3. /WAIT pin is High-Z in Asynchronous mode.

MODE2. SYNCHRONOUS BURST READ / ASYNCHRONOUS WRITE MODE

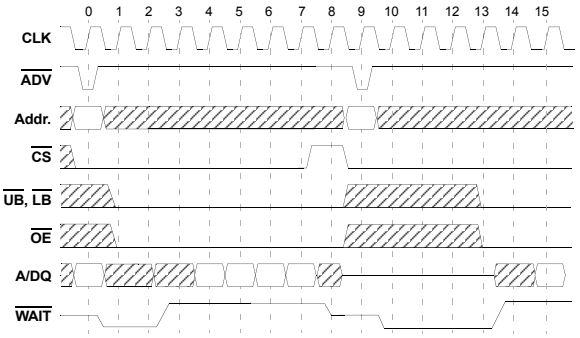
Synchronous Burst Read Operation

Burst Read command is implemented when $\overline{ADV}$ is detected low at clock rising edge. $\overline{WE}$ should be de-asserted during Burst read, Burst operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of operation.
Variable latency allows the UtRAM to be configured for minimum latency at high frequencies, but the controller must monitor $\overline{WAIT}$ to detect any conflict with refresh cycles.

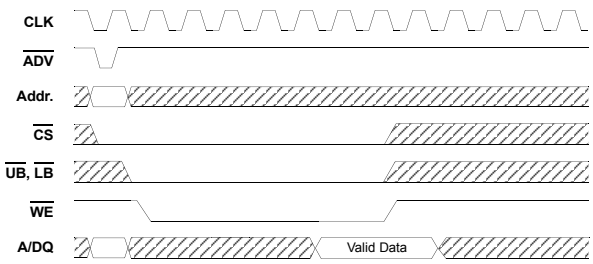
Asynchronous Write Operation

Asynchronous write operation starts when $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$ or $\overline{LB}$ are asserted. $\overline{PS}$ and should be de-asserted during write operation. Clock, $\overline{OE}$ are don't care during write operation and $\overline{WAIT}$ signal is Hi-Z.

SYNCHRONOUS BURST READ
(Latency 3, BL 4, WP : Low Enable, $\overline{PS}$ High, $\overline{WE}$ High)



ASYNCHRONOUS WRITE
($\overline{PS}$ High, $\overline{OE}$ High, $\overline{WAIT}$ High-Z, Clock Don't care)



FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{PS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	A/DQ0~7	A/DQ8~15	CLK	$\overline{ADV}$	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	Standby
H	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	PAR
L	H	H	H	X[1)]	X[1)]	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	H	X[1)]	H	X[1)]	X[1)]	Address	Address	⎍	⎍⎍	Read Command	Active
L	H	L	H	L	H	Dout	High-Z	⎍	H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	⎍	H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	⎍	H	Word Read	Active
L	H	H	L	L	H	Din	High-Z	X[1)]	H	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	X[1)]	H	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	X[1)]	H	Word Write	Active

1. X means "Don't care". X should be low or high state.
2. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

MODE3. SYNCHRONOUS BURST READ / SYNCHRONOUS BURST WRITE MODE

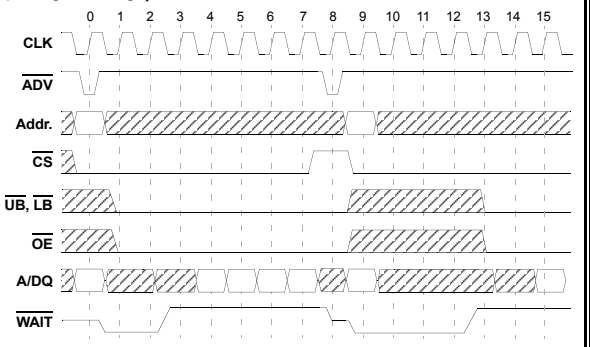
Synchronous Burst Read Operation

Burst Read command is implemented when $\overline{ADV}$ is detected low at clock rising edge. $\overline{WE}$ should be de-asserted during Burst read, Burst Read operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of Burst Read operation. Variable latency allows the UtRAM to be configured for minimum latency at high frequencies, but the controller must monitor $\overline{WAIT}$ to detect any conflict with refresh cycles.

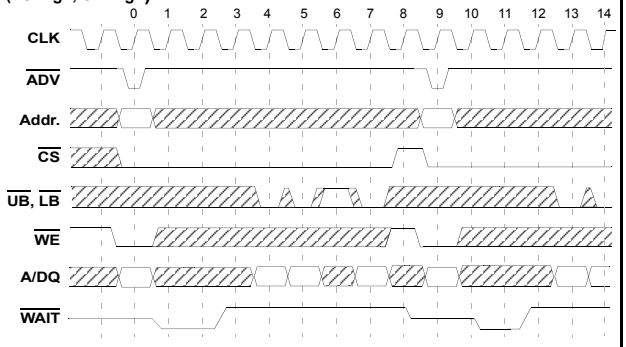
Synchronous Burst Write Operation

Burst Write command is implemented when $\overline{ADV}$ & $\overline{WE}$ are detected low at clock rising edge. Burst Write operation re-starts whenever $\overline{ADV}$ is detected low at clock rising edge even in the middle of Burst Write operation.
Write operations always use fixed latency.

SYNCHRONOUS BURST READ(Latency 3, BL 4, WP : Low Enable)
($\overline{PS}$ High, $\overline{WE}$ High)



SYNCHRONOUS BURST WRITE(Latency 3, BL 4, WP : Low Enable)
($\overline{PS}$ High, $\overline{OE}$ High)



FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{PS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	Standby
H	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	X[1)]	X[1)]	Deselected	PAR
L	H	H	H	X[1)]	X[1)]	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	X[1)]	H	Output Disabled	Active
L	H	X[1)]	H	X[1)]	X[1)]	High-Z	High-Z	⎍	⎍	Read Command	Active
L	H	L	H	L	H	Dout	High-Z	⎍	H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	⎍	H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	⎍	H	Word Read	Active
L	H	X[1)]	L	X[1)]	X[1)]	High-Z	High-Z	⎍	⎍	Write Command	Active
L	H	H	X[1)]	L	H	Din	High-Z	⎍	H	Lower Byte Write	Active
L	H	H	X[1)]	H	L	High-Z	Din	⎍	H	Upper Byte Write	Active
L	H	H	X[1)]	L	L	Din	Din	⎍	H	Word Write	Active

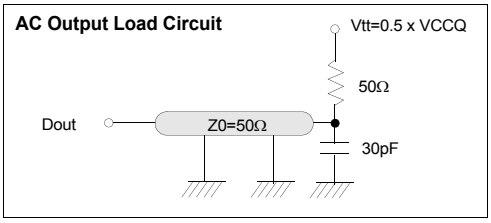
1. X means "Don't care". X should be low or high state.
2. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

MODE 1 AC OPERATING CONDITIONS (ASYNCH. READ / ASYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -40°C~85°C

AC Output Load Circuit



AC CHARACTERISTICS

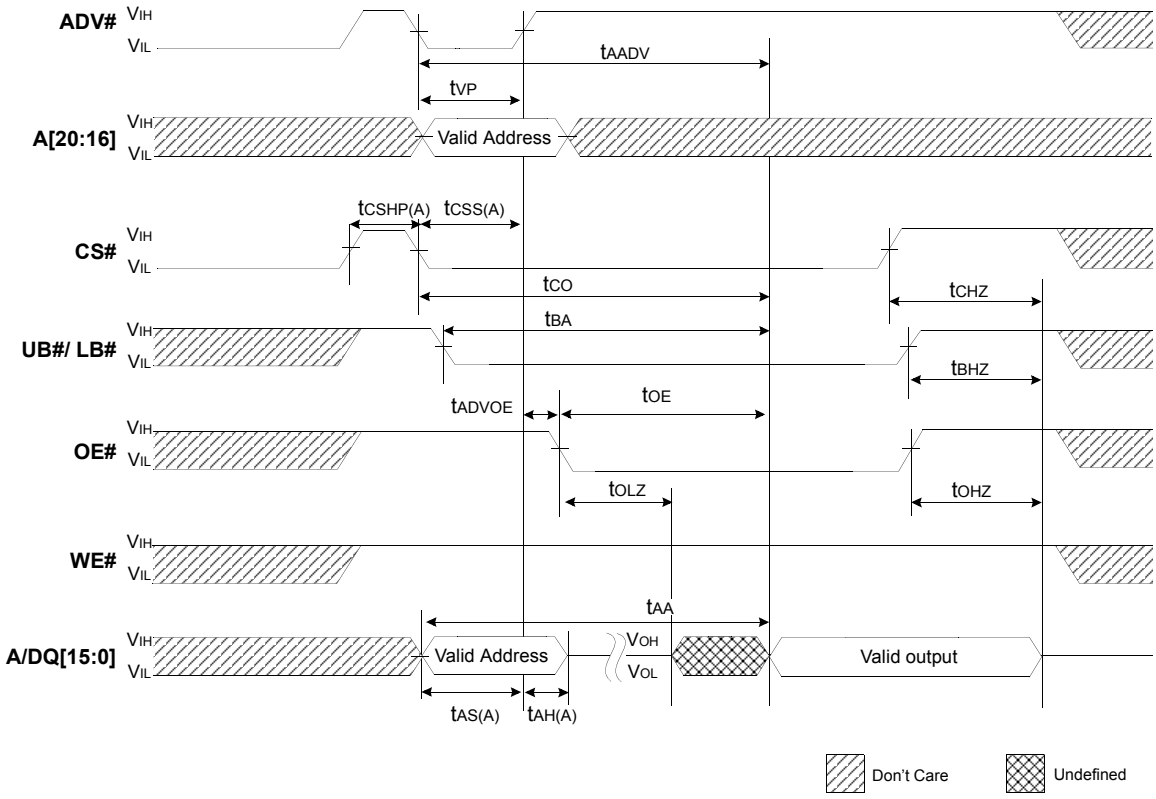
Parameter List		Symbol	Speed		Units
			Min	Max	
Common	$\overline{CS}$ High Pulse Width	$t_{CSHP(A)}$	10	-	ns
	Address Set-up Time to $\overline{ADV}$ Rising	$t_{AS(A)}$	7	-	ns
	Address Hold Time from $\overline{ADV}$ Rising	$t_{AH(A)}$	3	-	ns
	$\overline{ADV}$ Pulse Width Low	t_{VP}	7	-	ns
Asynch. Read	Address Access Time	t_{AA}	-	70	ns
	$\overline{ADV}$ Access Time	t_{AADV}	-	70	ns
	$\overline{CS}$ Setup Time to $\overline{ADV}$ Rising	$t_{CSS(A)}$	5	-	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	20	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	20	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{CHZ}	0	10	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	10	ns
	Output Disable to High-Z Output	t_{OHZ}	0	10	ns
	$\overline{ADV}$ High to $\overline{OE}$ Low	t_{ADVOE}	5	-	ns
Asynch. Write	$\overline{ADV}$ Setup to end of Write	t_{VS}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Data to Write Time Overlap	t_{DW}	20	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	$\overline{CS}$ Low to $\overline{ADV}$ High	t_{CVS}	7	-	ns
	$\overline{ADV}$ High to $\overline{WE}$ Low	t_{ADVWE}	5	-	ns

1. t_{WP}(min)=70ns for continuous write without CS toggling longer than 2.5us
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

TIMING WAVEFORMS (ASYNCH. READ / ASYNCH. WRITE)

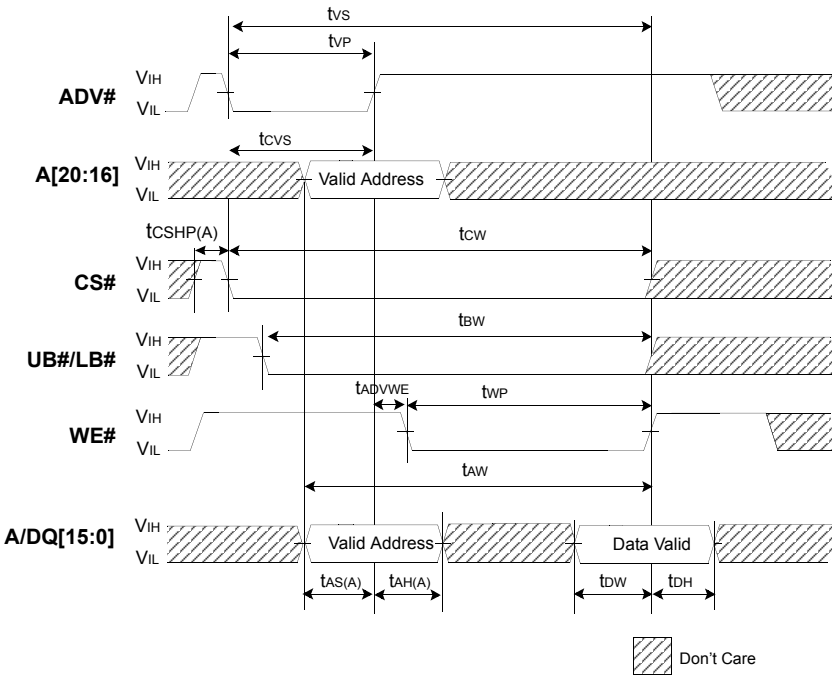
Asynch. READ

($\overline{PS}$=VIH, $\overline{WE}$=VIH, $\overline{WAIT}$=High-Z)



1. tCHZ and tOHZ are defined as the time when the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. In asynchronous read cycle, Clock is ignored.

Asynchronous WRITE

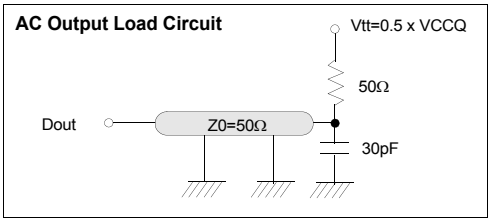


Notes:
1. The end of the WRITE cycle is controlled by CE#, UB#/LB#, or WE#, whichever de-asserts first.

MODE 2 AC OPERATING CONDITIONS (SYNCH. READ / ASYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 1ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -40°C~85°C



AC CHARACTERISTICS

Parameter List		Symbol	66MHz		80MHz		104MHz		Units
			Min	Max	Min	Max	Min	Max	
Synch. Burst Read	Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
	Burst Cycle Time	t_{BC}	-	2500	-	2500	-	2500	ns
	Address Set-up Time to clock	$t_{AS(B)}$	5	-	4	-	3	-	ns
	Address Hold Time from clock	$t_{AH(B)}$	2	-	2	-	2	-	ns
	$\overline{ADV}$ Setup Time to clock	t_{ADVS}	5	-	4	-	3	-	ns
	$\overline{ADV}$ Hold Time from clock	t_{ADVH}	2	-	2	-	2	-	ns
	$\overline{CS}$ Setup Time to clock	$t_{CSS(B)}$	5	-	4	-	3	-	ns
	$\overline{CS}$ High to $\overline{ADV}$ Low (Burst Stop)	t_{BSADV}[1]	0		0		0		ns
	$\overline{CS}$ Low Hold Time from Clock(Burst Stop)	t_{CSLH}	2	-	2	-	2	-	ns
	$\overline{CS}$ High Pulse Width	t_{CSHP}	5	-	5	-	5	-	ns
	$\overline{CS}$ Low to $\overline{WAIT}$ Low	t_{WL}	-	7.5	-	7.5	-	7.5	ns
	Clock to $\overline{WAIT}$ High	t_{WH}	-	11	-	9	-	7	ns
	$\overline{CS}$ High to $\overline{WAIT}$ High-Z	t_{WZ}	-	10	-	10	-	10	ns
	$\overline{UB}$, $\overline{LB}$ Low to End of Latency Clock	t_{BEL}	20	-	20	-	20	-	ns
	$\overline{OE}$ Low to End of Latency Clock	t_{OEL}	20	-	20	-	20	-	ns
	$\overline{UB}$, $\overline{LB}$ Low to Low-Z Output	t_{BLZ}	5	-	5	-	5	-	ns
	$\overline{OE}$ Low to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	ns
	Clock Rising to Data Output	t_{CD}	-	11	-	9	-	7	ns
	Output Hold from clock	$t_{OH(B)}$	3	-	3	-	3	-	ns
	Burst End Clock to Output High-Z	t_{HZ}	-	10	-	10	-	10	ns
	$\overline{CS}$ High to Output High-Z	t_{CHZ}	-	10	-	10	-	10	ns
	$\overline{OE}$ High to Output High-Z	t_{OHZ}	-	10	-	10	-	10	ns
	$\overline{UB}$, $\overline{LB}$ High to Output High-Z	t_{BHZ}	-	10	-	10	-	10	ns
	ADV# high to OE# Low	t_{ADVO}	5	-	4	-	3	-	ns

1. Refresh can not be implemented when tBSADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBSADV.
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

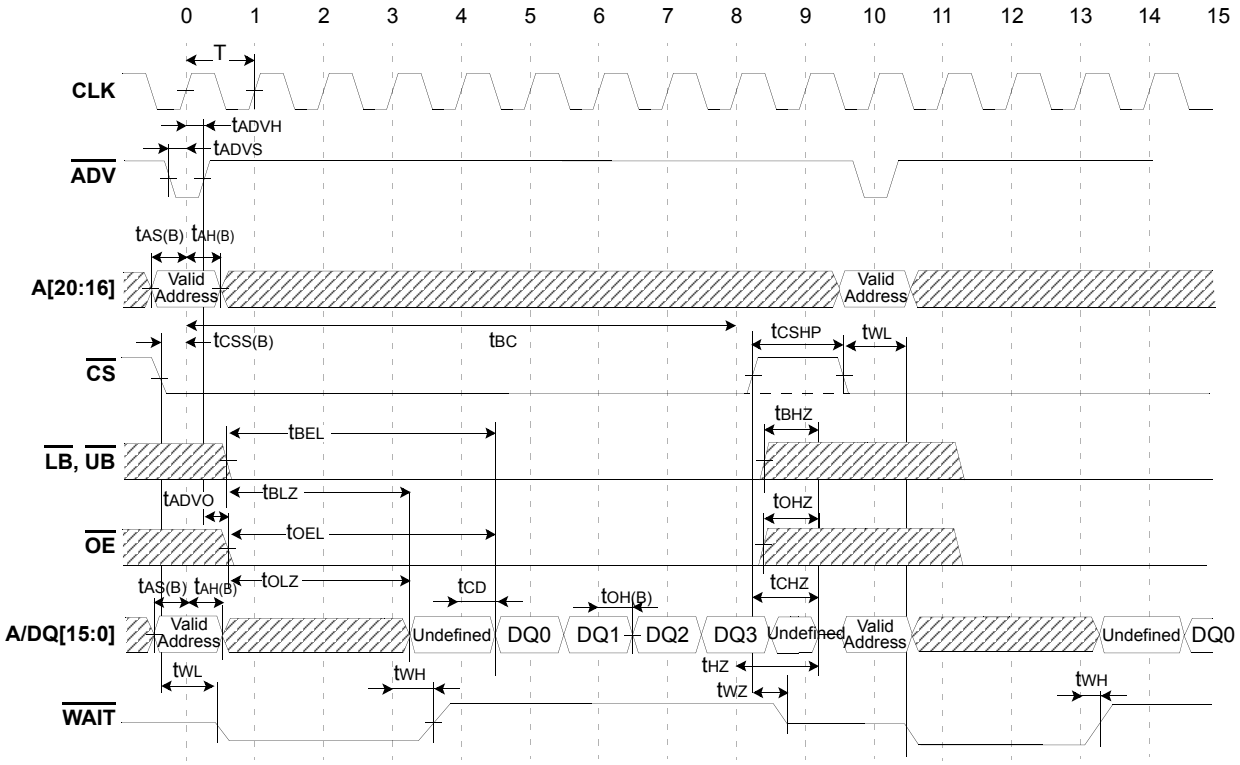
Parameter List		Symbol	Speed		Units
			Min	Max	
Asynch. Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	$\overline{ADV}$ Minimum Low Pulse Width	t_{ADV}	5	-	ns
	Address Set-up Time to $\overline{ADV}$ Rising	$t_{AS(A)}$	5	-	ns
	Address Hold Time from $\overline{ADV}$ Rising	$t_{AH(A)}$	3	-	ns
	$\overline{CS}$ Setup Time to $\overline{ADV}$ Rising	$t_{CSS(A)}$	5	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1]	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Data to Write Time Overlap	t_{DW}	20	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns
	ADV# HIGH to WE# LOW	t_{ADVWE}	5	-	ns

1. t_{WP}(min)=70ns for continuous write longer than 2.5us without CS toggling.

TIMING WAVEFORMS (SYNCH. READ / SYNCH. WRITE)

Burst READ - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



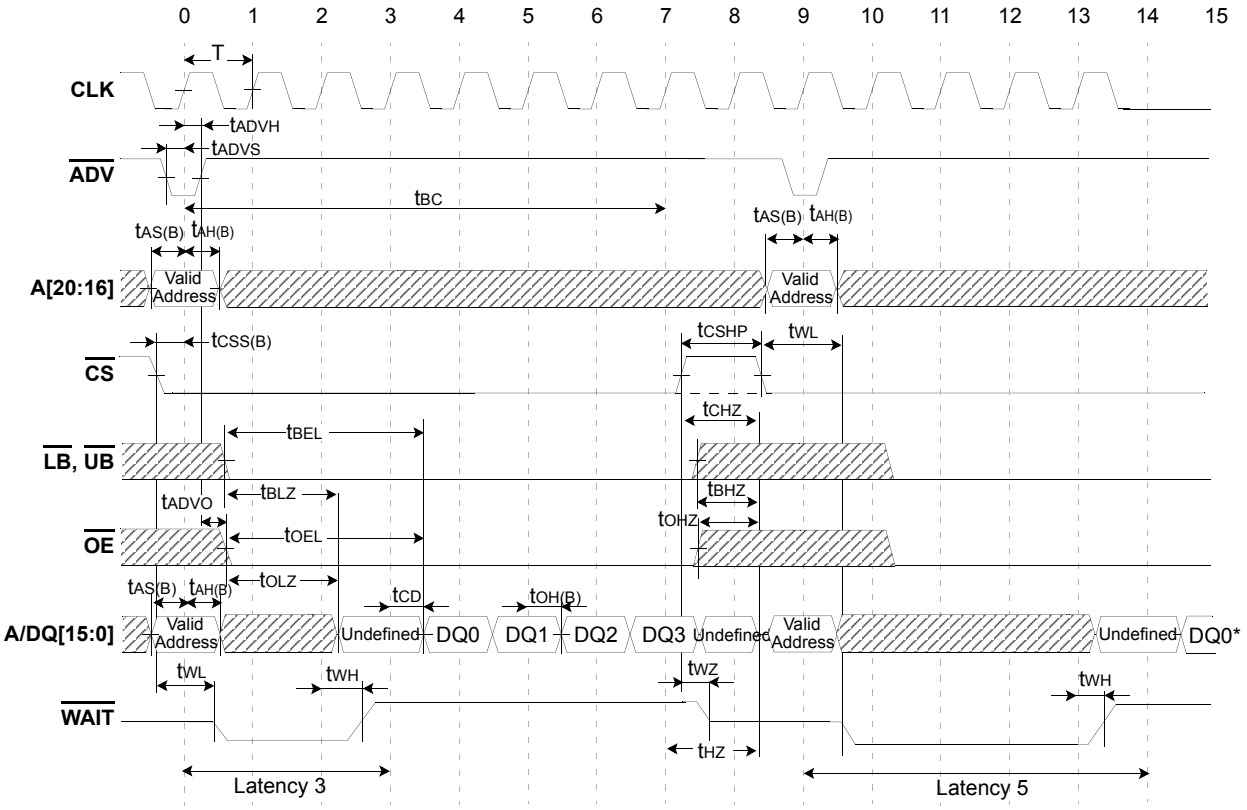
1. /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5μs)

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

Burst READ - Variable Latency

(PS=VIH, WE=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



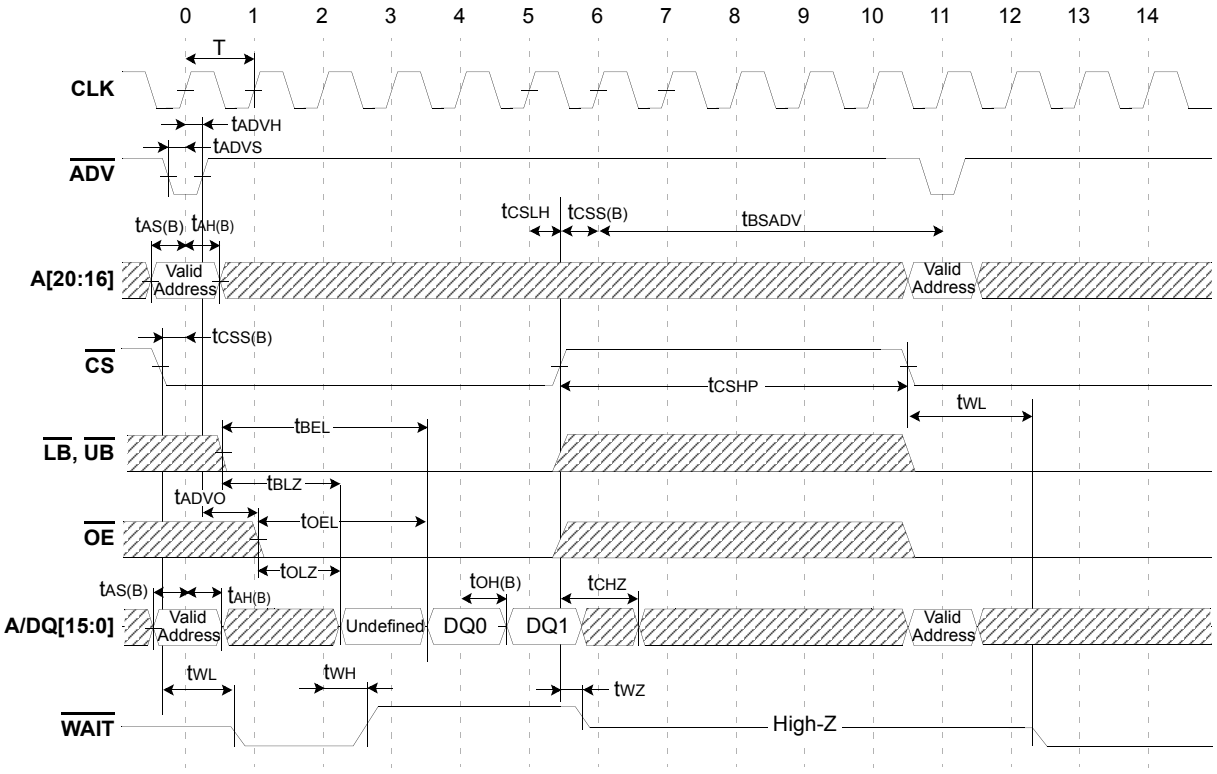
1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5μs).

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

Burst READ STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

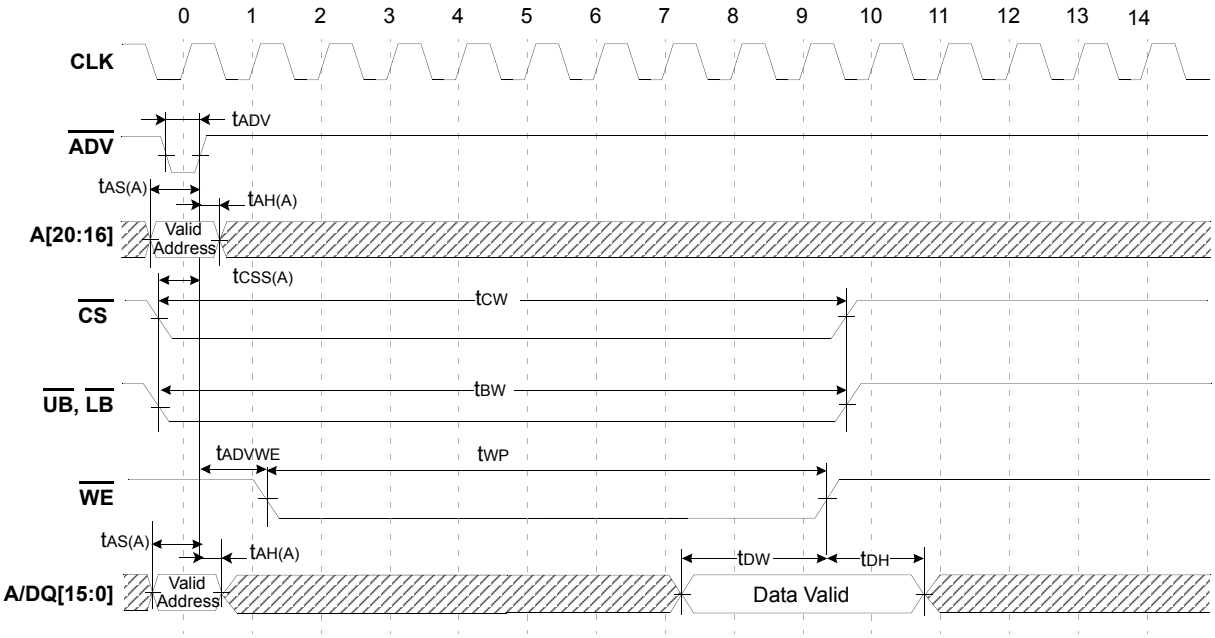


1. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Refresh can not be implemented when tBSADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBSADV.

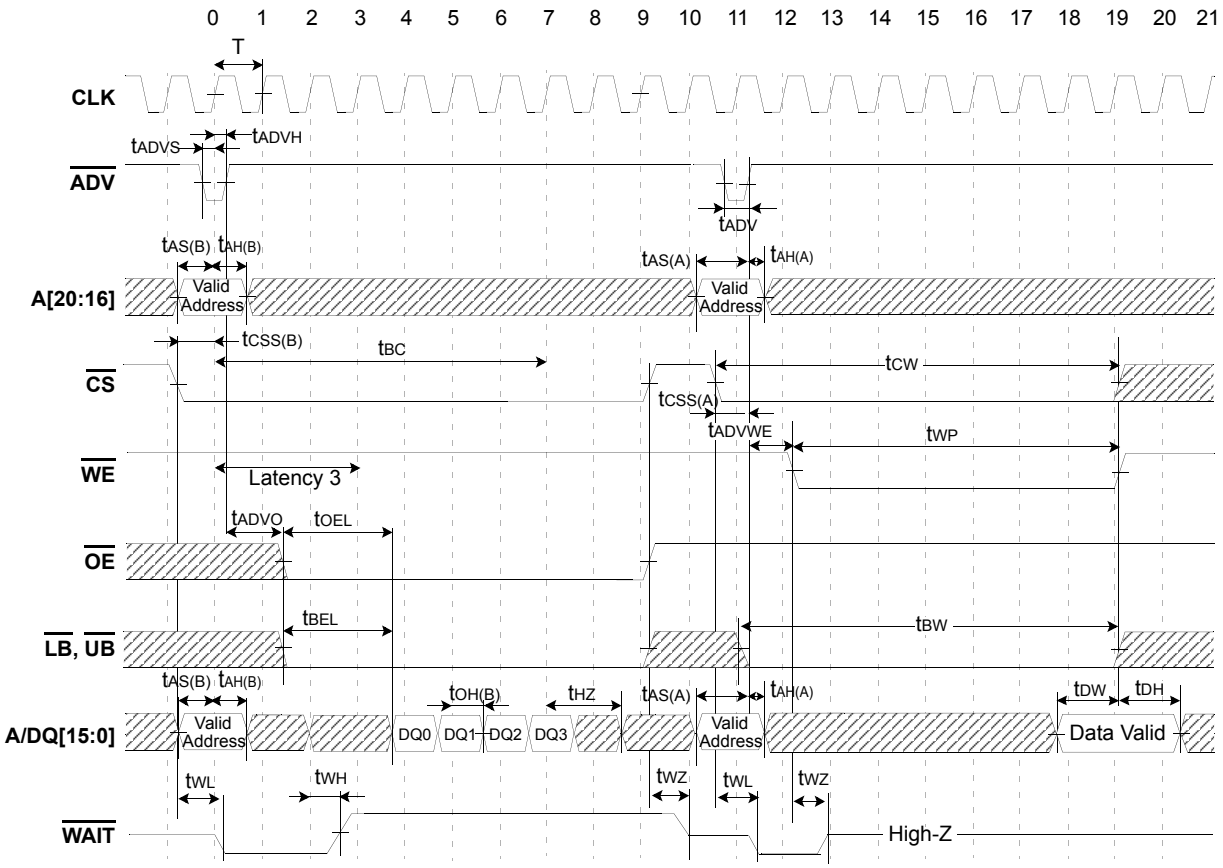
AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tBSADV	0	-	0	-	0	-	ns	tCD	-	11	-	9	-	7	ns
tCSLH	2	-	2	-	2	-	ns	tOH(B)	3	-	3	-	3	-	ns
tCSHP	5	-	5	-	5	-	ns	tCHZ	-	10	-	10	-	10	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tBLZ	5	-	5	-	5	-	ns	tWZ	-	10	-	10	-	10	ns
tOLZ	5	-	5	-	5	-	ns	tADVO	5	-	4	-	3	-	ns

Asynch. WRITE
(PS=VIH, OE=VIH, WAIT=High-Z)



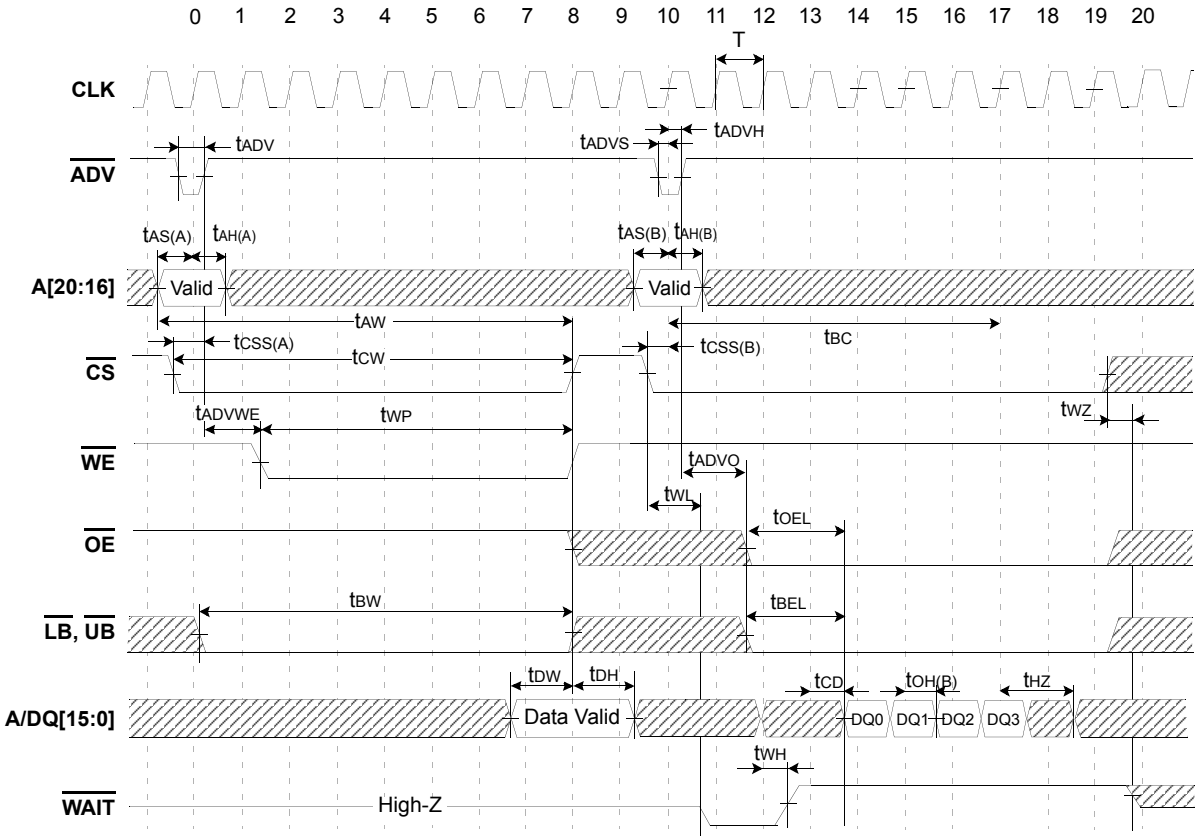
Burst READ followed by Asynch. WRITE
(PS=VIH, WAIT=High-Z, Variable Latency=3)



1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for word operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW}.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{BW} is measured from the $\overline{UB}$ and $\overline{LB}$ going low to the end of write.

Asynch. WRITE followed by Burst READ

(PS=VIH, Variable Latency=3,Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

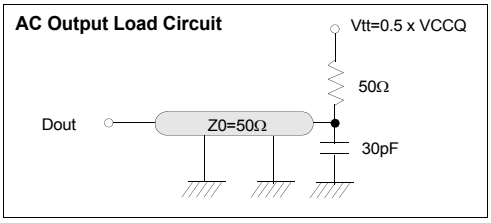


1. /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5μs)

MODE3. AC OPERATING CONDITIONS (SYNCH. READ / SYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CC}-0.2V
Input rising and falling time: 1ns
Input and output reference voltage: 0.5 x V_{CC}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -40°C~85°C



AC CHARACTERISTICS

Parameter List		Symbol	66MHz		80MHz		104MHz		Units
			Min	Max	Min	Max	Min	Max	
Burst Operation (Common)	Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
	Burst Cycle Time	t_{BC}	-	2500	-	2500	-	2500	ns
	Address Set-up Time to clock	$t_{AS(B)}$	5	-	4	-	3	-	ns
	Address Hold Time from clock	$t_{AH(B)}$	2	-	2	-	2	-	ns
	$\overline{ADV}$ Setup Time to clock	t_{ADVS}	5	-	4	-	3	-	ns
	$\overline{ADV}$ Hold Time from clock	t_{ADVH}	2	-	2	-	2	-	ns
	$\overline{CS}$ Setup Time to clock	$t_{CSS(B)}$	5	-	4	-	3	-	ns
	$\overline{CS}$ High to New $\overline{ADV}$ Low (Burst Stop)	t_{BSADV}	0	-	0	-	0	-	ns
	$\overline{CS}$ Low Hold Time from Clock(Burst Stop)	t_{CSLH}	2	-	2	-	2	-	ns
	$\overline{CS}$ High Pulse Width	t_{CSHP}	5	-	5	-	5	-	ns
	$\overline{CS}$ Low to $\overline{WAIT}$ Low	t_{WL}	-	7.5	-	7.5	-	7.5	ns
	Clock to $\overline{WAIT}$ High	t_{WH}	-	11	-	9	-	7	ns
	$\overline{CS}$ High to $\overline{WAIT}$ High-Z	t_{WZ}	-	10	-	10	-	10	ns
Burst Read Operation	$\overline{UB}$, $\overline{LB}$ Low to End of Latency Clock	t_{BEL}	20	-	20	-	20	-	ns
	$\overline{OE}$ Low to End of Latency Clock	t_{OEL}	20	-	20	-	20	-	ns
	$\overline{UB}$, $\overline{LB}$ Low to Low-Z Output	t_{BLZ}	5	-	5	-	5	-	ns
	$\overline{OE}$ Low to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	ns
	Clock Rising to Data Output	t_{CD}	-	11	-	9	-	7	ns
	Output Hold from clock	$t_{OH(B)}$	3	-	3	-	3	-	ns
	Burst End Clock to Output High-Z	t_{HZ}	-	10	-	10	-	10	ns
	$\overline{CS}$ High to Output High-Z	t_{CHZ}	-	10	-	10	-	10	ns
	$\overline{OE}$ High to Output High-Z	t_{OHZ}	-	10	-	10	-	10	ns
	$\overline{UB}$, $\overline{LB}$ High to Output High-Z	t_{BHZ}	-	10	-	10	-	10	ns
	ADV# high to OE# Low	t_{ADVO}	5	-	4	-	3	-	ns

1. Refresh can not be implemented when t_{BSADV} is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for t_{BSADV}.
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

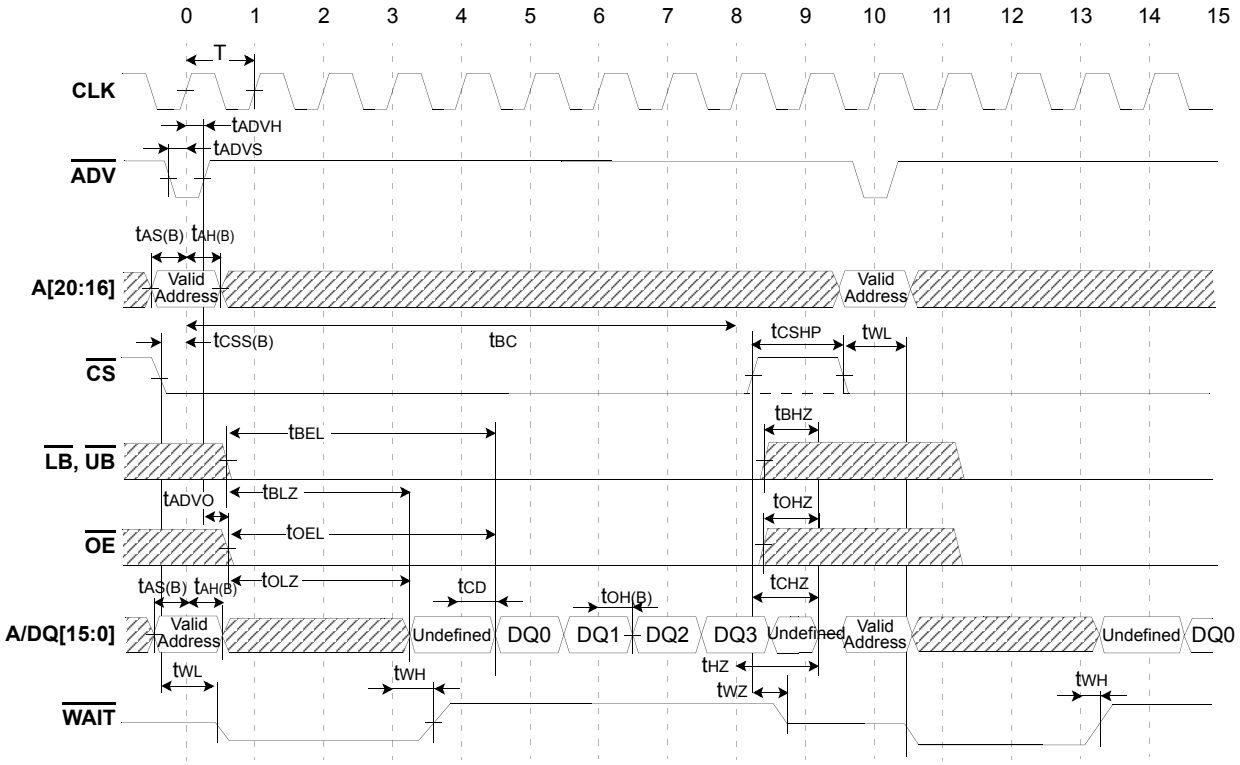
Burst Write Operation	$\overline{WE}$ Set-up Time to Clock	t_{WES}	5	-	4	-	3	-	ns
	$\overline{WE}$ Hold Time from Clock	t_{WEH}	2	-	2	-	2	-	ns
	$\overline{UB}$, $\overline{LB}$ Set-up Time to Clock	t_{BS}	5	-	4	-	3	-	ns
	Burst End clock to New $\overline{ADV}$ Low	t_{BEADV}	0	-	0	-	0	-	ns
	$\overline{UB}$, $\overline{LB}$ Hold Time from Clock	t_{BH}	2	-	2	-	2	-	ns
	Byte Masking Set-up Time to Clock	t_{BMS}	5	-	4	-	3	-	ns
	Byte Masking Hold Time from Clock	t_{BMH}	2	-	2	-	2	-	ns
	Write Data Set-up Time to Clock	t_{DS}	5	-	4	-	3	-	ns
	Write Data Hold Time from Clock	t_{DHC}	2	-	2	-	2	-	ns

1. Refresh can not be implemented when t_{BEADV} is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for t_{BEADV}.

TIMING WAVEFORMS (SYNCH. READ / SYNCH. WRITE)

Burst READ - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



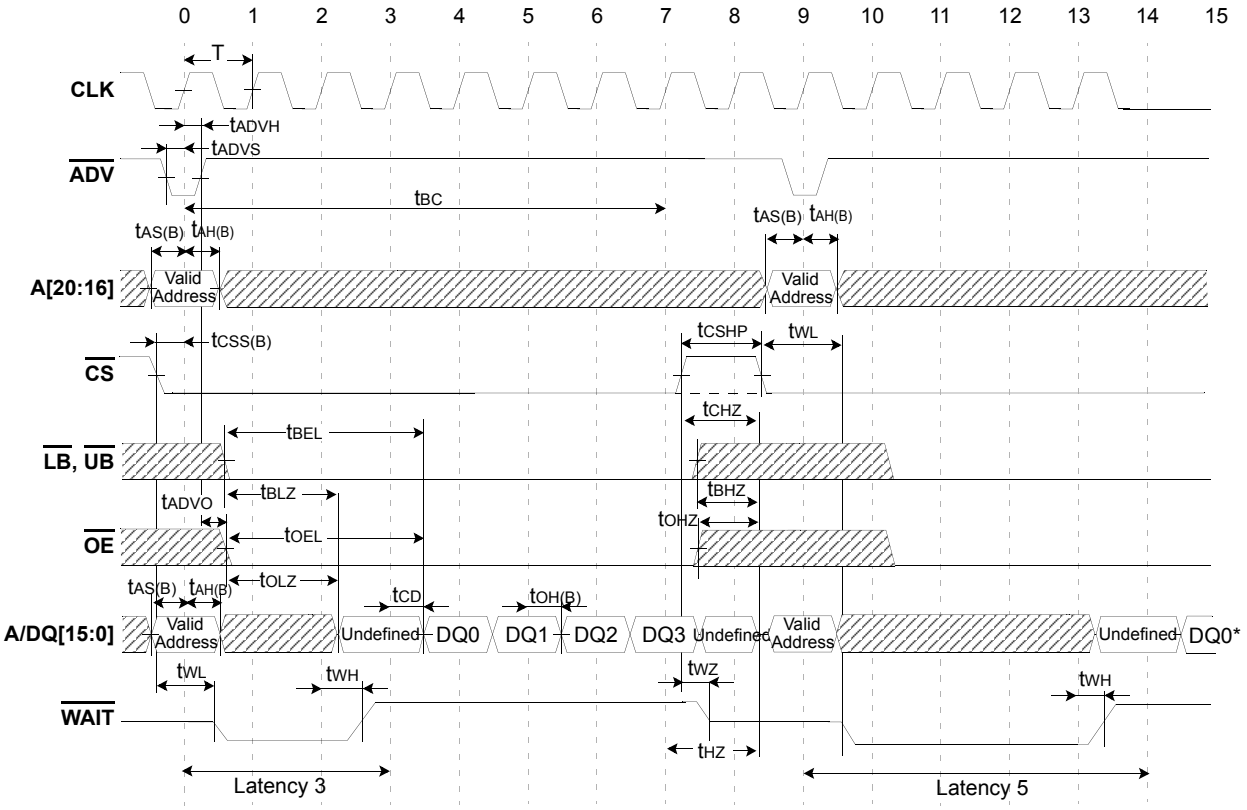
1. /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5μs)

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

Burst READ - Variable Latency

(PS=VIH, WE=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



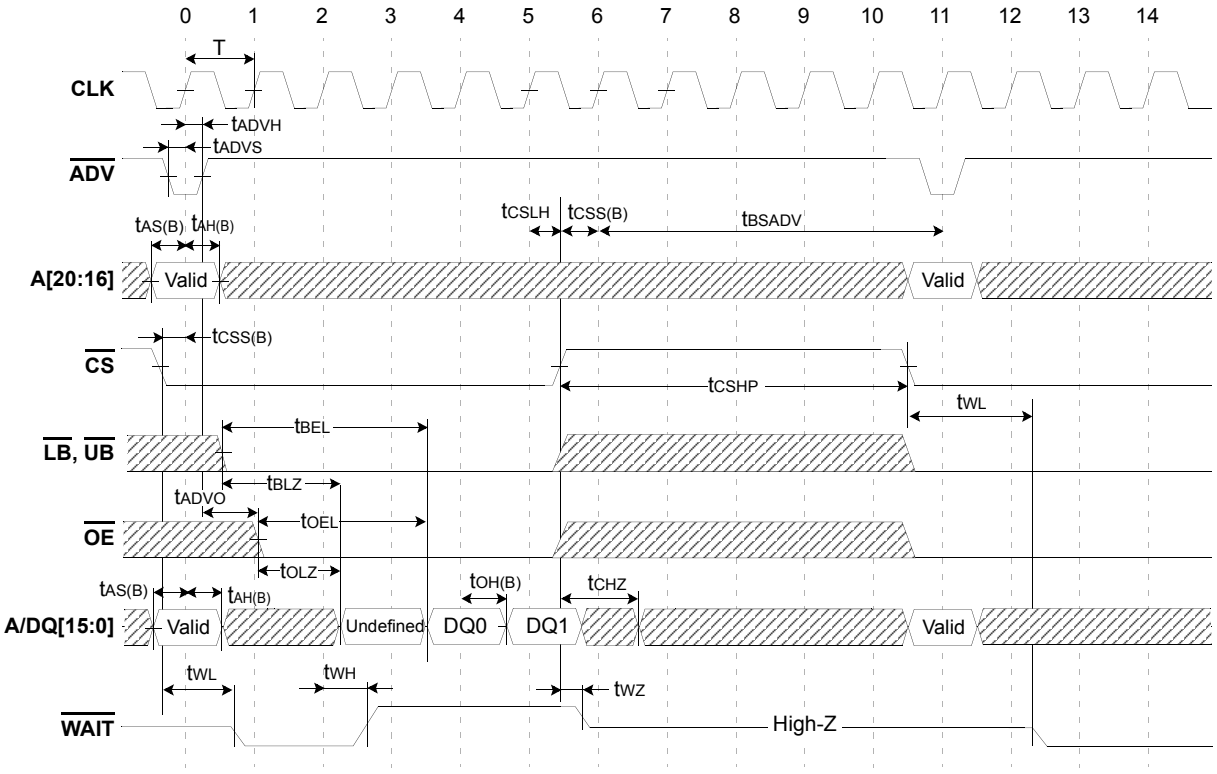
1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5μs).

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

Burst READ STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



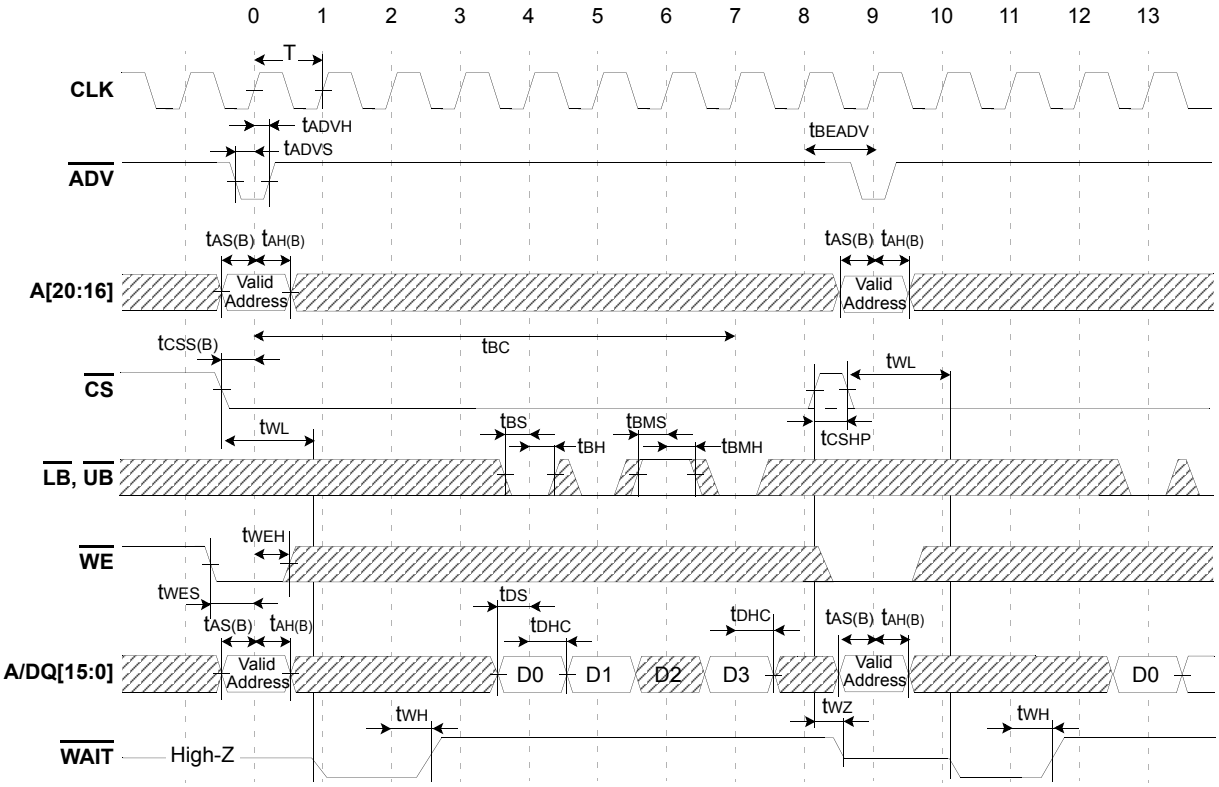
1. /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The data starts after set Latency from the last clock rising.
3. Refresh can not be implemented when tBSADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without $\overline{CS}$ toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBSADV.

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tBSADV	0	-	0	-	0	-	ns	tCD	-	11	-	9	-	7	ns
tCSLH	2	-	2	-	2	-	ns	tOH(B)	3	-	3	-	3	-	ns
tCSHP	5	-	5	-	5	-	ns	tCHZ	-	10	-	10	-	10	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tBLZ	5	-	5	-	5	-	ns	tWZ	-	10	-	10	-	10	ns
tOLZ	5	-	5	-	5	-	ns								

Burst WRITE

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



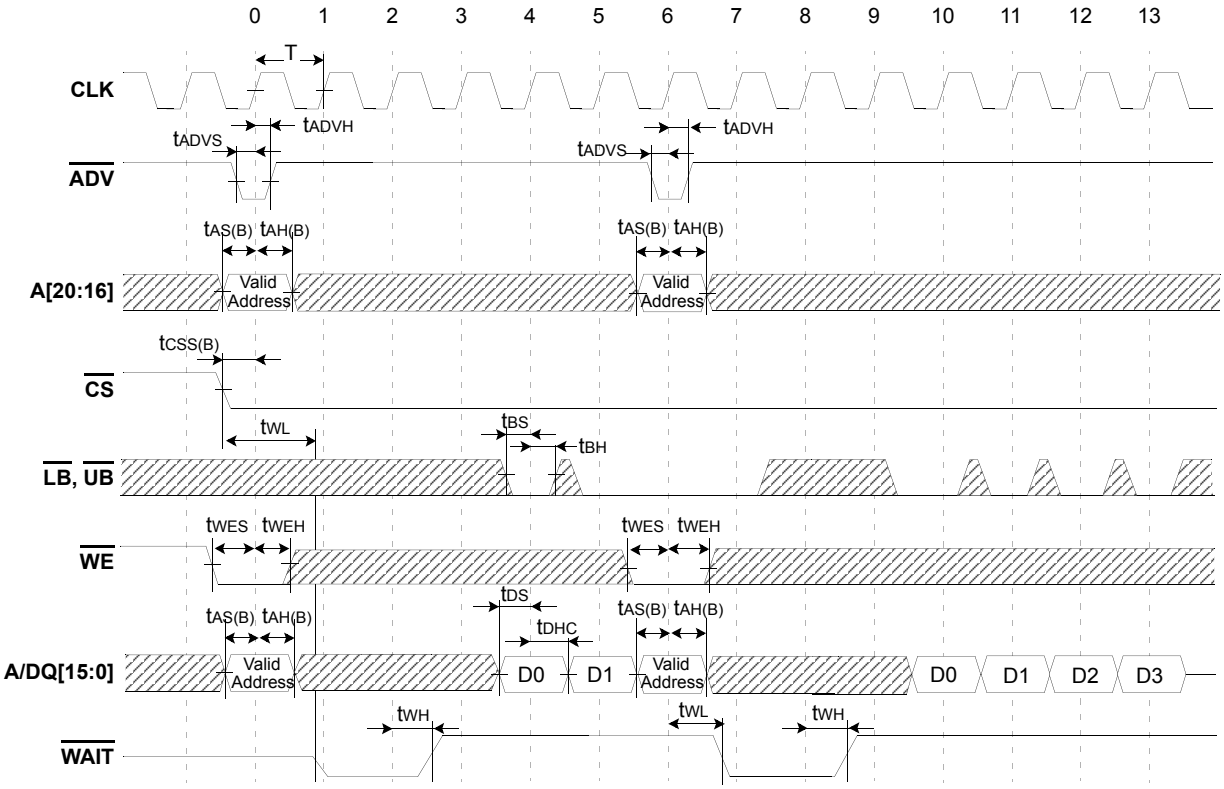
1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5μs)

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	3	-	3	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	tWZ	-	10	-	10	-	10	ns
tWES	5	-	4	-	3	-	ns								
tWEH	2	-	2	-	2	-	ns								

Burst WRITE (ADV PULSE Interrupt)

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



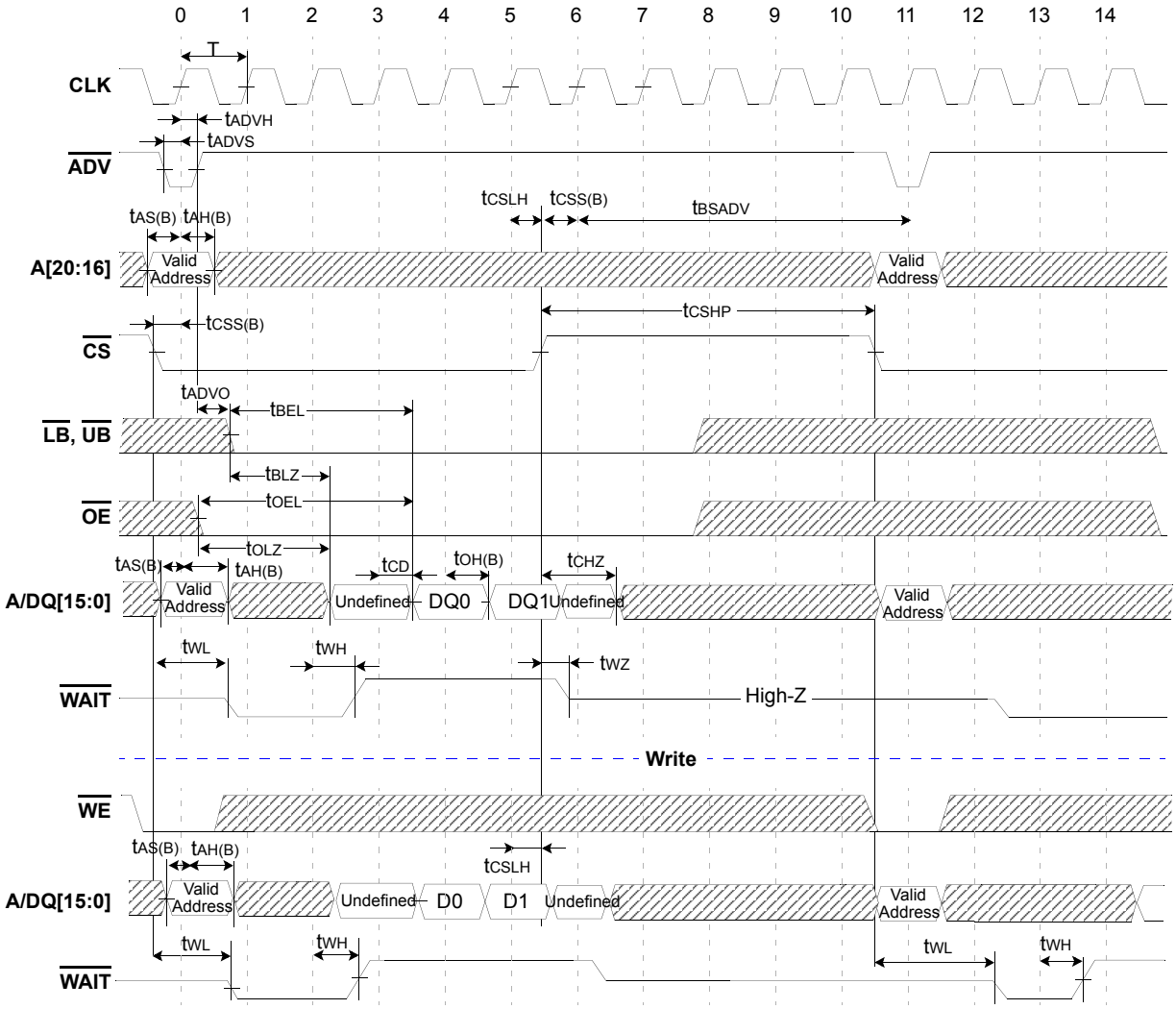
1. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Burst interrupt is allowable after the first data word written.

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	5	-	4	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	tWZ	-	10	-	10	-	10	ns
tWES	5	-	4	-	3	-	ns								
tWEH	2	-	2	-	2	-	ns								

Burst READ STOP & Burst WRITE STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



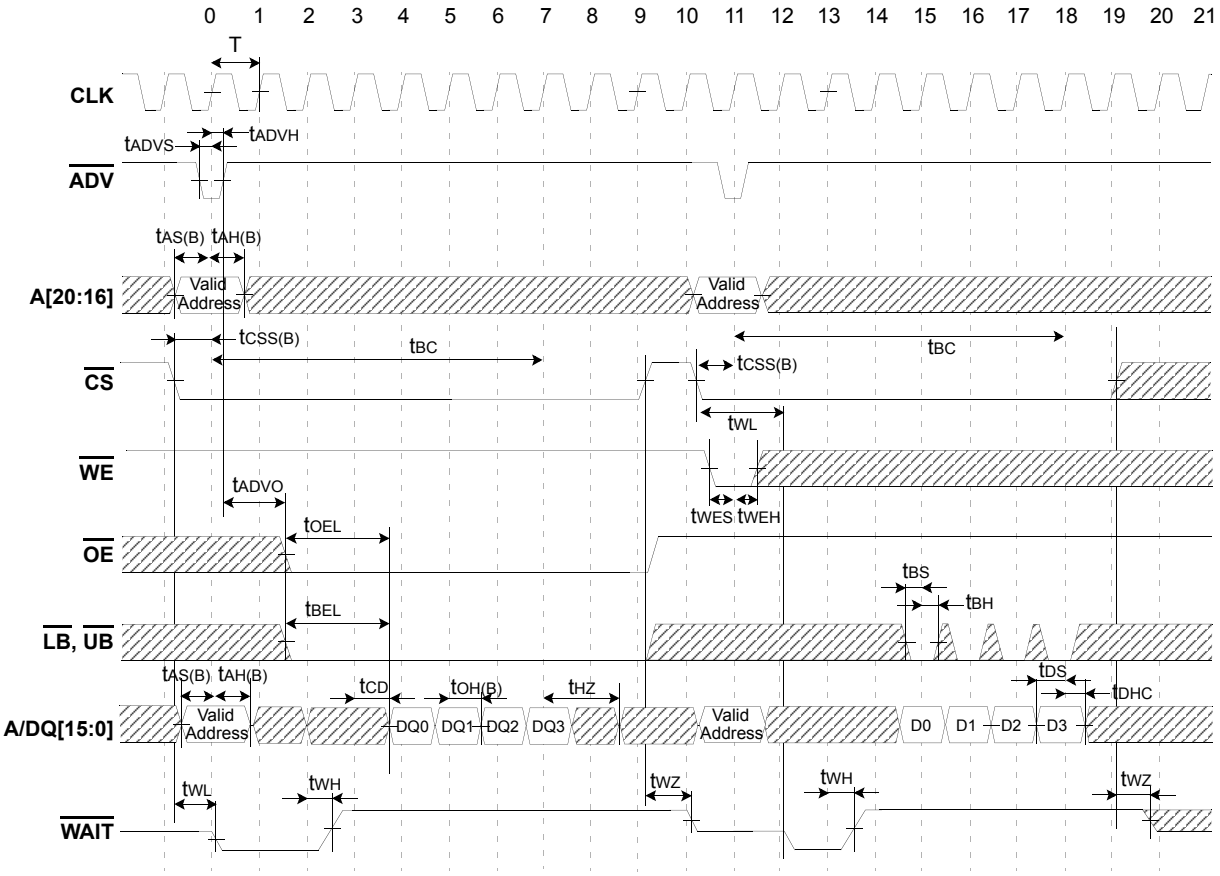
1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)

AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	5	-	4	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	tWZ	-	10	-	10	-	10	ns
tWES	5	-	4	-	3	-	ns	tBSADV	-	0	-	0	-	0	ns
tWEH	2	-	2	-	2	-	ns	tOH(B)	3	-	3	-	3	-	ns

Burst READ followed by Burst WRITE

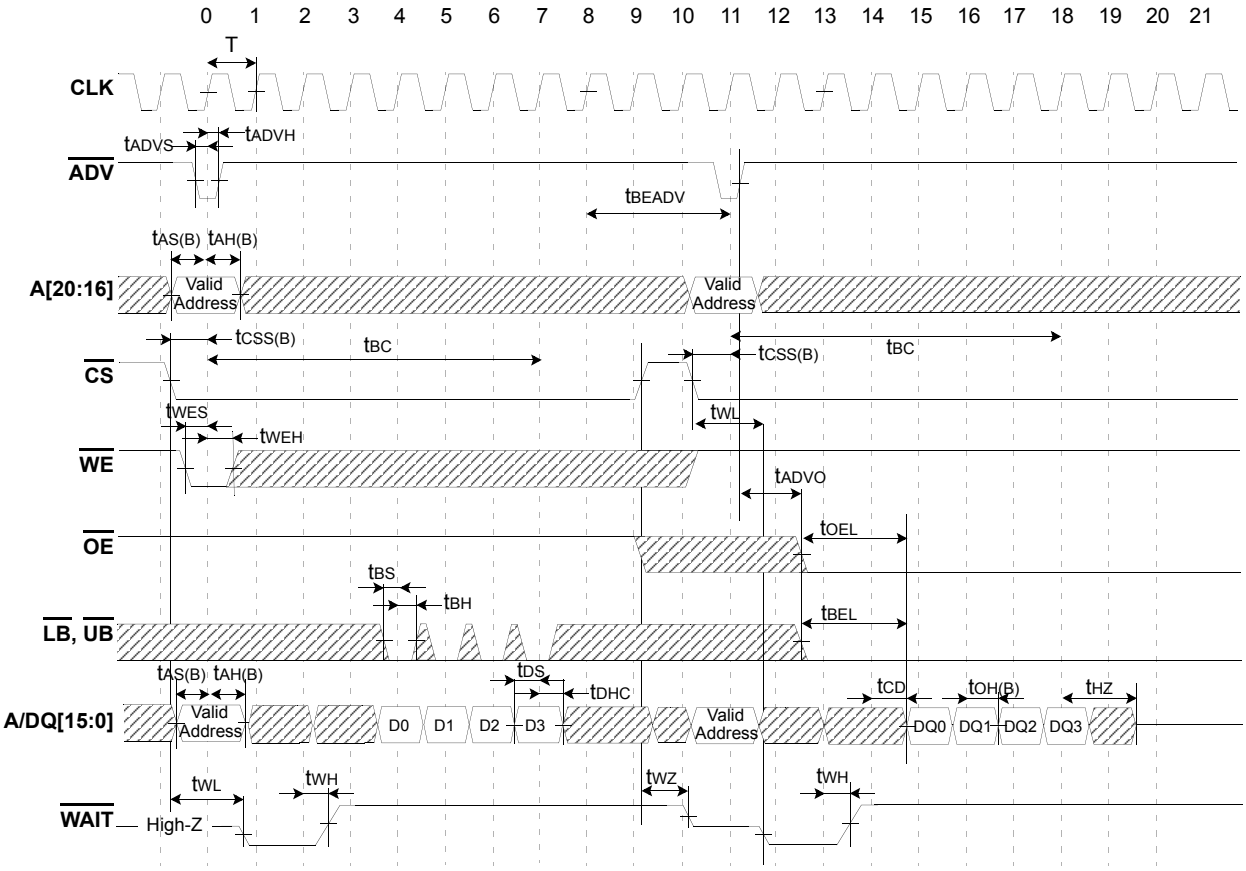
(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. /WAIT Low(tWL) : Data not available(driven by $\overline{CS}$ low going edge or $\overline{ADV}$ low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by $\overline{CS}$ high going edge)
2. Multiple clock risings are allowed during low $\overline{ADV}$ period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5μs)

Burst WRITE followed by Burst READ

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

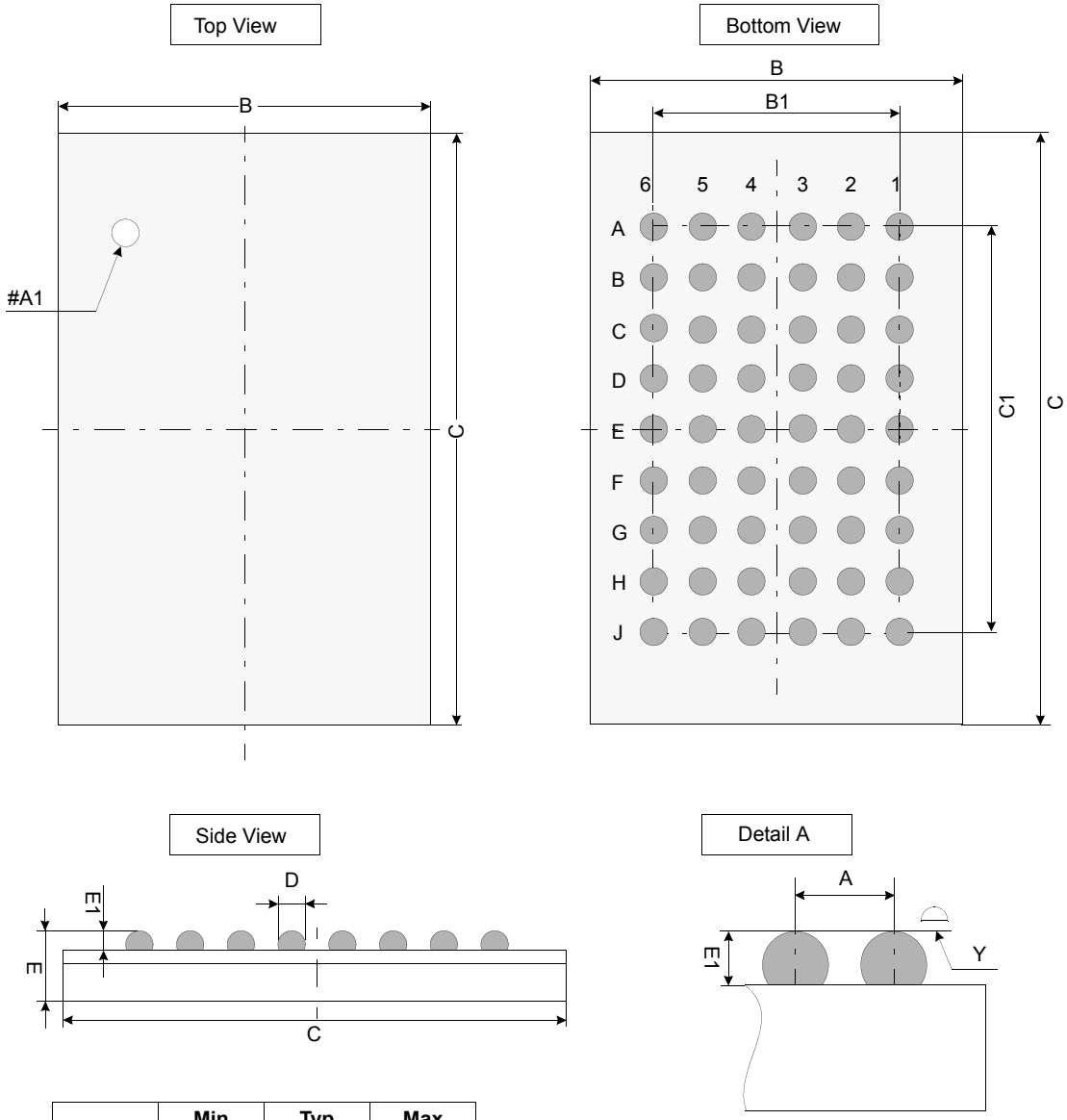


1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
   /WAIT High(tWH) : Data available(driven by Latency-1 clock)
   /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than (tBC)2.5μs.

PACKAGE DIMENSION

Unit: millimeters

54 BALL FINE PITCH BGA(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

Notes.

1. Ball counts: 54(9 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity