Overview

The Rambus® RIMM™ module is a general purpose high-performance memory subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The Rambus RIMM module consist of 128Mb/144Mb Direct Rambus DRAM devices. These are extremely high-speed CMOS DRAMs organized as 8M words by 16 or 18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz ,711MHz or 800MHz transfer rates while using conventional system and board design technologies. Direct RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10ns per 16 bytes).

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's 16-banks architecture supports up to four simultaneous transactions per device.

Features

- High speed 800,711 and 600 MHz RDRAM storage
- 184 edge connector pads with 1 mm pad spacing
- Maximum module PCB size: 133.5mm x 31.75mm x 1.37mm(5.21" x 1.25" x 0.05")
- Each RDRAM has 32 banks, for a total of 512, 384, 256, 192 or 128 banks on each 256MB, 192MB, 128MB, 96MB, or 64MB module respectively
- Gold plated edge connector pad contacts
- Serial Presence Detect(SPD) support
- Operates from a 2.5 volt supply (± 5%)
- Low power and powerdown self refresh modes
- Separate Row and Column buses for higher efficiency

Key Timing Parameters/Part Numbers

The following table lists the frequency and latency bins available from RIMM modules. An optional -LP designator is used to indicate low power modules.

Table 1: RIMM Module Frequency and Latency

Organization	I/O Freq. MHz	t rac (Row Access Time) ns
x16	600	53
x16	711	45
x16	800	45
x16	800	40
x18	600	53
x18	711	45
x18	800	45
x18	800	40

Form Factor

The Rambus RIMM modules are offered in a 184-pad 1mm edge connector pad pitch from factor suitable for either 184 or 168 contact RIMM connectors. The RIMM module is suitable for desktop and other system applications. Figure 1 shows an eight device Rambus RIMM module without heat spreader.

Rev. 1.0/Dec.99

Table 2: Module Pad Number and Signal Names

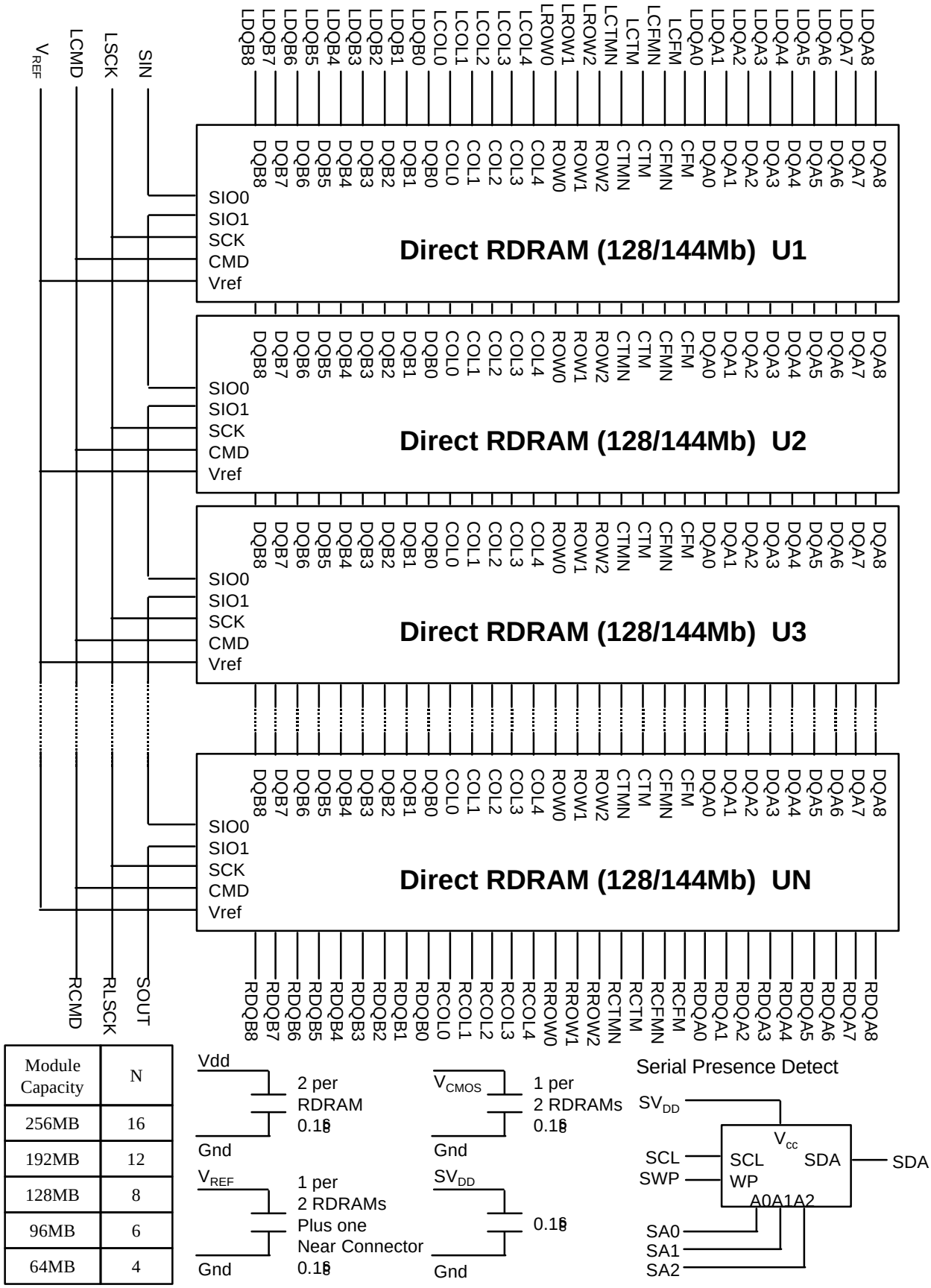
Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

Pin	Pin Name	Pin	Pin Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	B10	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	I	V_{CMOS}	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A20, B20, A22, B22, A24	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A14	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on x16 RDRAM devices.
LDQB8.. LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on x16 RDRAM devices.
LROW2.. LROW0	B16, A18, B18	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A34	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A16, B14, A38, B38, A40, B40, A77, B79			These pads are not connected. These 8 connector pads are reserved for future use.
NC	A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50			These pads are not connected. These 16connector pads art reserved for future use. The 168 contact RIMM connector does not connect to these PCB pads.
RCFM	B83	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Signal	Module Connector Pads	I/O	Type	Description
RCMD	B59	I	V_{CMOS}	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on x16 RDRAM devices.
RROW2.. RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A59	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B53	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B55	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	B57	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	A53	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A55	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O)
SIN	B36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58	I		Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.



Module Capacity	N
256MB	16
192MB	12
128MB	8
96MB	6
64MB	4

Note 1: Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.
Note 2: See Serial Presence Detection Specification for information on the SPD device and its contents

Figure 2: RIMM Module Functional Diagram

Absolute Maximum Ratings

Signal	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	- 0.3	V DD + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V DD + 1.0	V
T_{STORE}	Storage temperature	- 50	100	ºC

DC Recommended Electrical Conditions

Signal	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	V V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3	$0.5V_{CMOS}$ - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$ + 0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OL,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS} - 0.3		V
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	μA
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	μA
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	μA

a. The tale below shows the number of 128Mb or 144Mb RDRAM devices contained in a RIMM module of listed memory storage capacity

RIMM Module Capacity:	256MB	192MB	128MB	96MB	64MB
Number of 128Mb or 144Mb RDRAM devices:	16	12	8	6	4

RIMM Module Current Profile

I_{DD}	RIMM Module Capacity: No. of 128/144Mb RDRAMs:		256/288MB 16	192/216MB 12	128/144MB 8	96/108MB 6	64/72MB 4	Unit
	RIMM module power conditions[a]	Freq.	**Max**	**Max**	**Max**	**Max**	**Max**	
I_{DD1}	One RDRAM in Read[b], balance in NAP mode	800	690/658	675/641	660/625	652/616	645/608	mA
		711	633/605	618/589	603/572	596/564	589/556	
		600	556/532	541/516	527/500	520/492	512/484	
I_{DD2}	One RDRAM in Read[b], balance in Standby mode	800	2302/2354	1857/1885	1412/1416	1189/1181	967/947	mA
		711	2142/2199	1725/1757	1307/1316	1099/1095	890/874	
		600	1928/2005	1547/1596	1167/1188	977/983	787/779	
I_{DD3}	One RDRAM in Read[b], balance in Active mode	800	3506/3560	2740/2769	1974/1979	1591/1583	1208/1188	mA
		711	3222/3318	2517/2578	1811/1838	1459/1468	1106/1098	
		600	2889/3006	2253/2331	1616/1655	1297/1317	979/979	
I_{DD4}	One RDRAM in Write, balance in NAP mode	800	794/766	778/750	763/733	756/724	748/716	mA
		711	765/705	750/688	735/672	728/663	720/655	
		600	668/625	654/609	639/594	632/586	625/578	
I_{DD5}	One RDRAM in Read, balance in Standby mode	800	2405/2462	1960/1993	1515/1524	1293/1290	1070/1055	mA
		711	2273/2298	1856/1857	1439/1415	1230/1195	1022/974	
		600	2040/2098	1660/1690	1280/1281	1090/1077	900/872	
I_{DD6}	One RDRAM in Read, balance in Active mode	800	3609/3668	2843/2878	2077/2087	1694/1692	1311/1296	mA
		711	3353/3418	2648/2678	1943/1938	1590/1568	1238/1198	
		600	3002/3100	2365/2424	1729/1748	1410/1410	1092/1073	

a. Specifications in this table are maximum guidelines. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Please refer to specific RIMM module vendor data sheets for additional information. Max current computed for x18 144Mb RDRAMs. X16 128Mb RDRAMs use 8mA less current per RDRAM in Read.

b. I/O current is a function of the % of 1's, to add I/O power for 50% 1's for a X16 need to add 257mA or 290mA for X18ECC module for the following : V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.

AC Electrical Specifications

Symbol	Parameter and Condition	Min	Typ	Max	Unit
Z	Module Impedance	25.2	28	30.8	Ω
T_{PD}	Average clock delay form finger to finger of all RSL clock nets (CTMN, CFM, and CFMN)	-		See Table[a]	ns
Δ T_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}[b,c] for 4, 6, 8, and 12 device modules	-21		21	ps
	Propagation delay variation of RSL signals with respect to T_{PD}[b,c] for 16 device modules	-24		24	ps
Δ $T_{PD-CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay[b]	-100		100	ps
V_{N} /V_{IN}	Attenuation Limit			See Table[a]	%
V_{XF} /V_{IN}	Forward crosstalk coefficient (300ps input rise time 20%-80%)			See Table[a]	%
V_{XB} /V_{IN}	Backward crosstalk coefficient (300ps input rise time 20%-80%)			See Table[a]	%

a. Table below lists parameters and specifications for different storage capacity RIMM Modules that use 128Mb or 144Mb RDRAM devices.
b. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN)
c. If the RIMM module meets the following specification , then it is compliant to the specification. If the RIMM module does not meet these specification. Then the specification can be adjusted by the " Adjusted Δ T_{PD} Specification " table

Adjusted Δ T_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Asolute Min/Max		Unit
Δ T_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 4,6 and 8 device modules	+/-[17+(18*N*Δ Z0)][a]	-30	30	ns
	Propagation delay variation of RSL signals with respect to T_{PD} for 12 device modules	+/-[20+(18*N*Δ Z0)][a]	-40	40	ps
	Propagation delay variation of RSL signals with respect to T_{PD} for 16 device modules	+/-[24+(18*N*Δ Z0)][a]	-50	50	ps

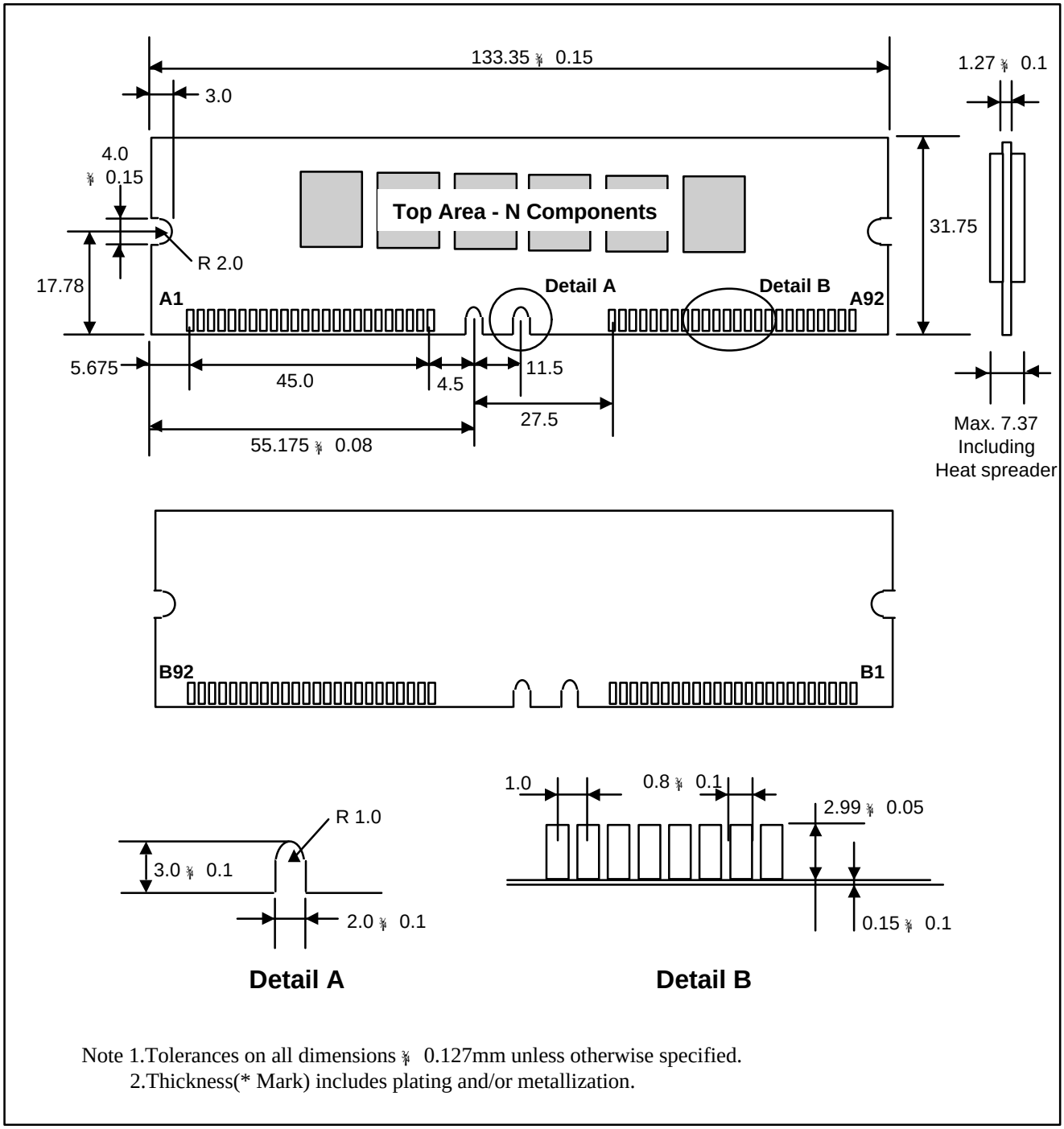
a. Where : N =Number of RDRAM devices installed on the RIMM module
Δ Z0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

AC Electrical Specifications for RIMM Modules

Symbol	RIMM Module Capacity: / No. of 128/144Mb RDRAMs:	256/288MB 16	192/216MB 12	128/144MB 8	96/108MB 6	64/72MB 4	Unit
	Parameter and Condition for -800 & -600 RIMM Module	**Max**	**Max**	**Max**	**Max**	**Max**	
T_{PD}	Propagation Delay, all RSL signals -800,-711	2.06	1.76	1.50	1.4	1.25	ns
	Propagation Delay, all RSL signals -600	2.10	1.76	1.60	1.40	1.25	ns
$V_{\square}/V_{IN}$	Attenuation Limit -800,-711	25	20	16	14	12	%
	Attenuation Limit -600	21	18	10	9	8	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%) -800,-711	8	6	4	3	2	%
	Forward crosstalk coefficient (300ps input rise time @ 20%-80%) -600	8	6	4	3	2	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%) -800,-711	2.5	2.3	2.0	1.8	1.5	%
	Backward crosstalk coefficient (300ps input rise time @ 20%-80%) -600	2.5	2.3	2.0	1.8	1.5	%
R_{DC}	DC Resistance Limit -800,-711	1.2	1.1	0.8	0.7	0.6	§
	DC Resistance Limit -600	1.2	1.1	0.8	0.7	0.6	§

Physical Dimensions

The following defines the RIMM module dimensions. All units are in millimeters. The height of the module is 31.75mm.



Note 1.Tolerances on all dimensions ± 0.127mm unless otherwise specified.
2.Thickness(* Mark) includes plating and/or metallization.

Figure 3: RIMM Module PCB Physical Description

Module Weight

The maximum RIMM Module weight is 75gm(2.625oz) with a center of mass 35mm (1.378 in.) upwards from bottom edge.

Serial Presence Detect Contents

The following table lists the contents of the serial presence detect device.

Byte (Dec)	Description	Option	Entry	Symbol	Value (HEX)
0	SPD revision level		2		02
1	Total number of bytes in the SPD		256		08
2	Device type		DRDRAM		01
3	Module type		RIMM		01
4	Row address bits, Column address bits		9,6		96
5	Bank address bits and byte	72M	16d (4 bank bits)		84
		128/144M	32d (5 bank bits)		C5
6	Refresh Bank Bits	72M	9,6		04
		128/144M	5		05
7	t_{REF} - Refresh interval		32	t_{REF}	20
8	Protocol version		2		02
9	Miscellaneous device configuration field	-LP	1 t_{SCK}	$t_{DQS,Min}$	-
		no -LP			01
		-LP S28IECO			-
		no -LP S28IECO			05
10	$t_{RP-R,Min}$	-40-800	8cycles	$t_{RP-R,Min}$	08
		-45-800	8cycles	$t_{RP-R,Min}$	08
		-45-711	8cycles	$t_{RP-R,Min}$	08
		-53-600	8cycles	$t_{RP-R,Min}$	08
11	$t_{RAS-R,Min}$	-40-800	20cycles	$t_{RAS-R,Min}$	14
		-45-800	20cycles	$t_{RAS-R,Min}$	14
		-45-711	20cycles	$t_{RAS-R,Min}$	14
		-53-600	20cycles	$t_{RAS-R,Min}$	14
12	$t_{RCD-R,Min}$	-40-800	8cycles	$t_{RCD-R,Min}$	08
		-45-800	10cycles	$t_{RCD-R,Min}$	0A
		-45-711	8cycles	$t_{RCD-R,Min}$	08
		-53-600	8cycles	$t_{RCD-R,Min}$	08
13	$t_{RR-R,Min}$	-40-800	8cycles	$t_{RR-R,Min}$	08
		-45-800	8cycles	$t_{RR-R,Min}$	08
		-45-711	8cycles	$t_{RR-R,Min}$	08
		-53-600	8cycles	$t_{RR-R,Min}$	08

Byte (Dec)	Description	Option	Entry	Symbol	Value (HEX)
14	$t_{PP-R,Min}$	-40-800	8cycles	$t_{PP-R,Min}$	08
		-45-800	8cycles	$t_{PP-R,Min}$	08
		-45-711	8cycles	$t_{PP-R,Min}$	08
		-53-600	8cycles	$t_{PP-R,Min}$	08
15	Min t_{CYCLE} for range A	-40-800	2.50 ns	t_{CYCLE}	13
		-45-800	2.50 ns	t_{CYCLE}	13
		-45-711	2.80 ns	t_{CYCLE}	15
		-53-600	3.33 ns	t_{CYCLE}	1A
16	Max t_{CYCLE} for range A	-40-800	3.83 ns	t_{CYCLE}	1E
		-45-800	3.83 ns	t_{CYCLE}	1E
		-45-711	3.83 ns	t_{CYCLE}	1E
		-53-600	3.83 ns	t_{CYCLE}	1E
17	t_{CDLY} range for range A	-40-800	5 - 9	t_{CYCLE}	59
		-45-800	5 - 9	t_{CYCLE}	59
		-45-711	5 - 9	t_{CYCLE}	59
		-53-600	5 - 9	t_{CYCLE}	59
18	t_{CLS} and t_{CAS} range for range A		$2t_{CYCLE}$ for t_{CYCLE} & t_{CYCLE}	t_{CYCLE}	AA
19	Min t_{CYCLE} for range B		0	Reserved	00
20	Max t_{CYCLE} for range B		0	Reserved	00
21	t_{CDLY} range for range B		0	Reserved	00
22	t_{CLS} and t_{CAS} range for range B		0	Reserved	00
23	Min t_{CYCLE} for range C		0	Reserved	00
24	Max t_{CYCLE} for range C		0	Reserved	00
25	t_{CDLY} range for range C		0	Reserved	00
26	t_{CLS} and t_{CAS} range for range C		0	Reserved	00
27	Min t_{CYCLE} for range D		0	Reserved	00
28	Max t_{CYCLE} for range D		0	Reserved	00
29	t_{CDLY} range for range D		0	Reserved	00
30	t_{CLS} and t_{CAS} range for range D		0	Reserved	00
31	$t_{PDNXA,Max}$		4 §	$t_{PDNXA,Max}$	04
32	$t_{PDNXB,Max}$		9000 cylces	$t_{PDNXB,Max}$	8D
33	$t_{NAPXA,Max}$		50 ns	$t_{NAPXA,Max}$	32
34	$t_{NAPXB,Max}$		40 ns	$t_{NAPXB,Max}$	28
35	f_{IMIN}[11:8], f_{IMAX}[11:8]	-800	261MHz, 400MHz	f_{IMIN} f_{IMAX}	11
		-711	261MHz, 357MHz		11
		-600	261MHz, 300MHz		11

Byte (Dec)	Description	Option	Entry	Symbol	Value (HEX)
36	f_{IMIN} [7:0]	-800	261MHz	f_{IMIN}	05
		-711	261MHz		05
		-600	261MHz		05
37	f_{IMAX} [7:0]	-800	400MHz	f_{IMAX}	90
		-711	357MHz		65
		-600	300MHz		2C
38	Reserved				00
39	Max. time between Current Control		100 ms	$t_{CCTRL,MAX}$	64
40	Max. time between Temp. Calibration		100 ms	$t_{TEMP,MAX}$	64
41	Max. time between Temp. Calibration Enable and Command		150 t_{CYCLE}	$t_{TCEN,MIN}$	96
42	Maximum RAS to Precharge time		64 t_{CYCLE}	$t_{RAS-R, MAX}$	40
43	Maximum time that a Device can stay in Nap Mode		10 t_{CYCLE}	$t_{NLIMIT, MAX}$	0A
44	ACTREFPT, PCHREFPT		6, 6 t_{CYCLE}	t_{CYCLE}	66
45	CPCHREFPT_DC, RDREFPT_DC		5, 5 t_{CYCLE}	t_{CYCLE}	55
46	RETREFPT_DC, WRREFPT_DC		5, 13 t_{CYCLE}	t_{CYCLE}	5D
47~49	Reserved				00
50	f_{RAS}[11:8]	-800	01	f_{RAS}	01
		-711	01		01
		-600	01		01
51	f_{RAS}[7:0]	-800	90	f_{RAS}	90
		-711	65		65
		-600	2C		2C
52	PMAX, HI, PMAX, LO, Tj (assumes active-write current is max, Tj = 100)	-800	0,0,(100-64)	É	24
		-711	0,0,(100-64)		24
		-600	0,0,(100-64)		24
53	Heat Spreader, Tplate (assumes heat spreader present, Tplate = 100)	-800	1,(100-64)	É	A4
		-711	1,(100-64)		A4
		-600	1,(100-64)		A4
54	PSTBY,HI		TBD	mA	-
55	PACTI,HI		TBD	mA	-
56	PACTRW,HI		TBD	mA	-
57	PSTBY,LO		TBD	mA	-
58	PACTI,LO		TBD	mA	-
59	PACTRW,LO		TBD	mA	-
60	PNAP		TBD	mA	-
61	PRESA		Reserved	-	-

Byte (Dec)	Description	Option	Entry	Symbol	Value (HEX)
62	PRESB		Reserved	-	-
63	Checksum for locations 0 - 62		TBD	-	-
64 - 71	Manufacturer ID code		TBD	-	-
72	Module manufacturing location		TBD	-	-
73 - 90	Module part number		TBD	-	-
91 - 92	Module revision code		TBD	-	-
93	Module Manufacturing Year		TBD	-	-
94	Module manufacturing week		TBD	-	-
95 - 98	Module serial number		TBD	-	-
99	Number of devices on module	4D	4	Ea	04
		6D	6		06
		8D	8		08
		12D	12		0C
		16D	16		10
100	Number of devices on module	x16	16	Bit	10
		x18	18		12
101	Device enables	4D	All 4	Bit	0F
		6D	All 6		3F
		8D	All 8		FF
		12D	All 16		FF
		16D	All 16		FF
102	Device enables	4D	-	Bit	00
		6D	-		00
		8D	-		00
103~104	Device Enables		-	Bit	00
105	Module Vdd, Module Voltage Interface Level		2.5V, 1.8V	V_{DD}, V_{TERM}	10
106	Module V_{DD} tolerance		5% DC, 2% AC		52
107-113	Reserved				
114	CDLY0/1 for tCDLY = 3		-	t_{CYCLE}	00
115	CDLY0/1 for tCDLY = 4		2/0	t_{CYCLE}	20
116	CDLY0/1 for tCDLY = 5		3/0	t_{CYCLE}	30
117	CDLY0/1 for tCDLY = 6		3/1	t_{CYCLE}	31
118	CDLY0/1 for tCDLY = 7		3/2	t_{CYCLE}	32
119	CDLY0/1 for tCDLY = 8		4/2	t_{CYCLE}	42
120	CDLY0/1 for tCDLY = 9		5/2	t_{CYCLE}	52

Byte (Dec)	Description	Option	Entry	Symbol	Value (HEX)
121	CDLY0/1 for tCDLY = 10		-	t_{CYCLE}	00
122	CDLY0/1 for tCDLY = 11		-	t_{CYCLE}	00
123	CDLY0/1 for tCDLY = 12		-	t_{CYCLE}	00
124	CDLY0/1 for tCDLY = 13		-	t_{CYCLE}	00
125	CDLY0/1 for tCDLY = 14		-	t_{CYCLE}	00
126	CDLY0/1 for tCDLY = 15		-	t_{CYCLE}	00
127	Checksum for bytes 99 - 126		TBD	TBD	Undefined
128+	Open for Customer Use		-	-	Undefined

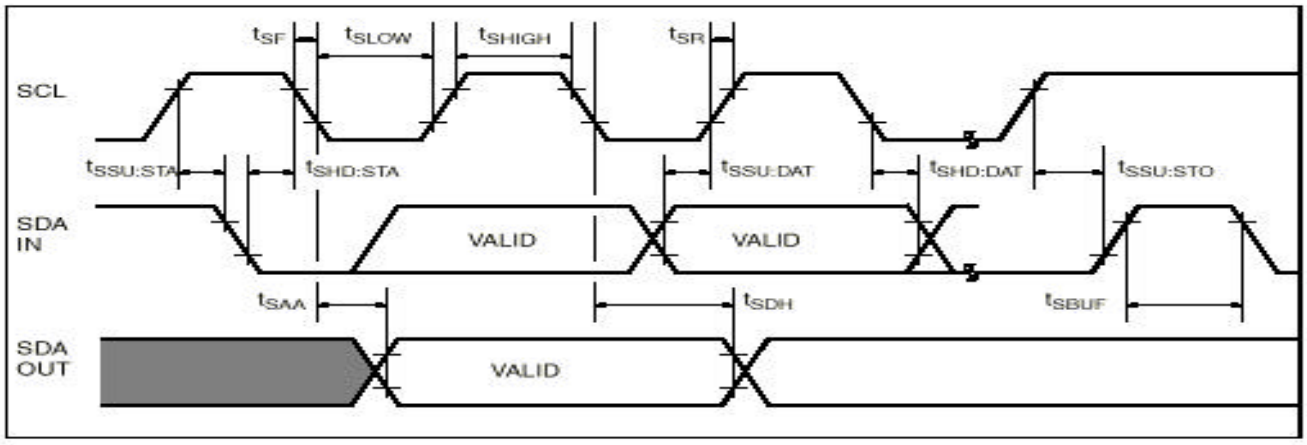
EEPROM Component AC and DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
SV_{DD}	power supply		2.2	3.6	V
I_{SVdd}	Active power supply current	f_{SCL} = 100 KHz		5.0	mA
I_{SVdd1}	standby current	V_{IN} = GND or SV_{DD}		100	μA
I_{SLI}	Input leakage current	V_{IN} = GND or SV_{DD}		10	μA
I_{SLO}	Output leakage current	V_{OUT} = GND or SV_{DD}		10	μA
V_{SIL}	Input Low Voltage		-0.3	SV_{DD} x 0.3	V
V_{SIH}	Input High Voltage		SV_{DD} x 0.7	SV_{DD} + 0.3	V
V_{SOL}	Output Low Voltage	I_{SOL} = 3.0 mA		0.4	V

EEPROM Component AC Timing Parameters

Symbol	Parameter and Conditions	Min	Max	Unit
f_{SCL}	SCL frequency		100	KHz
T_1	Noise suppression time constant for SCL, SDA		100	ns
t_{SAA}	SCL Low to SDA Data Out Valid	0.3	0.7	μs
t_{SBUF}	Time bus must be free before a new transmission can start	6.7		μs
$t_{SHD:STA}$	Start Condition Hold Time	4.5		μs
t_{SLOW}	Clock Low Time	6.7		μs
t_{SHIGH}	Clock High Time	4.5		μs
$t_{SSU:STA}$	Start Condition Setup Time	6.7		μs
$t_{SHD:DAT}$	Data In Hold Time	0		μs
$t_{SSU:DAT}$	Data In Setup Time	500		ns
t_{SR}	SDA and SCL Rise Time		1	μs
t_{SF}	SDA and SCL Fall Time		300	ns
$t_{SSU:STO}$	Stop Condition Setup Time	6.7		μs
t_{SDH}	Data Out Hold Time	300		ns
t_{SWR}	EEPROM Write Cycle Time		15	ms

SPD Timing Diagram



Direct RDRAM Module Ordering Information

HYUNDAI MODULE

Component Group

R1 : 128Mb/144Mb D-RDRAM
R2 : 256Mb/288Mb D-RDRAM
R5 : 512Mb/576Mb D-RDRAM

Power Supply and Interface

None : 2.5V
W : 1.8V

Memory DEPTH

32 : 32M , 48 : 48M
64 : 64M , 96 : 96M
128 : 128M , 256 : 256M

Module Type

None : 184Pin RIMM
M : SO RIMM

Data Width

16 : x16 (Non ECC)
18 : x18 (ECC)

Speed*

53 : 53ns
50 : 50ns
45 : 45ns
40 : 40ns

I/O Frequency

6 : 600MHz
7 : 711MHz
8 : 800MHz

Module Revision

None : ORIGINAL
M : FIRST
N : SECOND

Die Generation

Ichon		Cheongju	
None	: 1st Gen.	H	: 1st Gen.
A	: 2nd Gen.	HA	: 2nd Gen.
B	: 3rd Gen.	HB	: 3rd Gen.
C	: 4th Gen.	HC	: 4th Gen.

* SPEED = t_{rac} : Row Access Time

HYUNDAI
MicroElectronics