2048K x 32 Static RAM CMOS, High Speed Module

Features

- 2048K x 32 bit CMOS Static
- Random Access Memory
  - Access Times: 20, 25, and 35ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- High Density Package
  - 72 lead SIMM
  - Common Data Inputs and Outputs
- Single +3.3V (±10%) Supply Operation

DESCRIPTION

The EDI8G322048V is a high speed 64 megabit Static RAM module organized as 2048K words by 32 bits. This module is constructed from sixteen 1024K x 4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

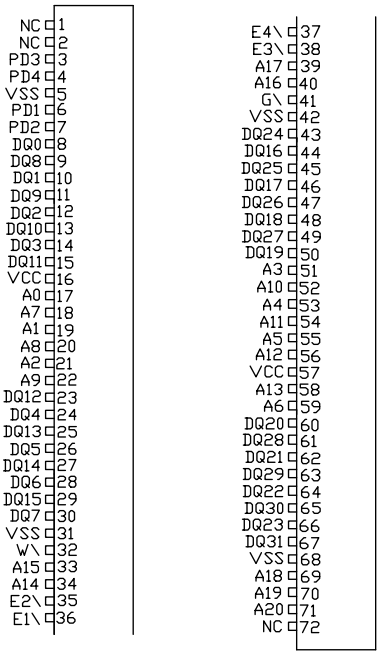
Four chip enables ($\overline{E_0}$-$\overline{E_3}$) and the highest order address line are used to independently enable the four bytes as well as the low or high block of addressable memory space. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8G322048V is offered in a 72 lead SIMM package, which enables 64 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 3.3V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

*Pins PD1- PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

PIN CONFIGURATION



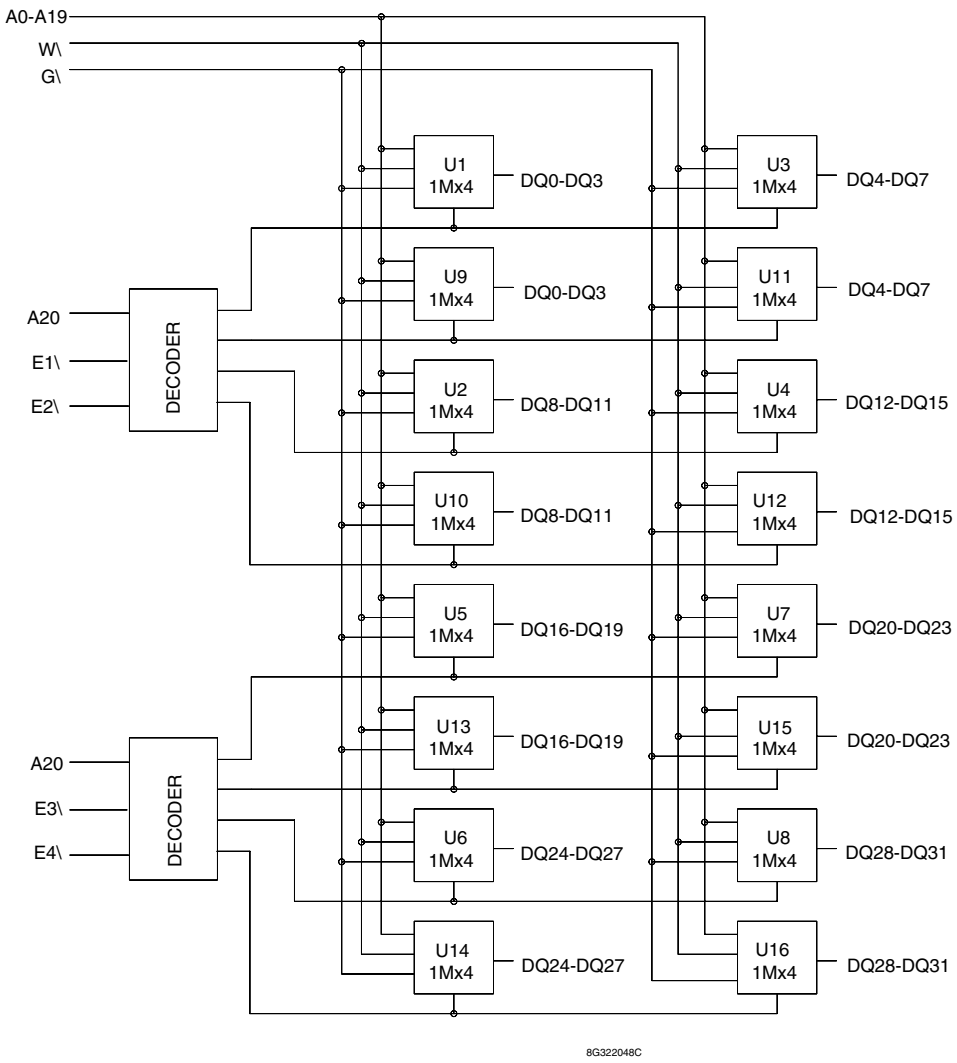
PIN NAMES

A_0-A_{20}	Address Inputs
$\overline{E_1}$-$\overline{E_4}$	Chip Enables
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ_0-DQ_{31}	Common Data Input/Output
V_{CC}	Power (+3.3V±10%)
V_{SS}	Ground
NC	No Connection

*

PD_1	PD_2	PD_3	PD_4
Open	V_{SS}	V_{SS}	Open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 4.6V
Operating Temperature T_A (Ambient) Commercial	0°C to +70°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	7.0 Watts
Output Current	20 mA

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power Supply Current	I_{CC1}	$\overline{W}$, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle			1750	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{E} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$			800	mA
Full Standby Power Supply Current CMOS	I_{CC3}	$\overline{E} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$			160	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	—	—	±80	µA
Output Leakage Current	I_{LO}	$V_{I/C}$ = 0V to V_{CC}	—	—	±20	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

**Typical: T_A = 25°C, V_{CC} = 3.3V*

TRUTH TABLE

$\overline{E1}$	$\overline{E2}$	$\overline{E3}$	$\overline{E4}$	$\overline{W}$	$\overline{G}$	Operational Comments
H	H	H	H	H	H	Disabled
L	L	L	L	H	L	Read Double Word
L	L	L	L	L	H	Write Double Word
*	*	*	*	L	H	Write One or More Bytes in Double Word
*	*	*	*	H	L	Read One or More Bytes in Double Word

**Each enable controls one byte (x8) within the x32 (doubleword) and one or more byte enables may be driven valid during this operation.*

CAPACITANCE
(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	C_I	120	pF
Data Lines	$C_{D/Q}$	20	pF
Chip Enable Line	C_C	120	pF
Write Line	C_N	120	pF

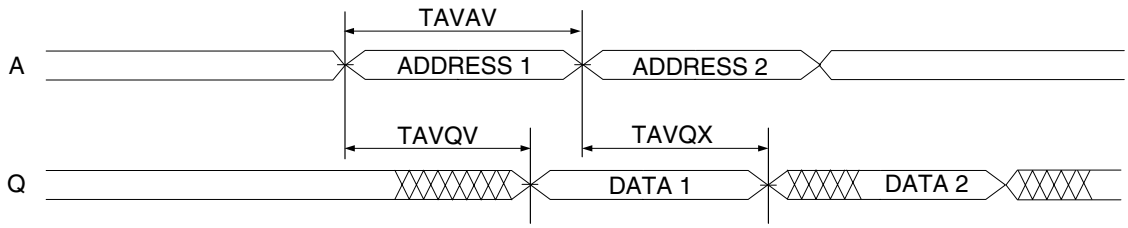
These parameters are sampled, not 100% tested.

AC CHARACTERISTICS READ CYCLE

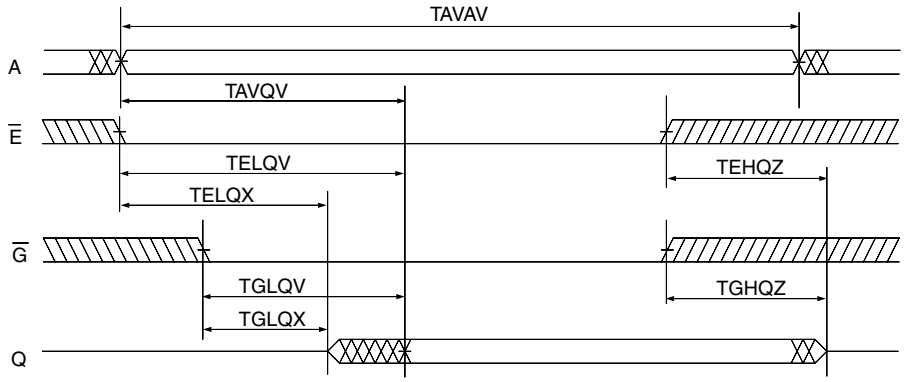
Parameter	Symbol JEDEC	Symbol Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	20		25		35		ns
Address Access Time	t_{AVQV}	t_{AA}		20		25		35	ns
Chip Enable Access	t_{ELQV}	t_{ACS}		20		25		35	ns
Chip Enable to Output in Low Z[1]	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z[1]	t_{EHQZ}	t_{CHZ}		15		17		20	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		15		17		20	ns
Output Enable to Output in Low Z[1]	t_{GLQX}	t_{OLZ}	0		0		0		ns
Output Disable to Output in High Z[1]	t_{GHQZ}	t_{OHZ}		15		17		20	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

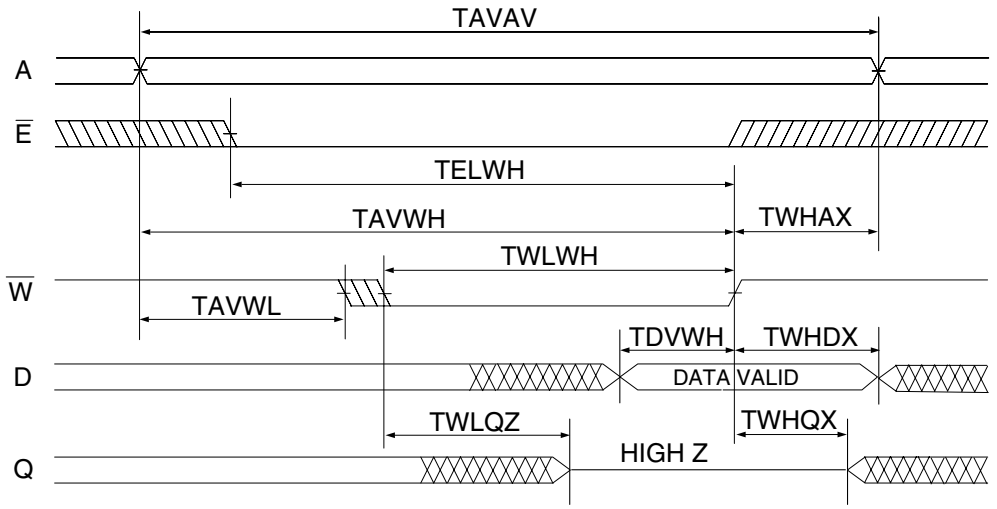


AC CHARACTERISTICS WRITE CYCLE

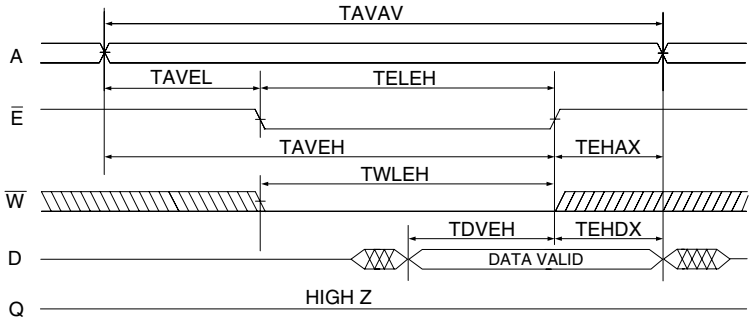
Parameter	Symbol JEDEC	Symbol Alt.	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	20		25		35		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	15		20		25		ns
	t_{WLEH}	t_{CW}	15		20		25		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	15		20		25		ns
	t_{AVEH}	t_{AW}	15		20		25		ns
Write Pulse Width	t_{WLWH}	t_{WP}	15		20		25		ns
	t_{ELEH}	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	3		0		0		ns
	t_{EHDX}	t_{DH}	3		0		0		ns
Write to Output in High Z[1]	t_{WLQZ}	t_{WHZ}	0	8	0	12	0	15	ns
Data to Write Time	t_{DVWH}	t_{DW}	12		15		20		ns
	t_{DVEH}	t_{DW}	12		15		20		ns
Output Active from End of Write[1]	t_{WHQX}	t_{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled

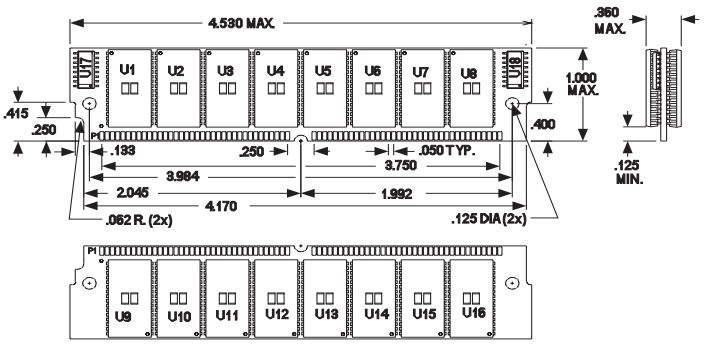


Ordering Information

Part Number	Speed (ns)
EDI8G322048V20MMC	20
EDI8G322048V25MMC	25
EDI8G322048V35MMC	35

Package Descriptions

72 LEAD SIMM



ALL DIMENSIONS ARE IN INCHES