TEMIC
Semiconductors

128 K × 8 Very Low Power CMOS SRAM

Introduction

The M 65608 is a very low power CMOS static RAM organized as 131072×8 bits. It is manufactured using the TEMIC high performance CMOS technology named SCMOS.

With this process, TEMIC brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the M 65608 combines an extremely low standby supply current (Typical value = 0.2 µA) with a fast access time at 25 ns over the full commercial temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
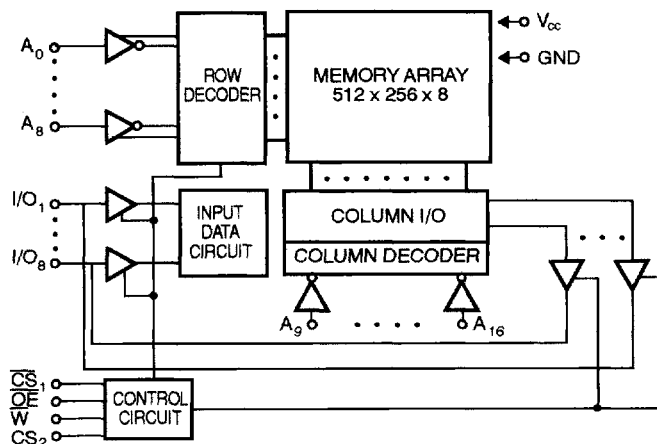
For military/space applications that demand superior levels of performance and reliability the M 65608 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

Features

- Access time : commercial : 25/30/35/45 ns
  industrial and military : 25/30/35/45 ns
- Very low power consumption
  active : 250 mW (Typ)
  standby : 1 µW (Typ)
  data retention : 0.5 µW (Typ)
- Wide temperature Range : –55 To +125°C
- 400 Mils width package

- TTL compatible inputs and outputs
- Asynchronous
- Single 5 volt supply
- Equal cycle and access time
- Gated inputs :
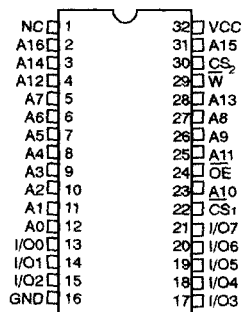 no pull-up/down
  resistors are required

Interface

Block Diagram

Pin Configuration

32 pins DLCC ceramic 400 MILS
32 pins DIL side-brazed   400 MILS
32 pins Flatpack   400 MILS
32 pins PDIL   400 MILS
32 pins SOIC and SOJ   400 MILS

```
        NC  1        32  VCC
       A16  2        31  A15
       A14  3        30  CS₂
       A12  4        29  W
        A7  5        28  A13
        A6  6        27  A8
        A5  7        26  A9
        A4  8        25  A11
        A3  9        24  OE
        A2 10        23  A10
        A1 11        22  CS₁
        A0 12        21  I/O7
      I/O0 13        20  I/O6
      I/O1 14        19  I/O5
      I/O2 15        18  I/O4
       GND 16        17  I/O3
```

Pin Names

A0–A16	Address inputs
I/O0–I/O7	Data Input/Output
$\overline{CS}_1$	Chip select 1
CS_2	Chip select 2
$\overline{W}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

Truth Table

$\overline{CS}_1$	CS_2	$\overline{W}$	$\overline{OE}$	INPUT/OUTPUT (I/O0 – I/O7)	MODE
H	X	X	X	Z	Deselect/Power-down
X	L	X	X	Z	Deselect/Power Down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential : . . . . - 0.5 V + 7.0 V

DC input voltage : . . . . GND − 0,3 V to VCC + 0,3

DC output voltage high Z state : . . . . . . GND − 0,3 V to VCC + 0,3

Storage temperature : . . . . −65 °C to + 150 °C

Output current into outputs (low) : . . . . 20 mA

Electro statics discharge voltage : . . . . > 2 001 V

(MIL STD 883D method 3015.3)

Operating Range

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	5 V ± 10 %	− 55 °C to + 125 °C
Industrial	5 V ± 10 %	− 40 °C to + 85 °C
Commercial	5 V ± 10 %	0 °C to + 70 °C

Recommended DC Operating Conditions

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	GND − 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	−	V_{CC} + 0.3	V

Capacitance

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (1)	Input low voltage	−	−	8	pF
Cout (1)	Output high volt	−	−	8	pF

Note : 1. Guaranteed but not tested.

DC Parameters

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX (2)	Input leakage current	− 1	−	1	µA
IOZ (2)	Output leakage current	− 1	−	1	µA
VOL (3)	Output low voltage	−	−	0.4	V
VOH (4)	Output high voltage	2.4	−	−	

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output Disabled.
3. Vcc min. IOL = 8.0 mA.
4. Vcc min. IOH = −4.0 mA.

Consumption for Commercial

SYMBOL	DESCRIPTION	6508LL/V -20	6508LL/V -25	6508LL/V -35	6508LL/V -45	UNIT	VALUE
ICCSB (5)	Standby supply current	5/2	5/2	5/2	5/2	mA	max
ICCSB$_1$ (6)	Standby supply current	500/50	500/50	500/50	500/50	µA	max
ICCOP (7)	Dynamic operating current	150	140	130	120	mA	max

Consumption for Industrial

SYMBOL	DESCRIPTION	6508LL/V -25	6508LL/V -30	6508LL/V -35	6508LL/V -45	UNIT	VALUE
ICCSB (5)	Standby supply current	5/2	5/2	5/2	5/2	mA	max
ICCSB$_1$ (6)	Standby supply current	700/100	700/100	700/100	700/100	µA	max
ICCOP (7)	Dynamic operating current	160	150	140	120	mA	max

Consumption for Military

SYMBOL	DESCRIPTION	6508LL/V -25	6508LL/V -30	6508LL/V -35	6508LL/V -45	UNIT	VALUE
ICCSB (5)	Standby supply current	5/2.5	5/2.5	5/2.5	5/2.5	mA	max
ICCSB$_1$ (6)	Standby supply current	1 000/300	1 000/300	1 000/300	1 000/300	µA	max
ICCOP (7)	Dynamic operating current	160	150	140	120	mA	max

Notes : 5. $\overline{CS}_1 \geq$ VIH or CS$_2 \leq$ VIL and $\overline{CS}_1 \leq$ VIL.
6. $\overline{CS}_1 \geq$ Vcc – 0.3 V or, CS$_2 <$ Gnd + 0.3 V and $\overline{CS}_1 \leq$ 0.2 V
7. F = 1/TAVAV, Iout = 0 mA, $\overline{W} = \overline{OE} =$ VIH, Vin = Gnd/Vcc, Vcc max.

AC Parameters

Input pulse levels : . . . . Gnd to 3.0 V
Input rise : . . . . 5 ns

Input timing reference levels : . . . . 1.5 V
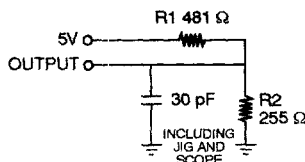Output loading IOL/IOH (see figure 1a and 1b) : . . . . + 30 pF

AC Test Loads Waveforms

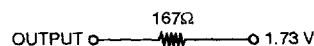Figure 1a

Figure 1b

Figure 2

Equivalent to : THEVENIN EQUIVALENT

167Ω
OUTPUT o——WWW——o 1.73 V

Data Retention Mode

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :
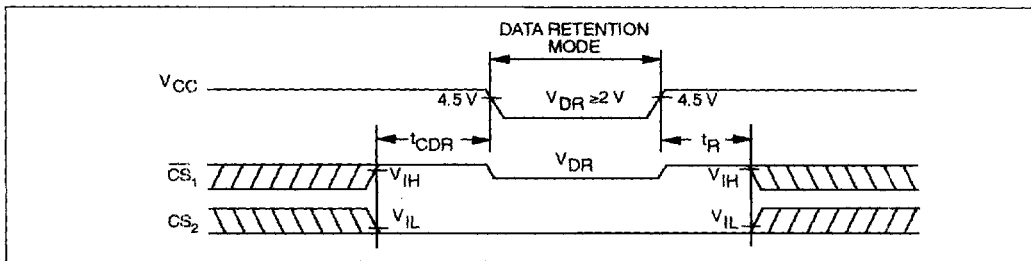
1. . During data retention chip select $\overline{CS}_1$ must be held high within VCC to VCC -0.2 V or, chip select CS_2 must be held low within GND to GND + 0.2 V.

2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.

3. During power up and power down transitions $\overline{CS}_1$ and $\overline{OE}$ must be kept between VCC + 0.3 V and 70 % of VCC, or with CS_2 between GND and GND - 0.3 V.

4. The RAM can begin operation > 45 ns after Vcc reaches the minimum operation voltages (4.5 V).

Timing

Data Retention Characteristics

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL $T_A = 25 °C$	MAXIMUM			UNIT
VCCDR	Vcc for data retention	2.0	--	--			V
TCDR	Chip deselect to data retention time	0.0	--	--			ns
TR	Operation recovery time	TAVAV (9)	--	--			ns
ICCDR1 (10)	Data retention current			COM	IND	MIL	
	@ 2.0 V : M-65608-V	--	0.1	20	40	150	μA
	M-65608-L	--	0.1	200	300	500	μA
ICCDR2 (10)	Data retention current			COM	IND	MIL	
	@ 3.0 V : M-65608-V	--	0.2	30	60	200	μA
	M-65608-L	--	0.2	300	450	600	μA

Notes : 9. TAVAV = Read cycle time.
10. $\overline{CS}_1$ = Vcc or $CS_2 = \overline{CS}_1$ = GND, Vin = Gnd/Vcc, this parameter is only tested at Vcc = 2 V.
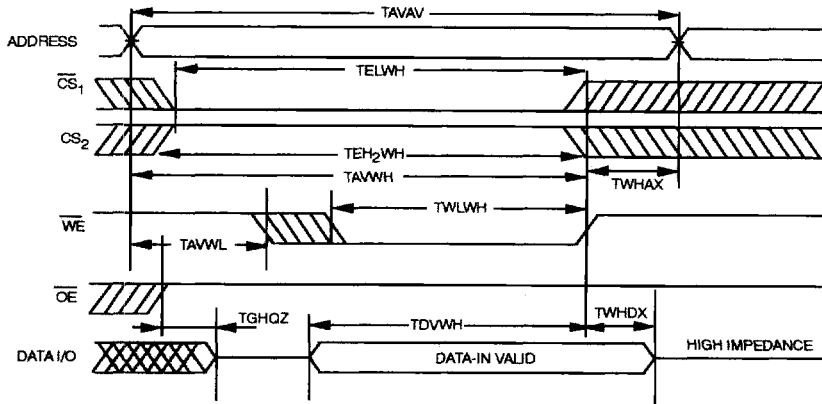
Write Cycle

SYMBOL	PARAMETER	65608LV-25	65608LV-30	65608LV-35	65608LV-45	UNIT	VALUE
TAVAW	Write cycle time	25	30	35	45	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	22	25	35	ns	min
TDVWH	Data set-up time	15	18	20	25	ns	min
TE$_1$LWH	$\overline{CS}_1$ low to write end	20	22	25	35	ns	min
TE$_2$HWH	CS$_2$ high to write end	20	22	25	35	ns	min
TWLQZ	Write low to high Z (11)	8	8	10	15	ns	max
TWLWH	Write pulse width	20	22	25	35	ns	min
TWHAX	Address hold from to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX	Write high to low Z (11)	0	0	0	0	ns	min

Read Cycle

SYMBOL	PARAMETER	65608LV-25	65608LV-30	65608LV-35	65608LV-45	UNIT	VALUE
TAVAV	Read cycle time	25	30	35	45	ns	min
TAVQV	Address access time	25	30	35	45	ns	max
TAVQX	Address valid to low Z	3	5	5	5	ns	min
TE$_1$LQV	Chip-select$_1$ access time	25	30	35	45	ns	max
TE$_1$LQX	$\overline{CS}_1$ low to low Z (11)	3	3	3	3	ns	min
TE$_1$HQZ	$\overline{CS}_1$ high to high Z (11)	15	18	20	20	ns	max
TE$_2$HQV	Chip-select$_2$ access time	25	30	35	45	ns	max
TE$_2$HQX	CS$_2$ high to low Z (11)	3	3	3	3	ns	min
TE$_2$LQZ	CS$_2$ low to high Z (11)	15	18	20	20	ns	max
TGLQV	Output Enable access time	10	12	12	15	ns	max
TGLQX	$\overline{OE}$ low to low Z (11)	0	0	0	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z (11)	8	8	10	15	ns	max

Notes : 11. Parameters guaranteed, not tested, with output loading 5 pF. (see fig. 1.b.).
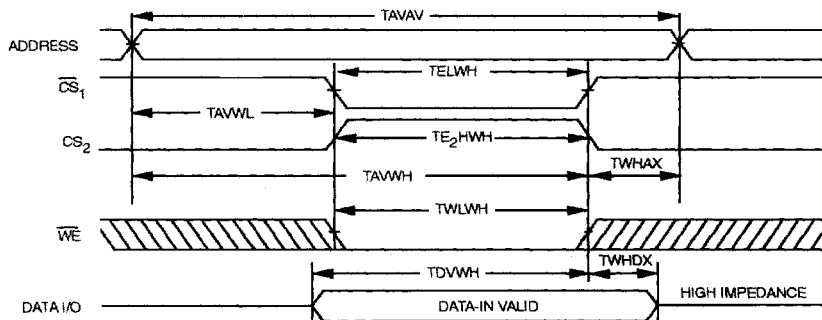
Write Cycle 1. $\overline{W}$ Controlled. $\overline{OE}$ High During Write

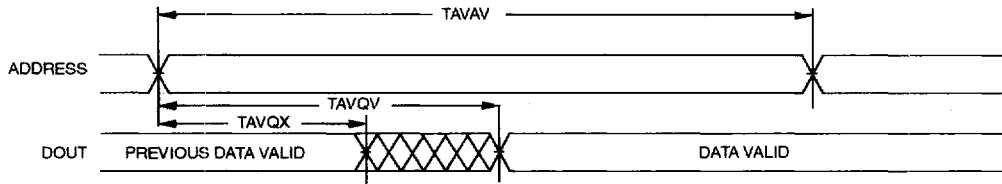## Write Cycle 2. $\overline{W}$ Controlled. $\overline{OE}$ Low

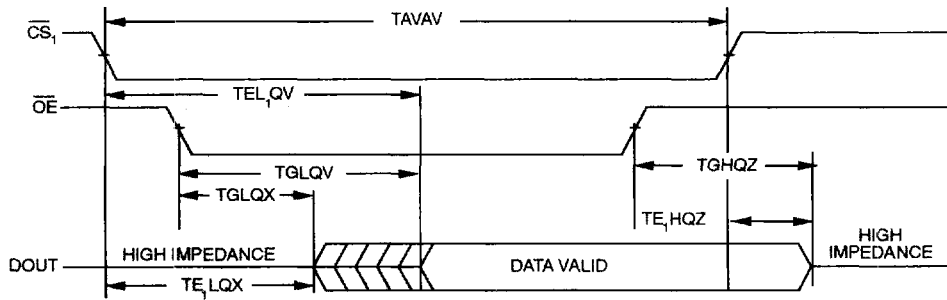## Write Cycle 3. $\overline{CS}_1$ or $\overline{CS}_2$ Controlled.

Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}_1$ Low and CS_2 HIGH and $\overline{W}$ LOW. Both signals must be actived to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write.
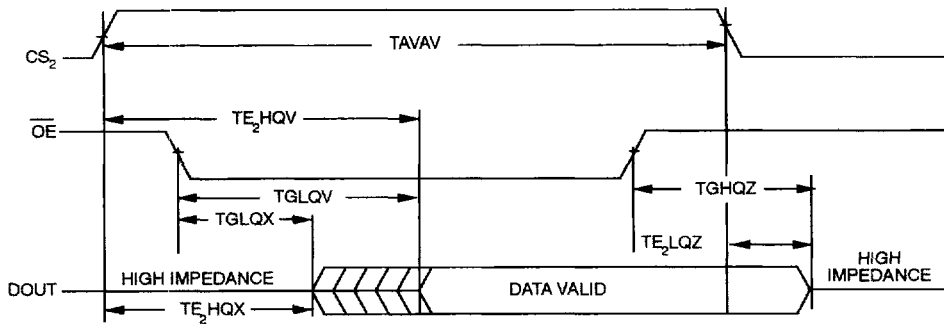Data out is high impedance if $\overline{OE}$ = VIH.

Read Cycle nb 1

Read Cycle nb 2

Read Cycle nb 3

Ordering Information

TEMPERATURE RANGE	PACKAGE	DEVICE	GRADE	SPEED	FLOW
M M	CJ	– 65608	V	– 45	/883

C = Commercial   0° to +70°C
I = Industrial   –40° to +85°C
M = Military   –55° to +125°C
S = Space   –55° to +125°C

L = Low power
V = Very low power

25 ns
30 ns
35 ns
45 ns

C9 =   Side Brazed 32 pins 400 mils
DJ =   Flat Package 32 pins 400 mils
4J =   Dual LCC 32 pins
39 =   Plastic DIL 32 pins 400 mils
T1 =   32 pins SOIC 400 mils
U1 =   32 pins SOJ 400 mils
0 =   die

128K × 8
STATIC RAM

blank   = MHS standards
/883   = MIL-STD 883 Class B or S
P883   = /883 + PIND Test
SB/SC   = SCC 9000 level B/C
SHXXX   = Special customer request
FHXXX   = Flight models (space)
EHXXX   = Engineering models (space)
MHXXX   = Mechanical parts (space)
LHXXX   = Life test parts (space)
: R   = Tape & Reel
: RD   = Tape & Reel and Dry pack
: D   = Dry pack

Military and Space Versions

The following table gives package/consumption/access time/process flow available combinations

Temp range	Package	Consumption		Access Time (ns)					Std process 65608	RT process 65608E	
		V	L	25	30	35	45	55	Mil flows (including SMD5962–89598)	Mil flows	Space flows
M	C9	●	●	●	●	●	●	●	●		
	DJ	X	X	X	X	X	X	X	X		
	4J	X	X	X	X	X	X	X	X		
	0	X	●	X	X	X	●	●	●		
S	C9	●			●	●	●	●		●	●
	DJ	X			X	X	X	X		X	X
	4J	X			X	X	X			X	X
	0	X	●		X	X		●		●	●

● = product in production

X = call sales office for availibility

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