

ACT-PS512K8 High Speed 4 Megabit Plastic Monolithic SRAM

Preliminary

PlasticPath™ Features

- Low Power Monolithic CMOS 512K x 8 SRAM
- Operating Temperature Range
 - Full Military (-55°C to +125°C)
 - Industrial (-40°C to +85°C)
- Burn-in and Temperature Cycle Available
- 15, 17, 20 & 25ns Access Times
- +5V Power Supply
- Industry Standard Pinouts
 - Center Power / Ground Pins
- TTL Compatible I/O
- 3.3V Device I/O Interfacing
- JEDEC Standard 36 pin Plastic SOJ Package
 - 36 Lead, .93" x .405" x 0.148" Small Outline J lead (SOJ), Aeroflex code# "L2"
- Fully Static Operation
 - No Clocks or Refresh Required

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www.aeroflex.com/act1.htm

General Description

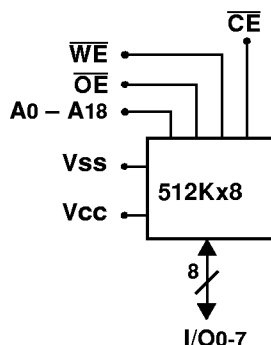
The ACT-PS512K8 is a Plastic High Speed, 4 Megabit (4,194,304 bits) CMOS Monolithic SRAM organized as 524,288 words by 8 bits. Designed for high-speed, high density, high reliability, mass memory and fast cache system applications.

The plastic monolithic is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 15ns, 17ns, 20ns and 25ns maximum are standard.

The +5 Volt power supply version is standard and +3.3 Volt lower power model is a future optional product.

The ACT-PS512K8 is Up-screened in Aeroflex's 80,000 square foot MIL-H-38534 certified facility in Plainview, N.Y.

Block Diagram – SOJ (L2)



Pin Description

I/O0-7	Data I/O
A0-18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

Absolute Maximum Ratings

Symbol	Parameter	MINIMUM	MAXIMUM	Units
T_o	Case Operating Temp.	-55	+125	°C
T_{STG}	Storage Temperature	-65	+150	°C
P_D	Maximum Package Power Dissipation		1.0	W
V_G	Maximum Signal Voltage to Ground	-0.5	$V_{CC} + 0.5$	V
V_{CC}	Power Supply Voltage	-0.5	+7.0	V

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{SS}	Ground	0	0	V
V_{IH}	Input High Voltage	+2.2	$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_A	Operating Temperature (Military)	-55	+125	°C
T_A	Operating Temperature (Industrial)	-40	+85	°C

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data I/O	Supply Current
Standby	H	X	X	High Z	I_{SB}
Output Disable	L	H	H	High Z	I_{CC}
Read	L	H	L	Data OUT	I_{CC}
Write	L	L	X	Data IN	I_{CC}

Capacitance

(V_{IN} & $V_{OUT} = 0V$, $f = 1MHz$, $T_A = 25^\circ C$, unless otherwise noted, Guaranteed but not tested)

Symbol	Parameter	Maximum	Units
C_{IN}	Input Capacitance (A_{0-18} , $\overline{WE}$ & $\overline{OE}$)	6	pF
C_{OUT}	Output Capacitance (I/O_{0-7} & $\overline{CE}$)	8	pF

DC Characteristics

($V_{CC} = 4.5V$ to $5.5V$, $V_{SS} = 0V$, $T_A = -55^\circ C$ to $+125^\circ C$ or $-40^\circ C$ to $+85^\circ C$)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	$V_{CC} = \text{Max}$, $V_{IN} = V_{SS}$ to V_{CC}	-10	+10	μA
Output Leakage Current	I_{LO}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}	-10	+10	μA
Operating Supply Current	I_{CC}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = 5.5V$		130	mA
Standby Current	I_{SB}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = 5.5V$		20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$, $V_{CC} = 4.5V$		0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4 \text{ mA}$, $V_{CC} = 4.5V$	2.4		V

Note: DC Test conditions: $V_{IL} = 0.3V$, $V_{IH} = V_{CC} - 0.3V$.

AC Characteristics

(V_{CC} = 4.5V to 5.5V, V_{SS} = 0V, T_A = -55°C to +125°C or -40°C to +85°C)

Read Cycle

Parameter	Sym	-015		-017		-020		-025		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		ns
Address Access Time	t _{AA}		15		17		20		25	ns
Chip Enable Access Time	t _{ACE}		15		17		20		25	ns
Output Hold from Address Change	t _{OH}	3		3		4		5		ns
Output Enable to Output Valid	t _{OE}		8		8		10		12	ns
Chip Enable to Output in Low Z (1)	t _{CLZ}	3		3		3		3		ns
Output Enable to Output in Low Z (1)	t _{OLZ}	0		0		0		0		ns
Chip Deselect to Output in High Z (1)	t _{CHZ}		7		7		8		10	ns
Output Disable to Output in High Z (1)	t _{OHZ}		7		7		8		10	ns

Note 1. Guaranteed by design, but not tested

Write Cycle

Parameter	Sym	-015		-017		-020		-025		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		ns
Chip Enable to End of Write	t _{CW}	12		12		13		15		ns
Address Valid to End of Write	t _{AW}	12		12		13		15		ns
Data Valid to End of Write	t _{DW}	8		8		9		10		ns
Write Pulse Width	t _{WP}	12		12		13		15		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		ns
Output Active from End of Write (1)	t _{OW}	3		3		4		5		ns
Write to Output in High Z (1)	t _{WHZ}		8		8		8		10	ns
Data Hold from Write Time	t _{DH}	0		0		0		0		ns

Note 1. Guaranteed by design, but not tested

Data Retention Electrical Characteristics (Special Order Only)

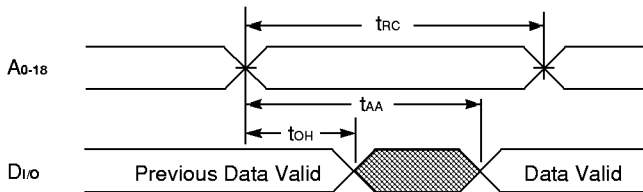
(T_A = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds			Units
			Min	Typ	Max	
V _{CC} for Data Retention	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		0.5	2.0	mA

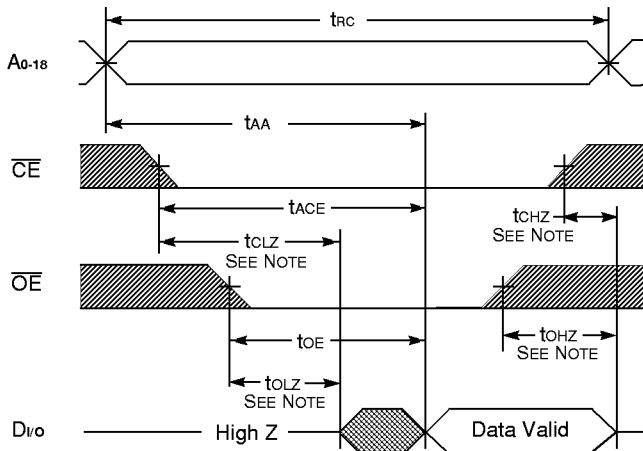
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



Read Cycle 2 ($\overline{WE} = V_{IH}$)



UNDEFINED

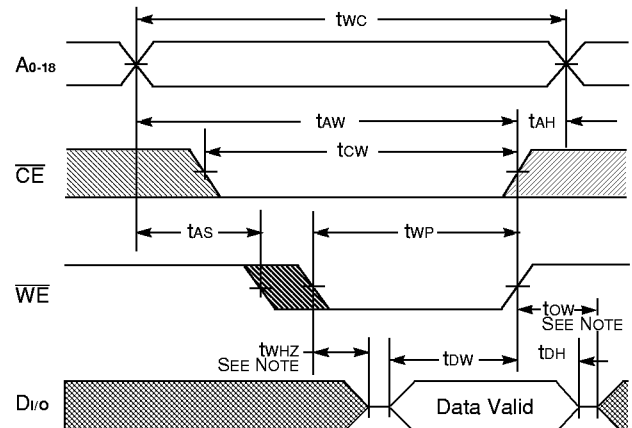


DON'T CARE

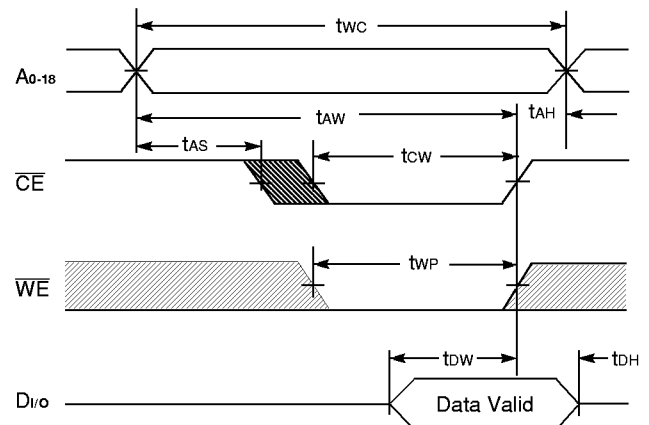
Note: Guaranteed by design, but not tested.

Write Cycle Timing Diagrams

Write Cycle 1 ($\overline{WE}$ Controlled, $\overline{OE} = V_{IL}$)

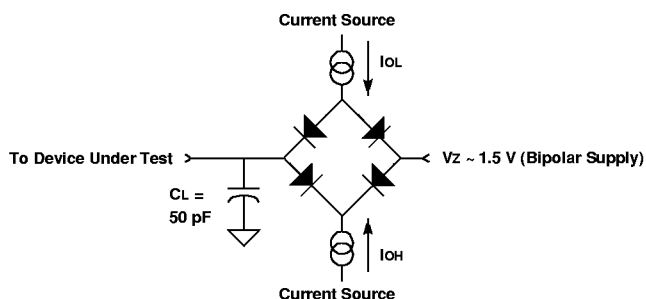


Write Cycle 2 ($\overline{CE}$ Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference	1.5	V
Output Load Capacitance	50	pF

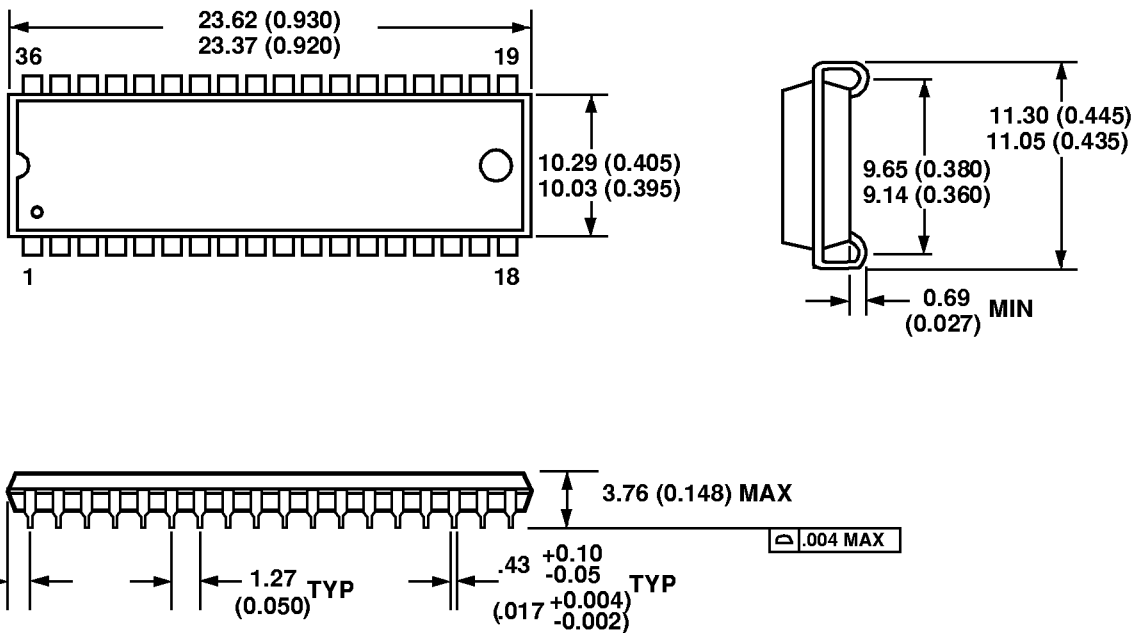
Notes:

- 1) V_Z is programmable from -2V to +7V.
- 2) I_{OL} and I_{OH} programmable from 0 to 16 mA.
- 3) Tester Impedance $Z_O = 75\Omega$.
- 4) V_Z is typically the midpoint of V_{OH} and V_{OL} .
- 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

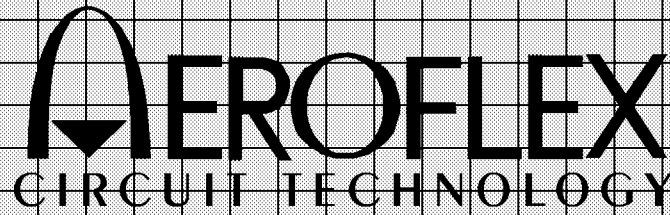
36 Pins — SOJ			
Pin #	Function	Pin #	Function
1	A ₀	19	NC
2	A ₁	20	A ₁₀
3	A ₂	21	A ₁₁
4	A ₃	22	A ₁₂
5	A ₄	23	A ₁₃
6	$\overline{CE}$	24	A ₁₄
7	I/O ₀	25	I/O ₄
8	I/O ₁	26	I/O ₅
9	V _{CC}	27	V _{CC}
10	V _{SS}	28	V _{SS}
11	I/O ₂	29	I/O ₆
12	I/O ₃	30	I/O ₇
13	$\overline{WE}$	31	$\overline{OE}$
14	A ₅	32	A ₁₅
15	A ₆	33	A ₁₆
16	A ₇	34	A ₁₇
17	A ₈	35	A ₁₈
18	A ₉	36	NC

Package Outline "L2" — SOJ Package, 36 Leads



All dimensions in inches

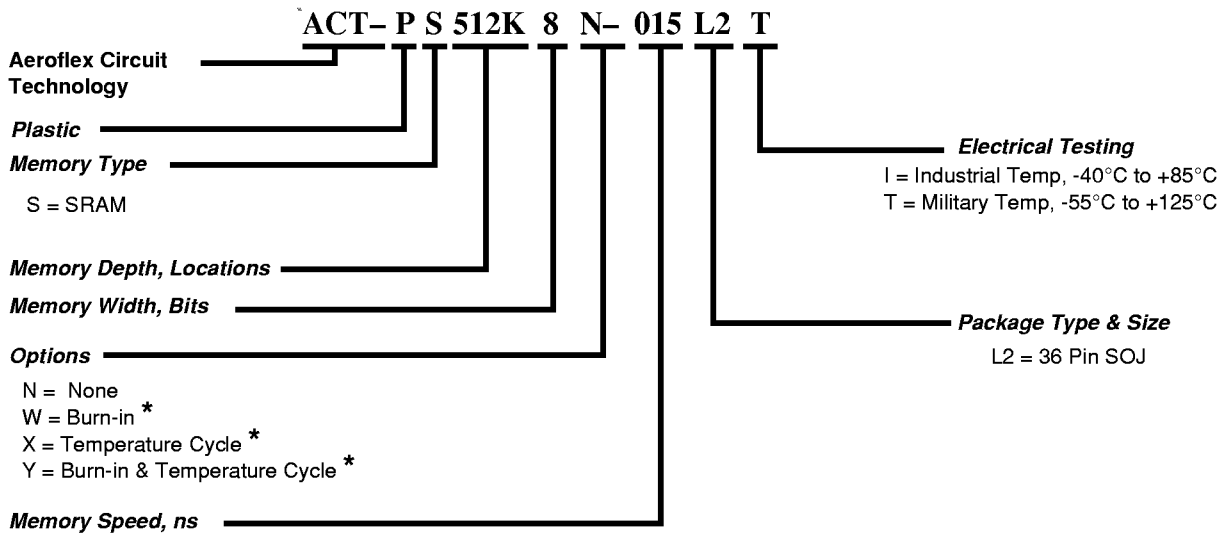
Dimensions in millimeters mm
Dimensions in inches ()



Ordering Information

Model Number	Speed	Package
ACT-PS512K8N-015L2T	15ns	36 Lead SOJ
ACT-PS512K8NB-017L2T	17ns	36 Lead SOJ
ACT-PS512K8N-020L2T	20ns	36 Lead SOJ
ACT-PS512K8N-025L2T	25ns	36 Lead SOJ

Part Number Breakdown



* Screened to the test methods of MIL-STD-883

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