The μPD17P203A is provided with a one-time PROM in the place of the internal ROM in the μPD17203A.

Since a program can be written into the PROM for this microcomputer, it is suitable for experimental production or small-scale production of systems using μPD17203A.

It is recommended that you also read the separately available reference materials on μPD17203A.

FEATRUES

- Internal one-time PROM: 4,096 x 16 bits
- Single power source: 2.2 to 5.5 V

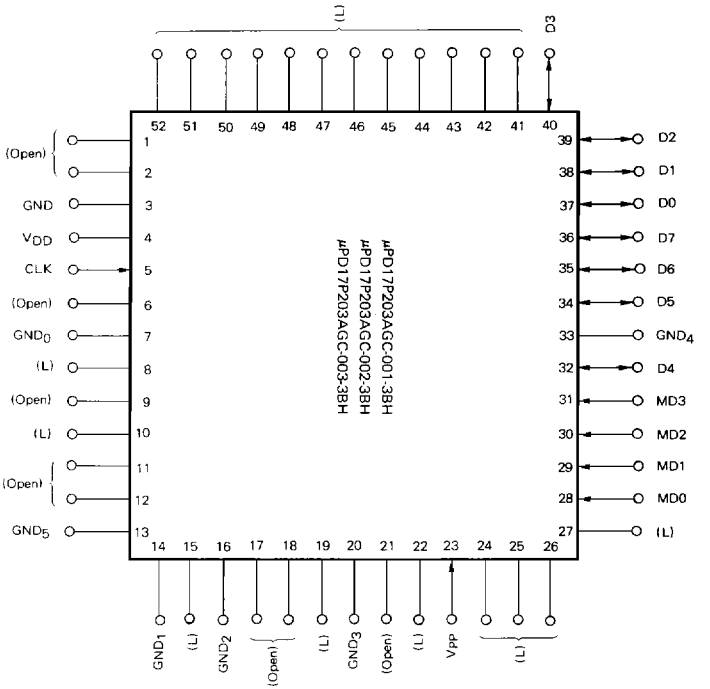
ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P203AGC-001-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-002-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-003-3BH	52-pin plastic QFP	Standard

The differences among the above models are as follows:

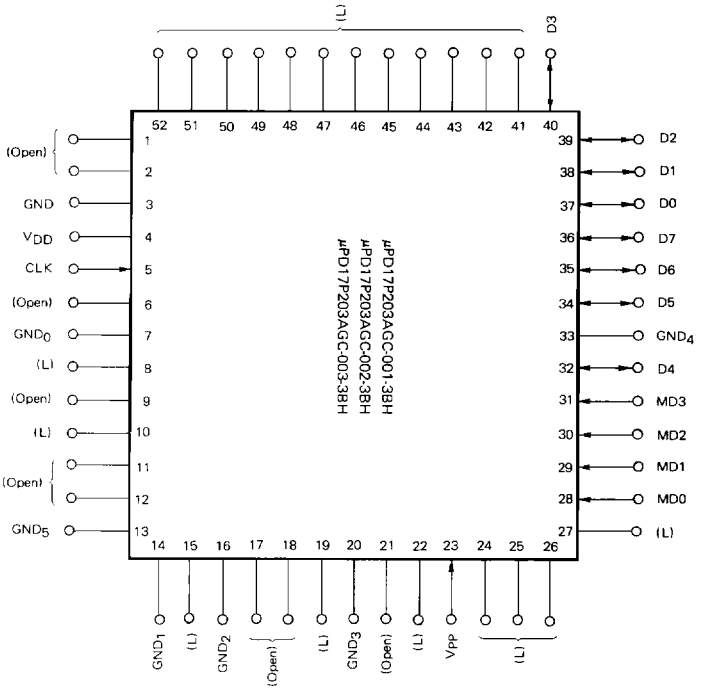
Item	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
$\overline{\text{RESET}}$ pin pull-up resistor	Provided	Not provided	Not provided	Mask option
P0A and P0B pins pull-up resistor	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option

(2) PROM programming mode



Note: ( ) indicates processing of pins not used in the PROM programming mode.
L : Ground each of these pins through a resistor (470 Ω).
Open : Connect nothing to these pins.

(2) PROM programming mode



Note: ( ) indicates processing of pins not used in the PROM programming mode.
L : Ground each of these pins through a resistor (470 Ω).
Open : Connect nothing to these pins.

The μPD17P203A is provided with a one-time PROM in the place of the internal ROM in the μPD17203A.

Since a program can be written into the PROM for this microcomputer, it is suitable for experimental production or small-scale production of systems using μPD17203A.

It is recommended that you also read the separately available reference materials on μPD17203A.

FEATRUES

- Internal one-time PROM: 4,096 x 16 bits
- Single power source: 2.2 to 5.5 V

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P203AGC-001-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-002-3BH	52-pin plastic QFP	Standard
μPD17P203AGC-003-3BH	52-pin plastic QFP	Standard

The differences among the above models are as follows:

Item	μPD17P203A-001	μPD17P203A-002	μPD17P203A-003	μPD17203A
$\overline{\text{RESET}}$ pin pull-up resistor	Provided	Not provided	Not provided	Mask option
P0A and P0B pins pull-up resistor	Provided	Provided	Not provided	Mask option
Main clock oscillator circuit	Provided	Provided	Not provided	Mask option
Subclock oscillator circuit	Provided	Not provided	Provided	Mask option

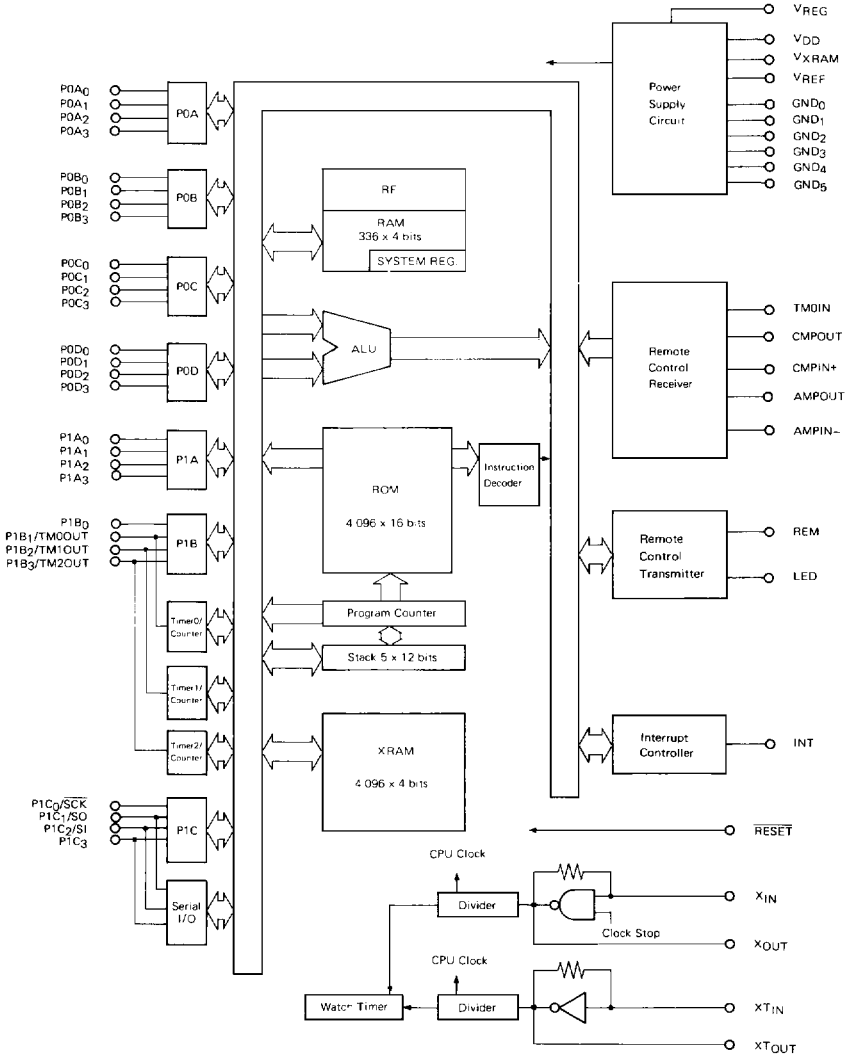
1. PIN FUNCTIONS

1.1 PORT PINS

Symbol	I/O	Shared by: *	Function	At reset
$P0A_0$–$P0A_3$	I/O	–	4-bit I/O port (Port 0A). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0B_0$–$P0B_3$	I/O	(MD0–MD3)	4-bit I/O port (Port 0B). Can be set in input or output mode in 4 bit units. Pull-up resistors are connected in I/O mode.	Input
$P0C_0$–$P0C_3$	I/O	(D4–D7)	4-bit I/O port (Port 0C). Can be set in input or output mode in 4 bit units. N-ch open-drain in output mode.	Input
$P0D_0$–$P0D_3$	I/O	(D0–D3)	4-bit I/O port (Port 0D). Can be set in input or output mode in units of 4 bits. N-ch open-drain in output mode.	Input
$P1A_0$–$P1A_3$	I/O	–	4-bit I/O port (Port 1A). Can be set in input or output mode in bit units. N-ch open-drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_0$	I/O	–	4-bit I/O port (Port 1B). Can be set in input or output mode in bit units. N-ch open drain in output mode. Pull-up resistor can be connected by program in I/O mode.	Input
$P1B_1$–$P1B_3$		TM0OUT–TM2OUT		
$P1C_0$	I/O	$\overline{SCK}$	4-bit I/O port (Port 1C). Can be set in input or output mode in bit units. Pull-up resistor can be connected by program in I/O mode.	Input
$P1C_1$		SO		
$P1C_2$		SI		
$P1C_3$		–		

*( ): Pins shared in PROM programming mode.

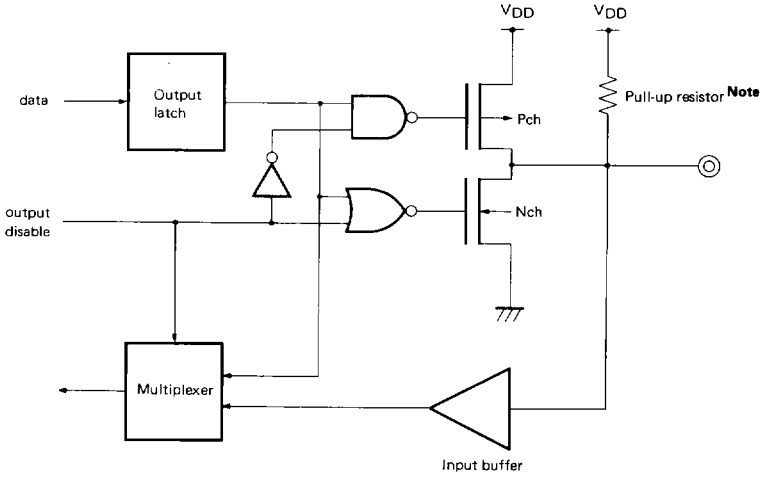
BLOCK DIAGRAM



1.4 INPUT/OUTPUT CIRCUITS

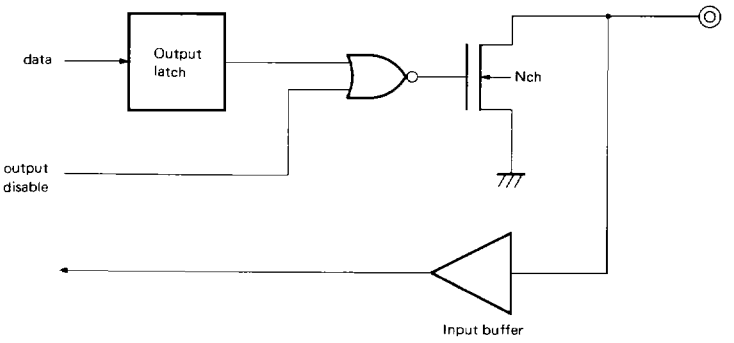
The input/output circuit for each μPD17P203A's pin are shown below.

(1) $P0A_0$–$P0A_3$, $P0B_0$/MD0–$P0B_3$/MD3



Note: μPD17P203A-001 and -002 only.

(2) $P0C_0$/D4–$P0C_3$/D7, $P0D_0$/D0–$P0D_3$/D3



4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD17203A is a 4-bit CMOS microcontroller for infrared remote controllers. It contains 16K-bit static RAM, three channels of timers, a carrier generator for remote control, an amplifier for remote control receive signals, and a waveform shaping circuit in one chip.

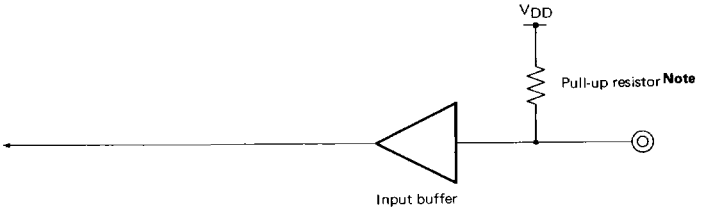
The 17K architecture used in the μPD17203A allows the user to perform an arithmetic/logical operation or data transfer between data memory locations or between data memory and a peripheral circuit with a single instruction. Every instruction is 1 word long, consisting of 16 bits.

The microcontroller is packaged in a 52-pin plastic QFP.

FEATURES

- 17K architecture
- Program memory (ROM): 8K bytes (4096 x 16 bits)
- Data memory (RAM): 336 words (336 x 4 bits)
- Static RAM: 16K bits (4096 x 4 bits)
- On-chip carrier generator for infrared remote control
- On-chip amplifier for infrared remote control receive signals
- On-chip waveform shaping circuit for infrared remote control receive signals
- Many input/output ports provided (28 lines)
- 3-wire serial interface contained (also used as a input/output port)
- 5 stack levels
- 8-bit timer: 1 channel (with a modulo function)
  Clock for the timer (8 μs, 16 μs, 64 μs, remote control carrier input)
- 10-bit timer: 1 channel (with a modulo function)
  Clock for the timer (0.5 μs, 4 μs, INT input)
- 16-bit timer: 1 channel (with a modulo function)
  Clock for the timer (8 μs, 16 μs, 32 μs, 64 μs)
- Clock timer: 1 channel (used as a watchdog timer or a clock)
- Instruction execution time: 4 μs (when a 4 MHz ceramic resonator is used)
- Standby function (STOP, HALT)
- Low-voltage detector contained
- Operating voltage: 2.2 to 5.5 V
- Operating clock: 4 MHz ceramic resonator/32.768 kHz crystal resonator

(3) $\overline{\text{RESET}}$



Note: μPD17P203A-001 only.

AC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address setup time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}	2			μs	
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address hold time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 setup time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → data output delay time	t_{DV}	t_{DV}			1	μs	MD0=MD1=V_{IL}
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H}+t_{M1R}$ ≧ 50 μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program counter reset time	t_{PCR}	–	10			μs	
CLK input high-, low-level width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4.19	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	μs	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

*1: Symbols for corresponding μPD27C256

*2: The internal address is incremented (+1) at the falling edge of third clock periods for the four CLK clock periods, which constitute one cycle. The internal address has no external pin connection.

3. WRITING, READING, AND VERIFYING ONE-TIME PROM (PROGRAM MEMORY)

The μPD17P203A internal program memory is a one-time 4,096 x 16 bit PROM.

The write, read, and verify this one-time PROM, the pins shown in the following table are used. Note that no address input pin is provided. Instead, the address is updated by the clock signal input from the CLK pin.

Pin	Function
V_{PP}	Program voltage application
CLK	Address updating clock input
MD0–MD3	Operation mode selection
D0–D7	8-bit data input/output

3.1 OPERATION MODES WHEN PROGRAM MEMORY IS WRITTEN, READ, OR VERIFIED

μPD17P203A is set in the program memory write, read, and verify mode, when, +6 V is applied to the V_{DD} pin and +12.5 V is applied to the V_{PP} pin after it has been reset for a certain period of time (V_{DD} = 5 V, $\overline{RESET}$ = 0 V). Once this mode has been set, the following operation modes are available, depending on the setting of the MD0 through MD3 pins. Note that all the unused pins are pulled down with resistors to the ground potential.

Operation mode setting						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address 0 clear
		L	H	H	H	Write mode
		L	L	H	H	Read and verify mode
		H	X	H	H	Program inhibit mode

X: L or H

3.2 PROGRAM MEMORY WRITING PROCEDURE

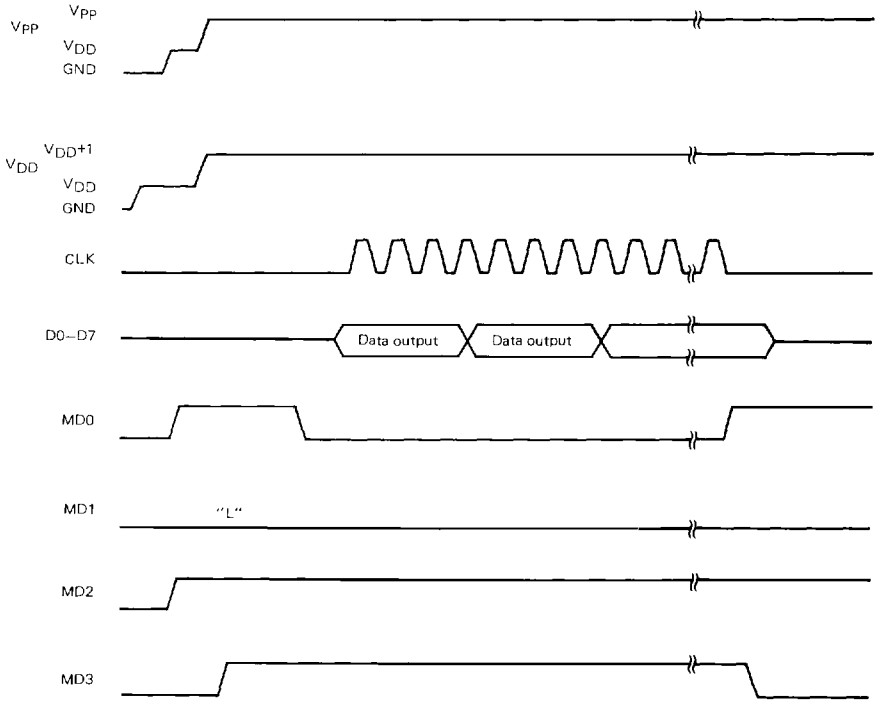
The program memory can be written in the following procedure at high speeds:

(1) Pull down the unused pins with resistors to the ground potential. Make the CLK pin low.
(2) Apply 5 V to the V_{DD} pin. Make the V_{PP} pin low.
(3) Wait for 10 μs. Then apply 5 V to the V_{PP} pin.
(4) Set the program memory address 0 clear mode by using the mode selection pins.
(5) Apply 6 V to V_{DD} and 12.5 V to V_{PP}.
(6) Set the program inhibit mode.
(7) Write data in the 1 ms write mode.
(8) Set the program inhibit mode.
(9) Set the verify mode. If the data has been correctly written, proceed to step (10). If not, repeat (7) through (9).
(10) Additional write for (the number of times (7) through (9) are repeated: X) x 1 ms.
(11) Set the program inhibit mode.
(12) Input a pulse to the CLK pin four times to increment the program memory address by one.
(13) Repeat (7) through (12) until the last address is written.
(14) Set the program memory address 0 clear mode.
(15) Apply 5 V to the V_{DD} and V_{PP} pins.
(16) Turn off power.

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
LCD Output Voltage Variable Range	V_{LCD0}	0.8		1.8	V		
Doubler Output Voltage	V_{LCD1}	1.9 V_{LCD0}	2 V_{LCD0}		V		
Tripler Output Voltage	V_{LCD2}	2.85 V_{LCD0}	3 V_{LCD0}		V		
Low-voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V	VDET pin external resistance = 2 MΩ	
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{\text{RESET}}$ pin and INT pin	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{\text{RESET}}$ pin and INT pin	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	RESET	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	P0A-P0D	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			0.2	μA	$\overline{\text{RESET}}$	V_{IL} = 0 V, w/o pull-up resistor
	I_{IL3}	20	50	100	μA		V_{IL} = 0 V w/pull-up resistor
	I_{IL4}			0.2	μA	P0A, P0B	V_{IL} = 0 V w/o pull-up resistor
	I_{IL5}	6	12	20	μA		V_{IL} = 0 V w/pull-up resistor
Low-Level Input Current	I_{IL6}			0.2	μA	P0C, P0D	V_{IL} = 0 V
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	V_{OH} = V_{DD}-0.3 V
	I_{OH2}	−7.0	−15.0	−25.0	mA	REM	V_{OH} = V_{DD}-2 V
	I_{OH3}	−0.3	−1.0	−2.0	mA	LED	V_{OH} = V_{DD}-0.3 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	$\overline{\text{VDOUT}}$	V_{OH} = V_{DD}-0.3 V

Steps (2) through (9) are illustrated below.



3. DIFFERENCES BETWEEN μPD17P202A AND μPD17202A

In the μPD17P202A, the internal mask ROM (program memory) for the μPD17202A is replaced by the PROM which can be programmed by the user. Therefore, the program memory and some mask options are the only differences between the μPD17P202A and μPD17202A, so the CPU functions and internal hardware are identical.

The table below summarizes the differences between the μPD17P202A and μPD17202A.

Refer to the μPD17202A data sheet for details on CPU functions and internal hardware.

<table>
<tr><th>Device / Item</th><th>μPD17P202A-001</th><th>μPD17P202A-002</th><th>μPD17P202A-003</th><th>μPD17202A</th></tr>
<tr><td>Program memory</td><td colspan="3">• PROM
• 0000H-07FFH
• 2048 x 16 bits</td><td>• Mask ROM
• 0000H-07FFH
• 2048 x 16 bits</td></tr>
<tr><td>$\overline{\text{RESET}}$ pin pull-up resistor</td><td rowspan="4">Provided</td><td>None</td><td rowspan="3">None</td><td rowspan="4">(Mask option)</td></tr>
<tr><td>P0A, P0B pins pull-up resistors</td><td rowspan="2">Provided</td></tr>
<tr><td>Main clock generator provided/not provided</td></tr>
<tr><td>Subclock generator provided/not provided</td><td>None</td><td>Provided</td></tr>
<tr><td>Pin connections</td><td colspan="3">V_{PP} pin, PROM programming pin are provided.</td><td>V_{PP} pin, PROM programming pin not provided</td></tr>
<tr><td>Operating voltage range</td><td colspan="4">2.2 to 5.5 V</td></tr>
<tr><td>Package</td><td colspan="4">64-pin plastic QFP (14 x 20 mm)</td></tr>
</table>

DC CHARACTERISTICS (V_{DD} = 3 V, T_a = −20 to +75 °C, f_X = 4 MHz, f_{XT} = 32 kHz)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Low Voltage Detection Voltage	V_{DET}	1.3	2.0	2.9	V		
High-Level Input Voltage	V_{IH1}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IH2}	0.7 V_{DD}		V_{DD}	V	Other than $\overline{RESET}$, INT pins	
Low-Level Input Voltage	V_{IL1}	0		0.2 V_{DD}	V	$\overline{RESET}$, INT pins	
	V_{IL2}	0		0.3 V_{DD}	V	Other than $\overline{RESET}$, INT pins	
High-Level Input Current	I_{IH1}			0.2	μA	INT	$V_{IH} = V_{DD}$
	I_{IH2}			0.2	μA	TM0IN	$V_{IH} = V_{DD}$
	I_{IH3}			0.2	μA	$\overline{RESET}$	$V_{IH} = V_{DD}$
	I_{IH4}			0.2	μA	P0A–P0D	$V_{IH} = V_{DD}$
	I_{IH5}			0.2	μA	P1A–P1C	$V_{IH} = V_{DD}$
Low-Level Input Current	I_{IL1}			−0.2	μA	INT	V_{IL} = 0 V
	I_{IL2}			−0.2	μA	TM0IN	V_{IL} = 0 V
	I_{IL3}			−0.2	μA	$\overline{RESET}$	V_{IL} = 0 V w/o pull-up resistor
	I_{IL4}	−20	−50	−100	μA		I_{IL} = 0 V w/pull-up resistor
	I_{IL5}	−6	−12	−20	μA	P0A, P0B	V_{IL} = 0 V w/pull-up resistor
	I_{IL6}			−0.2	μA	P0C, P0D	V_{IL} = 0 V
	I_{IL7}			−0.2	μA	P1A–P1C	V_{IL} = 0 V w/o pull-up resistor
	I_{IL8}	−20	−50	−90	μA		I_{IL} = 0 V w/pull-up resistor
High-Level Output Current	I_{OH1}	−0.6	−2.0	−4.0	mA	P0A, P0B	$V_{OH} = V_{DD}$−0.3 V
	I_{OH2}	−0.6	−2.0	−4.0	mA	P1C	$V_{OH} = V_{DD}$−0.3 V
	I_{OH3}	−7.0	−15.0	−25.0	mA	REM	$V_{OH} = V_{DD}$−2 V
	I_{OH4}	−0.3	−1.0	−2.0	mA	LED	$V_{OH} = V_{DD}$−0.3 V
	I_{OH5}	−0.3	−1.0	−2.0	mA	$\overline{VDOUT}$	$V_{OH} = V_{DD}$−0.3 V
	I_{OH6}	−0.3	−1.0	−2.0	mA	CMPOUT	$V_{OH} = V_{DD}$−0.3 V
Low-Level Output Current	I_{OL1}	0.5	1.5	2.5	mA	P0A, P0B	V_{OL} = 0.3 V
	I_{OL2}	0.5	1.5	2.5	mA	P0C, P0D	V_{OL} = 0.3 V
	I_{OL3}	0.5	1.5	2.5	mA	REM	V_{OL} = 0.3 V
	I_{OL4}	0.5	1.5	2.5	mA	LED	V_{OL} = 0.3 V
	I_{OL5}	0.5	1.5	2.5	mA	$\overline{VDOUT}$	V_{OL} = 0.3 V
	I_{OL6}	0.5	1.5	2.5	mA	CMPOUT	V_{OL} = 0.3 V
V_{REF} Output Voltage	V_{REF}	0.8	1.2	1.6	V	External capacitance for V_{REF} pin = 0.1 μF	
Supply Current	I_{DD1}	0.5	1.0	2.0	mA	Operation mode	XT and X
	I_{DD2}		15	30	μA		Only XT
	I_{DD3}			2.0	mA	HALT mode	XT and X
	I_{DD4}		10	15	μA		Only XT
XRAM Hold Voltage	V_{XRAM}	1.3	3.0	5.5	V	Operation mode, V_{XRAM} = 3 V	
XRAM Supply Current	I_{XRAM1}		3.0		μA	HALT mlde, V_{XRAM} = 3 V, T_a = 25 °C	
	I_{XRAM2}		0.2	1.0	μA		

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High-Level Input Voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than CLK
	V_{IH2}	V_{DD}−0.5		V_{DD}	V	CLK
Low-Level Input Voltage	V_{IL1}	0		0.3 V_{DD}	V	Other than CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{L1}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
High-Level Output Voltage	V_{OH}	V_{DD}−1.0			V	I_{OH} = −1 mA
Low-Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note: 1. Keep V_{PP} to less than +13.5 V, including the overshoot.

2. Apply V_{DD} before V_{PP}. Remove V_{DD} after V_{PP}.

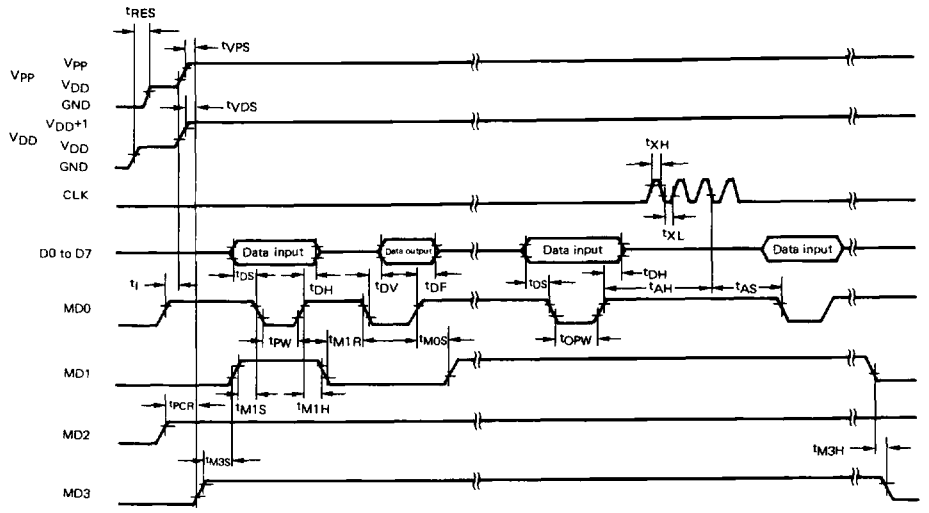
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0±0.25 V, V_{PP} = 12.5±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time*2 (vs. MD0 ↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (vs. MD0 ↓)	t_{MIS}	t_{OES}	2			μs	
Data Setup Time (vs. MD0 ↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time*2 (vs. MD0 ↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (vs. MD0 ↑)	t_{DH}	t_{DH}	2			μs	
MD0 ↑ → Data Output Float Delay Time	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time (vs. MD3 ↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (vs. MD3 ↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (vs. MD1 ↑)	t_{MOS}	t_{CES}	2			μs	
MD0 ↓ → Data Output Delay Time	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geq 50$ μs
MD1 Recovery Time (vs. MD0 ↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High, Low Level Widths	t_{XH}, t_{XL}	–	0.063			μs	
CLK Input Frequency	f_X	–			8	MHz	
Initial Mode Set Time	t_I	–	2			μs	
MD3 Setup Time (vs. MD1 ↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (vs. MD1 ↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (vs. MD0 ↓)	t_{M3SR}	–	2			μs	When program memory is read
Address*2 → Data Output Delay Time	t_{DAD}	t_{ACC}			2	μs	When program memory is read
Address*2 → Data Output Hold Time	t_{HAD}	t_{OH}	0		130	ns	When program memory is read
MD3 Hold Time (vs. MD0 ↑)	t_{M3HR}	–	2			μs	When program memory is read
MD3 ↓ → Data Output Float Delay Time	t_{DFR}	–	2			μs	When program memory is read
Reset Setup Time	t_{RES}		10			μs	

*1. Corresponding symbols of μPD27C256.

*2. The internal address signal is incremented by one at the falling edge of the third CLK input signal and is not connected to a pin.

PROGRAM MEMORY WRITE TIMING



PROGRAM MEMORY READ TIMING