# TC74HC4040P/F

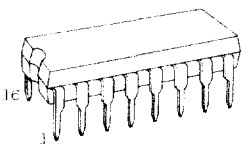
TC74HC4040P/F 12-STAGE BINARY COUNTER

## GENERAL DESCRIPTION

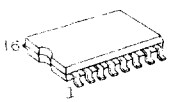
The TC74HC4040 is a high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate $C^2MOS$ technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4040B) with the same power dissipation.
A clear input is used to reset the counter to all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. All divided output stages are provided, and 1/4096 divided frequency will obtained at the last stage.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## FEATURES

- High Speed ..... $f_{max}$=60MHz(Typ.) at $V_{CC}$=5V
- Low Power Dissipation ..... $I_{CC}$=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% $V_{CC}$(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Functional Compatible with 4040B.



DIP16(3D16A-P)



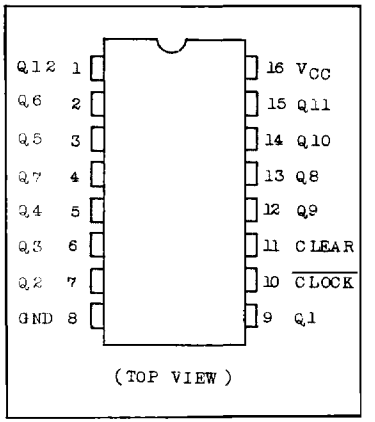
MFP16(F160C-P)

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage Range | $V_{CC}$ | -0.5 ∿ 7 | V |
| DC Input Voltage | $V_{IN}$ | -0.5 ∿ $V_{CC}$+0.5 | V |
| DC Output Voltage | $V_{OUT}$ | -0.5 ∿ $V_{CC}$+0.5 | V |
| Input Diode Current | $I_{IK}$ | ±20 | mA |
| Output Diode Current | $I_{OK}$ | ±20 | mA |
| DC Output Current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/Ground Current | $I_{CC}$ | ±50 | mA |
| Power Dissipation | $P_D$ | 500(DIP)*<br>180(MFP) | mW |
| Storage Temperature | $T_{stg}$ | -65 ∿ 150 | °C |
| Lead Temperature 10sec | $T_L$ | 300 | °C |

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

## PIN ASSIGNMENT



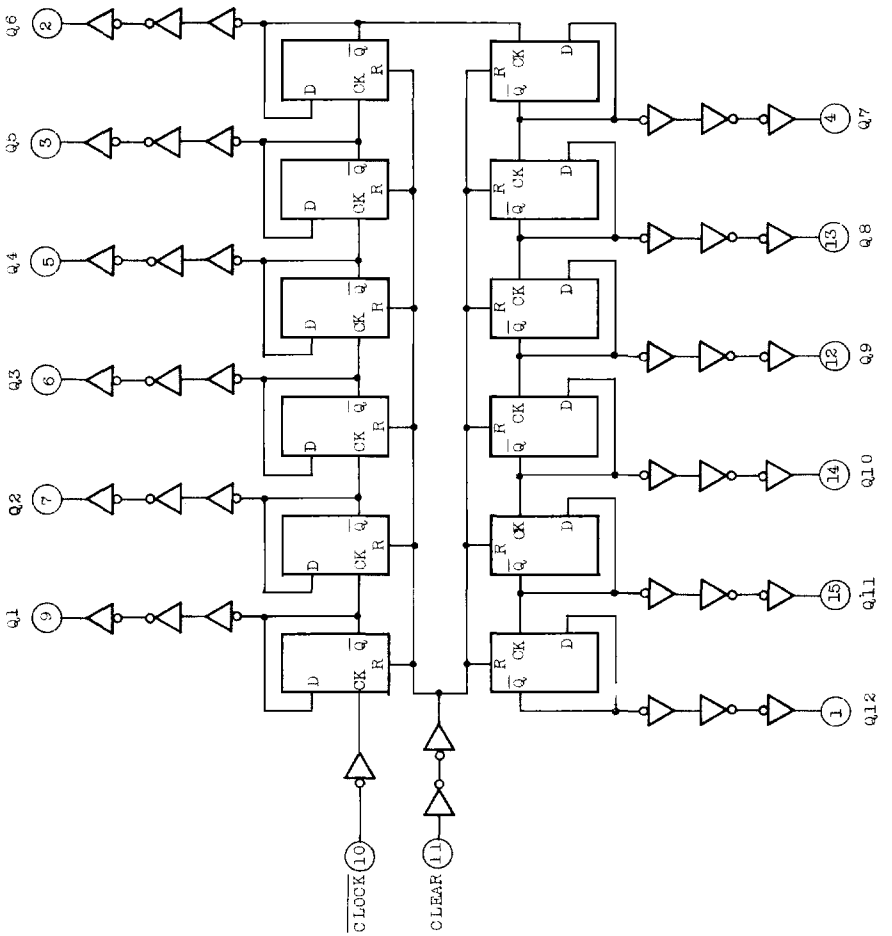

(TOP VIEW)

TRUTH TABLE

| $\overline{\text{CLOCK}}$ | CLEAR | OUTPUT STATE |
|---|---|---|
| X | H | ALL OUTPUTS = "L" |
| ↓ | L | NO CHANGE |
| ↑ | L | ADVANCE TO NEXT STATE |

X : DON'T CARE

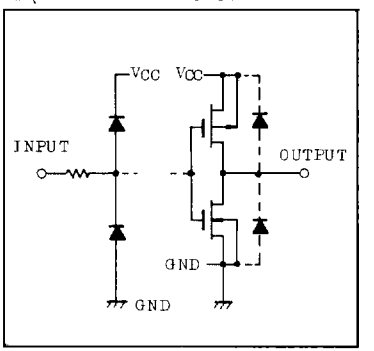
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | LIMIT | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2 ∿ 6 | V |
| Input Voltage | $V_{IN}$ | 0 ∿ $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0 ∿ $V_{CC}$ | V |
| Operating Temperature | $T_{opr}$ | -40 ∿ 85 | °C |
| Input Rise and Fall Time | $t_r$, $t_f$ | 0 ∿ 1000 ($V_{CC}$=2.0V)<br>0 ∿ 500 ($V_{CC}$=4.5V)<br>0 ∿ 400 ($V_{CC}$=6.0V) | ns |

INPUT and OUTPUT EQUIVALENT CIRCUIT




DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | | $V_{CC}$ | Ta=25°C MIN. | Ta=25°C TYP. | Ta=25°C MAX. | Ta=-40∿85°C MIN. | Ta=-40∿85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| High-Level Input Voltage | $V_{IH}$ | | | 2.0 | 1.5 | - | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | |
| | | | | 6.0 | 4.2 | - | - | 4.2 | - | |
| Low-Level Input Voltage | $V_{IL}$ | | | 2.0 | - | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | |
| | | | | 6.0 | - | - | 1.8 | - | 1.8 | |
| High-Level Output Voltage | $V_{OH}$ | $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OH}$=-20μA | 2.0 | 1.9 | 2.0 | - | 1.9 | - | V |
| | | | | 4.5 | 4.4 | 4.5 | - | 4.4 | - | |
| | | | | 6.0 | 5.9 | 6.0 | - | 5.9 | - | |
| | | | $I_{OH}$=-4mA | 4.5 | 4.18 | 4.31 | - | 4.13 | - | |
| | | | $I_{OH}$=-5.2mA | 6.0 | 5.68 | 5.80 | - | 5.63 | - | |
| Low-Level Output Voltage | $V_{OL}$ | $V_{IN}$=$V_{IH}$ or $V_{IL}$ | $I_{OL}$=20μA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | V |
| | | | | 4.5 | - | 0.0 | 0.1 | - | 0.1 | |
| | | | | 6.0 | - | 0.0 | 0.1 | - | 0.1 | |
| | | | $I_{OL}$=4mA | 4.5 | - | 0.17 | 0.26 | - | 0.33 | |
| | | | $I_{OL}$=5.2mA | 6.0 | - | 0.18 | 0.26 | - | 0.33 | |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$=$V_{CC}$ or GND | | 6.0 | - | - | ±0.1 | - | ±1.0 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{IN}$=$V_{CC}$ or GND | | 6.0 | - | - | 4.0 | - | 40.0 | |

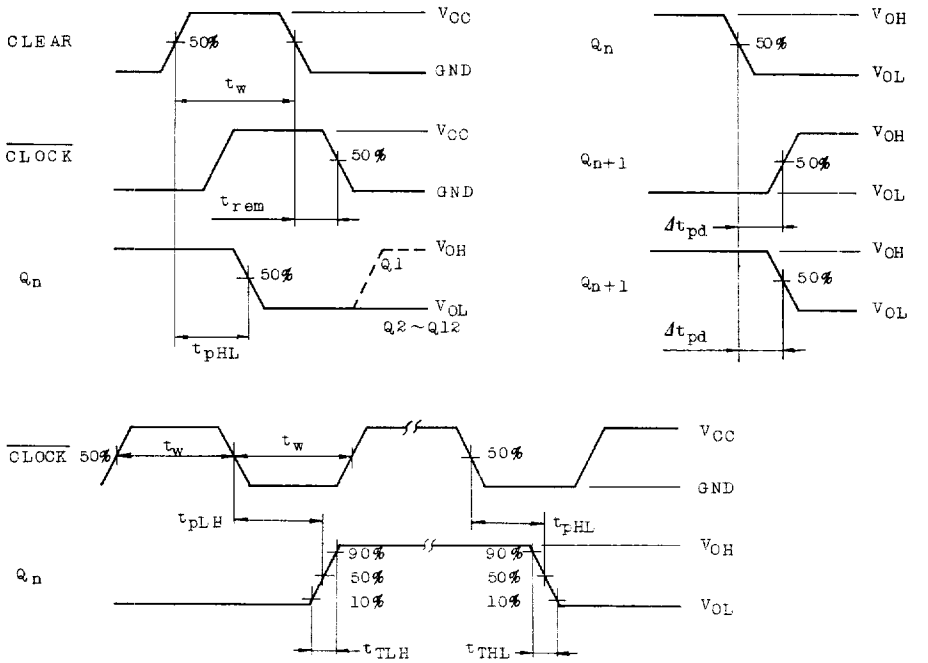
AC ELECTRICAL CHARACTERISITCS ($C_L$=50pF, Input $t_r=t_f$=6ns)

| PARAMETER | SYMBOL | TEST CONDITION | | Ta=25°C | | | Ta=-40~85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ | MIN. | TYP. | MAX. | MIN. | MAX. | |
| Output Transition Time | $t_{TLH}$ $t_{THL}$ | | 2.0 | - | 30 | 75 | - | 95 | ns |
| | | | 4.5 | - | 8 | 15 | - | 19 | |
| | | | 6.0 | - | 7 | 13 | - | 16 | |
| Propagation Delay Time ($\overline{CLOCK}$ - $Q_1$) | $t_{pLH}$ $t_{pHL}$ | | 2.0 | - | 72 | 145 | - | 180 | |
| | | | 4.5 | - | 18 | 29 | - | 36 | |
| | | | 6.0 | - | 15 | 25 | - | 31 | |
| Propagation Delay Time Difference ($Q_n$ - $Q_{n+1}$) | $\Delta t_{pd}$ | | 2.0 | - | 35 | 75 | - | 95 | |
| | | | 4.5 | - | 9 | 15 | - | 19 | |
| | | | 6.0 | - | 8 | 13 | - | 16 | |
| Propagation Delay Time (CLEAR) | $t_{pHL}$ | | 2.0 | - | 104 | 205 | - | 225 | |
| | | | 4.5 | - | 26 | 41 | - | 50 | |
| | | | 6.0 | - | 22 | 35 | - | 43 | |
| Maximum Clock Frequency | $f_{MAX}$ | | 2.0 | 6 | 14 | - | 5 | - | MHz |
| | | | 4.5 | 30 | 55 | - | 24 | - | |
| | | | 6.0 | 35 | 65 | - | 28 | - | |
| Minimum Pulse Width ($\overline{CLOCK}$) | $t_{w(L)}$ $t_{w(H)}$ | | 2.0 | - | 30 | 75 | - | 95 | ns |
| | | | 4.5 | - | 8 | 15 | - | 19 | |
| | | | 6.0 | - | 7 | 13 | - | 16 | |
| Minimum Pulse Width (CLEAR) | $t_{w(H)}$ | | 2.0 | - | 60 | 125 | - | 155 | |
| | | | 4.5 | - | 15 | 25 | - | 31 | |
| | | | 6.0 | - | 13 | 21 | - | 26 | |
| Minimum Removal Time | $t_{rem}$ | | 2.0 | - | - | 50 | - | 65 | |
| | | | 4.5 | - | - | 10 | - | 13 | |
| | | | 6.0 | - | - | 9 | - | 11 | |
| Input Capacitance | $C_{IN}$ | | | - | 5 | 10 | - | 10 | pF |
| Power Dissipation Capacitance | $C_{PD(1)}$ | | | - | 32 | - | - | - | |

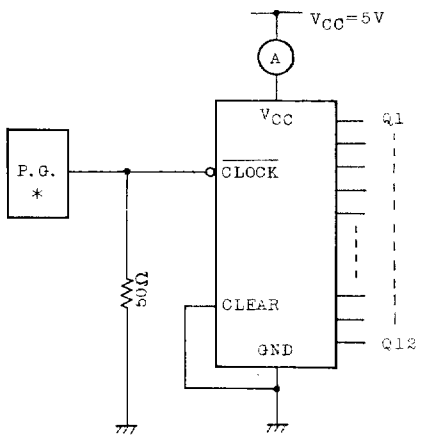
Note(1) $C_{PD}$ is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM




$I_{CC(opr.)}$ TEST CIRCUIT




* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.