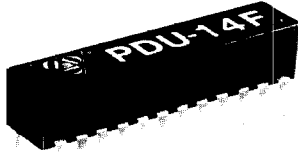


Fast Logic

Programmable Delay Units

SERIES: PDU-14F

(4 Bit) TTL Interfaced



Features:

- Input & Output TTL buffered
- 4-Bit TTL programmable delay line
- Two (2) Separate outputs; inverting and non-inverting.
- Completely interfaced
- Compact & low profile

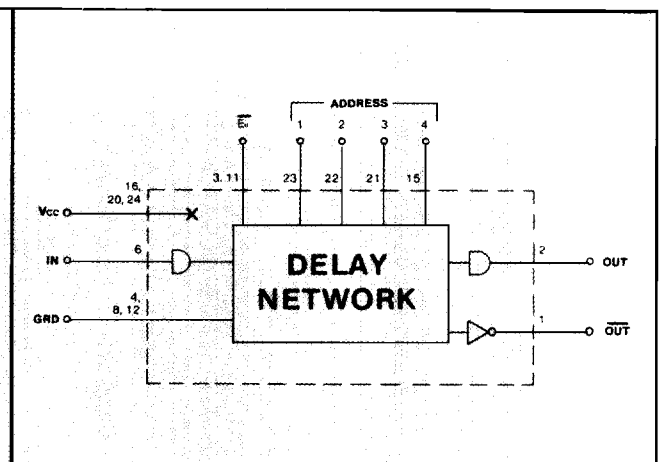
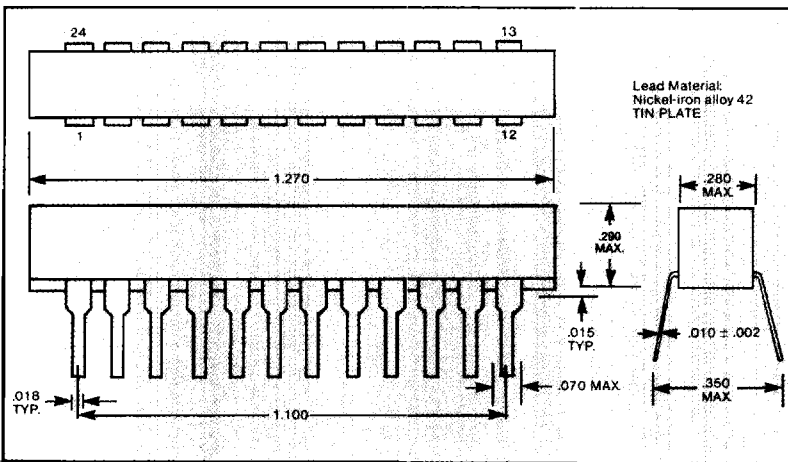
Specifications:

- Delay variation: Monotonic in one direction.
- Programmed delay tolerance: 5% or 1 ns whichever is greater.
- Inherent delay (T_{00}): 9 ns on pin 2 } typical
8 ns on pin 1 }
- Propagation delay:
Address to output (T_{SUA}) 7 ns typ.
Enable to output (T_{SUE}) 6 ns typ.
- Supply voltage: 5 Vdc \pm 5%.
- Operating temperature: 0-70 °C.
- Temperature coefficient: 100 PPM/°C.
- DC parameters: See TTL-Fast Schottky Logic Table on Page 6.

- Supply current: I_{CCM} = 74 ma.
 I_{CCL} = 30 ma.
- Minimum pulse-width = 10% of total delay.

Test Conditions:

- Input pulse-width: 150% of Max. delay.
- Input pulse spacing: 3 times of Max. delay.
- Input pulse voltage: TTL logic.
- Measurements taken at T_a = 25 °C; V_{CC} = 5V.



TRUTH TABLE

Enable (E_0)	Address				Delay Out
	4	3	2	1	
0	0	0	0	0	T_0
0	0	0	0	1	T_1
0	0	0	1	0	T_2
0	0	0	1	1	T_3
0	0	1	0	0	T_4
0	0	1	0	1	T_5
0	0	1	1	0	T_6
0	0	1	1	1	T_7
0	1	0	0	0	T_8
0	1	0	0	1	T_9
0	1	0	1	0	T_{10}
0	1	0	1	1	T_{11}
0	1	1	0	0	T_{12}
0	1	1	0	1	T_{13}
0	1	1	1	0	T_{14}
0	1	1	1	1	T_{15}
1	ϕ	ϕ	ϕ	ϕ	0

Part No.	Incremental Delay Per Step (ns)	Total Programmed Delay (ns)
PDU-14F-5	.5 \pm .3	7.5
PDU-14F-1	1 \pm .5	15
PDU-14F-2	2 \pm .5	30
PDU-14F-3	3 \pm 1.0	45
PDU-14F-4	4 \pm 1.0	60
PDU-14F-5	5 \pm 1.0	75
PDU-14F-6	6 \pm 1.0	90
PDU-14F-8	8 \pm 1.0	120
PDU-14F-10	10 \pm 1.5	150
PDU-14F-12	12 \pm 1.5	180
PDU-14F-15	15 \pm 1.5	225
PDU-14F-20	20 \pm 2.0	300
PDU-14F-25	25 \pm 2.5	375
PDU-14F-30	30 \pm 3.0	450
PDU-14F-35	35 \pm 3.5	525
PDU-14F-40	40 \pm 4.0	600
PDL-14F-45	45 \pm 4.5	675
PDL-14F-50	50 \pm 5.0	750
PDU-14F-60	60 \pm 6.0	900
PDU-14F-80	80 \pm 8.0	1,200
PDU-14F-100	100 \pm 10.0	1,500

0 Logic 0 1 Logic 1 ϕ Don't care.
 T_0 Reference or inherent delay of unit.
 $T_1 \rightarrow T_{15}$ Multiplier of incremental delay.