Ordering number : ENA1186

SANYO Semiconductors
DATA SHEET

LC749880T — CMOS IC Silicon gate Image controller LSI for LCD-TV

Overview

LC749880T is an LSI to display the converted NTSC/PAL analog video signals in the liquid crystal panel of maximum VGA size.
This product performs A/D conversion, YC separation, color decoding, IP conversion, resolution conversion, and various enhancements according to the panel.
When combined with a microcomputer and LCD panel, this product can readily makes up a video signal processing circuit for flat panel display

Features

(1) Analog input
- 3ch A/D converter incorporated
- CVBS, S-Video,YCbCr/YPbPr input

(2) YC separation video decoder
- Adaptive 3-line comb filter
- AGC, ACC

(3) Resolution conversion
- Interlace - progressive conversion
- Expansion/compression possible independently in horizontal and vertical directions

(4) Enhancing functions
- Adjusting the TV picture quality: Contour correction, color, hue, luminance, contrast
- Adjusting the panel display picture quality: White balance, black balance,γ correction
- Color exciter (6-phase RGBYMC independent saturation adjustment)
- Shadow adjuster (emphaizing the three-dimensionality)
- Dither (8bit/6bit)

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(5) Panel interface
- Video signal of either RGB 24-bit (single phase) or 18-bit signal output
- Timing controller output for panel driver

(6) Others
- OSD I/F: R, G, B, EN
- Clock generator (PLL) incorporated
- I^2C bus interface incorporated

LSI Specifications
- Supply voltage Core: 1.8V, I/O block: 3.3V
- Maximum operating frequency: 27MHz
- Package: TQFP120

Principal Applications
- LCD TV

Analog Input
CVBS×2ch: Composite video input 2channels
S-Video: S video input 1channel
YCbCr/YPbPr (480i/576i input compatible): Component input 1channel

YC Separation Video Decoder
A video decoder that converts either the NTSC/PAL video signal or component video signal into the digital video signal is incorporated, which is compatible with the composite video signal, S video signal, and component video signal (480i).

Resolution Conversion
Two-dimensional IP conversion, and expansion/contraction processings available

1. Interlace progressive conversion (IP conversion)
   Two-dimensional IP conversion possible for NTSC/PAL input
2. Horizontal vertical scaler functions
   Expansion/contraction to VGA size possible. Expansion/contraction possible independently in horizontal and vertical directions. Full-screen display and zoom display possible.

Enhancement Functions
Various enhancement functions are available. Picture quality adjustment can be made appropriate to characteristics of LCD-TV.

1. Adjusting the TV picture quality

1-1. Contour correction (horizontal vertical)
Contour correction of the input luminance signal. Adquate peaks are added around the contour.
In this case, coring adjustment is possible to prevent emphasizing of the peak amount and extremely small noises.

1-2. Color
Saturation can be adjusted by adjusting the color gain of input color-difference signal.

1-3. Hue
The hue of the screen as a whole can be adjusted.

1-4. Luminance
Luminance of the screen as a whole can be adjusted.

1-5. Contrast
Brightness of the screen as a whole can be adjusted.

2. Adjusting the panel picture quality
 2-1. White balance
  White balance adjustment appropriate to LCD-TV is possible.
 2-2. Black balance
  Black balance adjustment appropriate to LCD-TV is possible.
 2-3. γ correction
  γ correction appropriate to LCD-TV is possible. The γ correction curve may be made programmable by means of LUT γ correction can be made independently by RGB.
3. Color exciter
 A total of 12 colors including red, green, blue, magenta, yellow, cyan, and colors between these colors can be adjusted independently in terms of saturation.
4. Shadow adjuster
 The three-dimensionality can be emphasized by adding the shading through addition of the adequate peaks before and after the detected input signal contour.
5. Dither
 In the case of 6-bit output, pseudo-mulltiple tone processing enables the output equivalent to the 8-bit output.

Panel Interface

1. Video output
 Digital RGB 24-bit/18-bit output possible
2. Synchronizing signal (timing controller) output
 Timing controller output and synchronizing signal output (horizontal/vertical synchronizing signal, data enable) possible.
 The output can be selected according to specifications of LCD module.

Others

1. OSD interface
 This LSI has no OSD.
 OSD can be interfaced with the external OSD microcomputer by means of the input pin (Pin Nos.: 105 to 108) and output pin (Pin Nos.: 96,103,104).
 Interlace synchronization/progressive synchronization can be changed over according to register setting.
 The closed caption can be displayed.
2. I^2C bus interface
 The internal register is controlled by means of I^2C. The slave address can be changed over by controlling the "I^2CSEL" pin (Pin No: 33) according to the system.
 I^2CSEL "L" Slave address "88H"
 I^2CSEL "H" Slave address "8AH"

I/O Specifications

1. Input Signals

Signal type	No. of pins	Pin symbol	Description	Remarks
Video signal	1	CVBS1	Analog I/F	Composite video signal input 1
	1	CVBS2		Composite video signal input 2
	1	CRIN		Component video signal input Cr
	1	CBIN		Component video signal input Cb
	1	YIN		Component video signal input Y
	1	SY		S-Video signal input Y
	1	SC		S-Video signal input C
Synchronizing signal	1	VSI	Vertical synchronization	Vertical synchronizing signal input pin (From Sync. Sep)
	1	HSI	Horizontal synchronization	Horizontal synchronizing signal input pin (From Sync. Sep.)
OSD signal	1	BLKIN	OSD I/F	OSD signal input enable (From μ-CON)
	1	RIN		OSD signal R input pin (From μ-CON)
	1	GIN		OSD signal G input pin (From μ-CON)
	1	BIN		OSD signal B input pin (From μ-CON)

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Signal type	No. of pins	Pin symbol	Description	Remarks
Clock	1	XIN	Clock	Crystal oscillator input pin (27MHz)
	(1)	(DCLKO3)	Clock (GPIO pin)	Clock input when MODE≠0, 1
System reset	1	RESET	System reset	System reset input pin (Lo-Active)
I/F mode selection	3	MODE	I/F mode selection	I/F mode selection signal input pin 0: Two-phase 6-bit output (TCON signal output) 1: Single-phase 8-bit/6-bit output (RGB, TCON signal output) DCLKO3; 3.375MHz output 2: Single-phase 8-bit/6-bit output (RGB, TCON signal output) DCLKO3; Clock input 3,4: Decoder output (RGB/YCbCr/YC (register setting), synchronizing signal output) 5: Single-phase 8-bit/6-bit output (RGB, synchronizing signal output) * Others not applicable because they are not defined.

2. Output Signals

Signal type	No. of pins	Pin symbol	Description	Remarks
Video signal	(36)	(VP)	Digital I/F (GPIO pin)	Video signal output pin. MODE pin. Pin function changed through register setting. 6-bit output for output after dither processing For single-phase 8-bit output(MODE≠0) VP00 to VP07: R0 to R7(Cb0 to Cb7) VP08 to VP15: B0 to B7(Cb0 to Cr7/CbCr0 to CbCr7) VP16 to VP23: G0 to G7(Y0 to Y7) * ( ) shows the YCbCr 4:4:4/4:2:2 output (MODE=3,4) For single-phase 6-bit output (MODE≠0) VP00 to VP05: R0 to R5 VP08 to VP13: B0 to B5 VP16 to VP21: G0 to G5 For two-phase 6-bit output (MODE=0) VP00 to VP05: RO0 to RO5 VP18 to VP23: RE0 to RE5 VP06 to VP11: BO0 to BO5 VP24 to VP29: BE0 to BE5 VP12 to VP17: GO0 to GO5 VP30 to VP35: GE0 to GE5 * xO: Odd-numbered picture elements xE: Even-numbered picture elements
	1	SVO	Analog I/F	Internal analog video signal output
Synchronizing signal	(1)	(TIM1)	Vertical synchronizing (GPIO pin)	Applicable when MODE=3, 4, and 5. Synchronizing period, Polarity reversal possible
	(1)	(TIM2)	Horizontal synchronization (GPIO pin)	Applicable when MODE≠0. Synchronizing period. Polarity reversal possible
Data enable signal	(1)	(TIM0)	Data enable (GPIO pin)	Applicable when MODE=3, 4, and 5. H,V composite data enable output. Position, polarity reversal possible

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Signal type	No. of pins	Pin symbol	Description	Remarks
TCON signal	(1)	(GRST)	TCON signal (GPIO pin)	When MODE=0, the gate reset signal output/clamp pulse output/PWM3 output selectable through register selection When MODE≠0, the gate reset signal output/clamp pulse output selectable through register selection GRST: Pulse width, position, and polarity reversal possible
	1	FLM		When MODE=0, 1, and 2, gate start pulse signal output Pulse width, position, polarity reversal possible. Hi-Z when FLM2 is used
	1	OE		When MODE=0, 1, and 2, gate output enable signal output. Pulse width, position, polarity reversal possible.
	1	CPV		When MODE=0, 1, and 2, gate clock signal output. Pulse width, position, polarity reversal possible.
	1	STRB		When MODE=0, 1, and 2, source strobe signal output. Pulse width, position, polarity reversal possible.
	1	SP		When MODE=0, 1, and 2, source start pulse signal output. Pulse width, position, polarity reversal possible. Hi-Z when SP2 is used
	1	DEXR		When MODE=0, 1, and 2, source picture element reversal signal output. When MODE=0, DEXR output of odd-numbered picture elements
	1	POL		When MODE=0, 1, and 2, source voltage polarity selection signal output. Position adjustment, 1 line/2 line reversal and 1 frame/2 frame reversal possible
	(1)	(TIM0)		When MODE=0, 1, and 2, FLM2 output through register setting Pulse width, position, polarity reversal possible. Hi-Z when FLM is used
	(1)	(TIM1)		When MODE=0,1, and 2, SP2 output through register setting Pulse width, position, polarity reversal possible. Hi-Z when SP2 is used
	(1)	(TIM2)		When MODE=0, DEXR (DEXR_E) output of even-numbered picture elements
Clock	1	DCLKO	Dot clock	Picture element clock output. Polarity reversal, 1/2 output possible
	1	(DCLKO3)	Clock	When MODE=0 and 1, clock output (3.357MHz)
	1	XOUT		Crystal oscillator output pin
For OSD signal	1	VSO	OSD I/F	Vertical synchronizing signal output for OSD (To μ-CON) Pulse width, position, polarity reversal possible.
	1	HSO		Horizontal synchronizing signal output for OSD (To μ-CON) Pulse width, position, polarity reversal possible.
	1	DCLKO2		Picture-element clock output for OSD (To μ-CON) Polarity reversal, 1/2 output possible
PWM output	(1)	(VP32)	PWM signal (GPIO pin)	When MODE≠0, PWM1 output through register setting. Pulse width, position, polarity reversal possible.
	(1)	(VP35)		When MODE≠0, PWM2 output/PWM3 output/clamp pulse output selectable through register setting. PWM2, 3: Pulse width, position, polarity reversal possible.
	(1)	(GRST)		When MODE=0, PWM3 output/GRST output/clamp pulse output selectable through register setting PWM3: Pulse width, position, polarity reversal possible.
Clamp pulse	(1)	(VP35)	Clamp pulse (GPIO pin)	When MODE≠0, clamp pulse output/PWM2 output/PWM3 output selectable through register setting Clamp pulse: Pulse width and position adjustment possible.
	(1)	(GRST)		When MODE=0, clamp pulse output/GRST output/PWM3 output selectable through register setting. When MODE≠0, clamp pulse output/GRST output selectable through register setting Clamp pulse: Pulse width and position adjustment possible.

* The signals in parentheses show that one pin has multiple functions or acts as the I/O pin.
  Selection can be made with the MODE pin or through register setting.

3. Control Signal

Signal type	No. of pins	Pin symbol	Description	Remarks
I^2C bus	1	I^2CSEL	Slave changeover	I^2C BUS bus slave address setting (normally “L”) “L”: 88_H, “H”: $8A_H$
	1	SDA	Data bus	Slave address for internal register setting and internal status output: ”1000100+(R/W)”
	1	SCL	Bus clock	

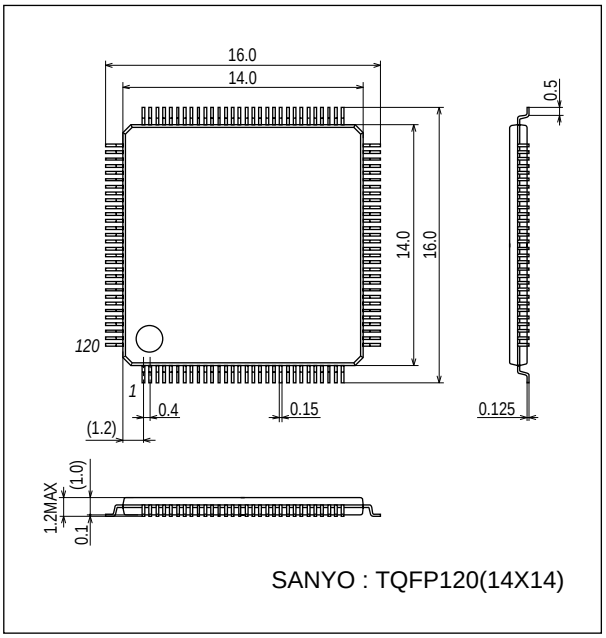
4. Other Signals

Signal type	No. of pins	Pin symbol	Description	Remarks
SCAN test	1	SCANEN	SCAN test	Test pin (Normally, ”L”)
	1	SCANMOD		Test pin (Normally, ”L”)
Test	1	TEST	Test	Test pin (Normally, ”L”)
ADC/AFE	3	VRT	ADC/AFE	ADC top level reference output
	3	VRB		ADC bottom level reference output
	1	NBIAS		ADC bias voltage output
	1	VREF		ADC reference output
AGC	1	VRTC	AGC	AGC control voltage input
	1	LPFO		AGC PWM output
	1	$LPFV_{DD}$		AGC PWM output buffer power supply
PLL	1	CHAGPUP	PLL	Charge pump output for built-in PLL
	1	VCOR		Range resistor for built-in PLL

Package Dimensions

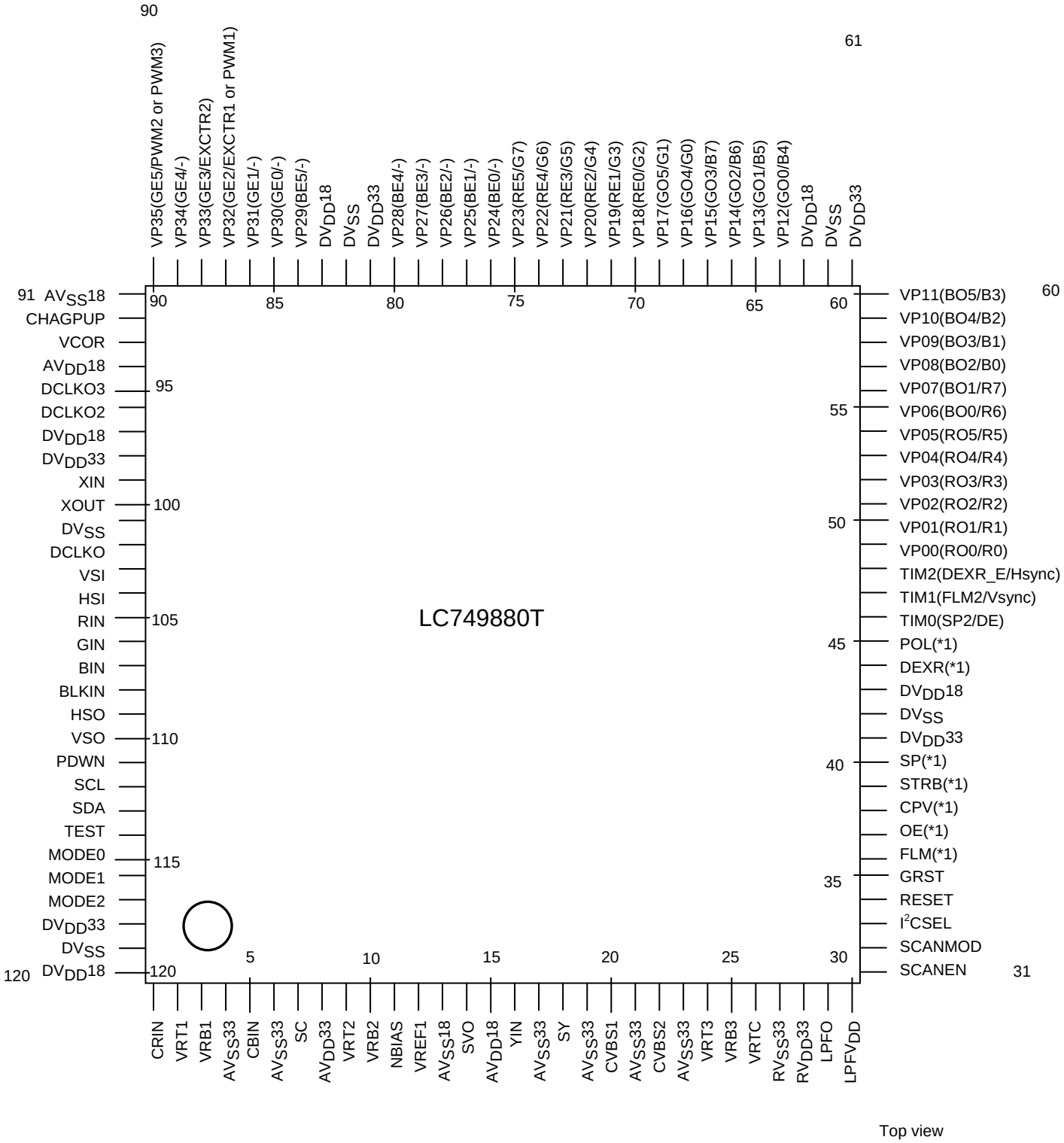
unit : mm (typ)

3257A



SANYO : TQFP120(14X14)

Pin Assignment



Top view

*1: NC for the mode in which built-in TCON is not to be used.

Pin Functions

Pin No.	Pin symbol	I/O format		Connected to	Remarks
		I/O	Format		
1	CRIN	I	A	Analog IF	Analog CR input (ADC1)
2	VRT1	O	A		Top level reference voltage connection pin for ADC1
3	VRB1	O	A		Bottom level reference voltage connection pin for ADC1
4	$AV_{SS}33$	P		Analog GND	
5	CBIN	I	A	Analog IF	Analog CB input (or S-C) (ADC2)
6	$AV_{SS}33$	P		Analog GND	
7	SC	I	A	Analog IF	Analog S-C input (ADC2)
8	$AV_{DD}33$	P		Analog 3.3V	
9	VRT2	O	A		Top level reference voltage connection pin for ADC2
10	VRB2	O	A		Bottom level reference voltage connection pin for ADC2
11	NBIAS	O	A		Bias voltage connection pin for ADC
12	VREF1	O	A		Reference voltage connection pin for ADC
13	$AV_{SS}18$	P		Analog GND	
14	SVO	O	A		ADC3 input internal analog video signal output
15	$AV_{DD}18$	P		Analog 1.8V	
16	YIN	I	A	Analog IF	Analog Y input (or S-Y,CVBS) (ADC3)
17	$AV_{SS}33$	P		Analog GND	
18	SY	I	A	Analog IF	Analog S-Y input (or CVBS) (ADC3)
19	$AV_{SS}33$	P		Analog GND	
20	CVBS1	I	A	Analog IF	Analog CVBS1 input (ADC3)
21	$AV_{SS}33$	P		Analog GND	
22	CVBS2	I	A	Analog IF	Analog CVBS2 input (ADC3)
23	$AV_{SS}33$	P		Analog GND	
24	VRT3	O	A		Top level reference voltage connection pin for ADC3
25	VRB3	O	A		Bottom level reference voltage connection pin for ADC3
26	VRTC	I	A		AGC control voltage input
27	$RV_{SS}33$	P		Analog GND	VREF generator circuit analog GND
28	$RV_{DD}33$	P		Analog 3.3V	VREF generator circuit analog 3.3V
29	LPFO	O	A		AGC PWM output
30	$LPFV_{DD}$	I	A		AGC PWM output buffer power supply
31	SCANEN	I	C		Test pin (Normally, Lo)
32	SCANMOD	I	C		Test pin (Normally, Lo)
33	I^2CSEL	I	C		I^2C slave addresses L=0×88, H=0×8A
34	RESET	I	B		System reset (Active Lo)
35	GRST	I/O	G		Gate reset signal (or test input)
36	FLM	I/O	G		Gate start signal (or test input)
37	OE	I/O	G		Gate OE signal (or test input)
38	CPV	I/O	G		Gate lock signal (or test input)
39	STRB	I/O	G		Source strobe signal (or test input)
40	SP	I/O	G		Source start signal (or test input)
41	$DV_{DD}33$	P		Digital 3.3V	
42	DV_{SS}	P		Digital GND	
43	$DV_{DD}18$	P		Digital 1.8V	
44	DEXR	I/O	G		Source picture element reversal signal (or test input)
45	POL	I/O	G		Source line reversal signal (or test input)
46	TIM0	O	E		Data enable signal output/FLM2 (register selection)
47	TIM1	O	E		Vertical synchronizing signal output/SP2 (register selection)
48	TIM2	O	E		Horizontal synchronizing signal output
49	VP00	O	E		Video signal output R0/R_ODD_0 (MODE pin select=0)
50	VP01	O	E		Video signal output R1/R_ODD_1 (MODE pin select=0)
51	VP02	O	E		Video signal output R2/R_ODD_2 (MODE pin select=0)

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Pin No.	Pin symbol	I/O format		Connected to	Remarks
		I/O	Format		
52	VP03	O	E		Video signal output R3/R_ODD_3 MODE pin select=0)
53	VP04	O	E		Video signal output R4/R_ODD_4 (MODE pin select=0)
54	VP05	O	E		Video signal output R5/R_ODD_5 (MODE pin select=0)
55	VP06	O	E		Video signal output R6/B_ODD_0 (MODE pin select=0)
56	VP07	O	E		Video signal output R7/B_ODD_1 (MODE pin select=0)
57	VP08	O	E		Video signal output B0/B_ODD_2 (MODE pin select=0)
58	VP09	O	E		Video signal output B1/B_ODD_3 (MODE pin select=0)
59	VP10	O	E		Video signal output B2/B_ODD_4 (MODE pin select=0)
60	VP11	O	E		Video signal output B3/B_ODD_5 (MODE pin select =0)
61	$DV_{DD}33$	P		Digital 3.3V	
62	DV_{SS}	P		Digital GND	
63	$DV_{DD}18$	P		Digital 1.8V	
64	VP12	O	E		Video signal output B4/G_ODD_0 (MODE pin select=0)
65	VP13	O	E		Video signal output B5/G_ODD_1 (MODE pin select=0)
66	VP14	O	E		Video signal output B6/G_ODD_2 (MODE pin select=0)
67	VP15	O	E		Video signal output B7/G_ODD_3 (MODE pin select=0)
68	VP16	O	E		Video signal output G0/G_ODD_4 (MODE pin select=0)
69	VP17	O	E		Video signal output G1/G_ODD_5 (MODE pin select=0)
70	VP18	O	E		Video signal output G2/R_EVEN_0 (MODE pin select=0)
71	VP19	O	E		Video signal output G3/R_EVEN_1 (MODE pin select=0)
72	VP20	O	E		Video signal output G4/R_EVEN_2 (MODE pin select=0)
73	VP21	O	E		Video signal output G5/R_EVEN_3 (MODE pin select=0)
74	VP22	O	E		Video signal output G6/R_EVEN_4 (MODE pin select=0)
75	VP23	O	E		Video signal output G7/R_EVEN_5 (MODE pin select=0)
76	VP24	I/O	G		-/Video signal output B_EVEN_0 (MODE pin select=0)
77	VP25	I/O	G		-/Video signal output B_EVEN_1 (MODE pin select=0)
78	VP26	I/O	G		-/Video signal output B_EVEN_2 (MODE pin select=0)
79	VP27	I/O	G		-/Video signal output B_EVEN_3 (MODE pin select=0)
80	VP28	I/O	G		-/Video signal output B_EVEN_4 (MODE pin select=0)
81	$DV_{DD}33$	P		Digital 3.3V	
82	DV_{SS}	P		Digital GND	
83	$DV_{DD}18$	P		Digital 1.8V	
84	VP29	I/O	G		-/Video signal output B_EVEN_5 (MODE pin select=0)
85	VP30	I/O	G		-/Video signal output G_EVEN_0 (MODE pin select=0)
86	VP31	I/O	G		-/Video signal output G_EVEN_1 (MODE pin select=0)
87	VP32	I/O	G		-/Video signal output G_EVEN_2 (MODE pin select=0)
88	VP33	I/O	G		-/Video signal output G_EVEN_3 (MODE pin select=0)
89	VP34	I/O	G		PWM signal/Video signal output G_EVEN_4 (MODE pin select=0)
90	VP35	I/O	G		PWM signal/Video signal output G_EVEN_5 (MODE pin select=0)
91	$AV_{SS}18$	P		Analog GND	
92	CHAGPUP	O	A		Charge pump output
93	VCOR	I	A		Range resistor for PLL
94	$AV_{DD}18$	P		Analog 1.8V	
95	DCLKO3	I/O	H		Clock I/O
96	DCLKO2	O	F		Clock output (dedicated to microcomputer, with 1/2 or DE)
97	$DV_{DD}18$	P		Digital 1.8V	
98	$DV_{DD}33$	P		Digital 3.3V	
99	XIN	I	D		Crystal oscillator connection pin (27MHz)
100	XOUT	O			Crystal oscillator connection pin
101	DV_{SS}	P		Digital GND	
102	DCLKO	O	F		Panel clock output
103	VSI	I	B		Vertical synchronizing signal input
104	HSI	I	B		Horizontal synchronizing signal input

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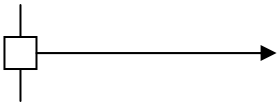
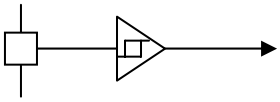
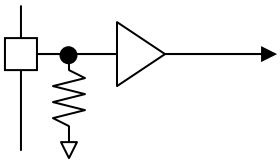
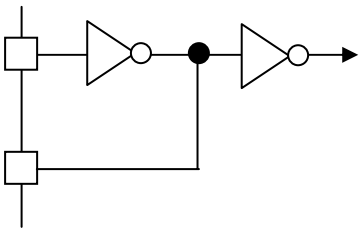
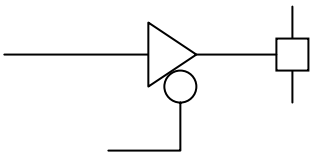
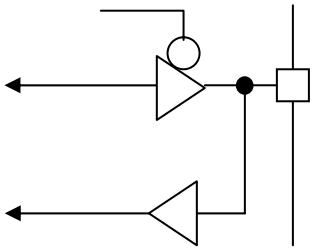
Pin No.	Pin symbol	I/O format		Connected to	Remarks
		I/O	Format		
105	RIN	I	C		R input of microcomputer OSD
106	GIN	I	C		G input of microcomputer OSD
107	BIN	I	C		B input of microcomputer OSD
108	BLKIN	I	C		BLK input of microcomputer OSD
109	HSO	O	E		Horizontal synchronizing signal output for microcomputer
110	VSO	O	E		Vertical synchronizing signal output for microcomputer
111	PDWN	I	B		Power DOWN (Active Lo)
112	SCL	I	B		I^2C bus clock
113	SDA	I/O	G		I^2C bus data
114	TEST	I	C		Test pin (normally, Lo)
115	MODE0	I	C		I/F mode pin
116	MODE1	I	C		I/F mode pin
117	MODE2	I	C		I/F mode pin
118	$DV_{DD}33$	P		Digital 3.3V	
119	DV_{SS}	P		Digital GND	
120	$DV_{DD}18$	P		Digital 1.8V	

Pin Type

I/O type	Function	Equivalent circuit	Applicable pins
A	Analog I/O		CRIN, VRT1, VRB1, CBIN, SC, VRT2, VRB2, NBIAS, VREF1, SVO, YIN, SY, CVBS1, CVBS2, VRT3, VRB3, VRTC, LPFO, LPFVDD, CHAGPUP, VCOR
B	5V withstand Schmidt trigger CMOS input*		RESET, VSI, HSI, PDWN, SCL
C	5V withstand With Pull-down CMOS input*		SCANEN, SCANMOD, I^2CSEL, RIN, GIN, BIN, BLKIN, TEST, MODE0, MODE1, MODE2
D	Oscillator circuit I/O		XIN, XOUT
E	8mA 3-STATE drive CMOS output*		TIM0, TIM1, TIM2, VP00, VP01, VP02, VP03, VP04, VP05, VP06, VP07, VP08, VP09, VP10, VP11, VP12, VP13, VP14, VP15, VP16, VP17, VP18, VP19, VP20, VP21, VP22, VP23, HSO, VSO
F	12mA 3-STATE drive CMOS output*		DCLKO2, DCLKO
G	8mA 3-STATE drive CMOS I/O*		GRST, FLM, OE, CPV, STRB, SP, DEXR, POL, VP24, VP25, VP26, VP27, VP28, VP29, VP30, VP31, VP32, VP33, VP34, VP35, SDA
H	12mA 3-STATE drive CMOS I/O*		DCLKO3

*: 5V Tolerant

Electrical Characteristics

Absolute Maximum Ratings at Ta = 25°C, DV_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Rating	Unit
Maximum supply voltage (I/O)	$DV_{DD}33$ $AV_{DD}33$	-0.3 to +4.0	V
Maximum supply voltage (core)	$DV_{DD}18$ $AV_{DD}18$	-0.3 to +2.2	V
Digital input voltage	V_I	-0.5 to 6.0	V
Digital output voltage	V_O	-0.3 to V_{DD} + 0.3	V
Storage temperature	Tstg	-55 to +125	°C
Operating temperature	Topr	-30 to +70	°C
Maximum allowable loss	Pd max	0.6	W

Allowable Operation Range at Ta = -30 to +70°C

Parameter	Symbol	min	typ	max	Unit
Supply voltage (I/O)	$DV_{DD}33$ $AV_{DD}33$	3.15	3.3	3.45	V
Supply voltage (core)	$DV_{DD}18$ $AV_{DD}18$	1.71	1.8	1.89	V
Input voltage range	V_{IN}	0		5.5	V

I/O Pin Capacity at Ta = 25°C, V_{DD} = V_I = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input pin	CIN	f=1MHz			10	pF
Output pin	COUT	f=1MHz			10	pF
I/O pin	CI/O	f=1MHz			10	pF

DC Characteristics at Ta = -30 to +70°C, $DV_{DD}33$ = 3.3V±5%, $DV_{DD}18$ = 1.8V±5%

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level voltage	V_{IH}	CMOS compatible	2.0		5.5	V
		CMOS compatible schmidt	2.0		5.5	V
		Oscillator circuit input	2.0		3.465	V
Input low-level voltage	V_{IL}	CMOS compatible	-0.3		+0.8	V
		CMOS compatible schmidt	-0.3		+0.8	V
		Oscillator circuit input	-0.3		+0.8	V
Input high-level current	I_{IH}	V_I=V_{DD}	-10		+10	µA
		V_I=V_{DD} with pull-down resistor	+10		+100	µA
Input low-level current	I_{IL}	V_I=V_{SS}	-10		+10	µA
Output high-level voltage	V_{OH}	CMOS	2.4			V
		Oscillator circuit output	2.4			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
		Oscillator circuit output			0.4	V
Output leak current	IOZ	At output of high-impedance	-10		+10	µA
Pull-down resistor	RDN		43	58	118	kΩ
Operating current	IDDOP	tck=27MHz				mA
Operating current ($AV_{DD}33$)	IDDOP	tck=27MHz gray scale		15		mA
Operating current ($AV_{DD}18$)		tck=27MHz gray scale		70		mA
Operating current ($DV_{DD}33$)		tck=27MHz gray scale		20		mA
Operating current ($DV_{DD}18$)		tck=27MHz gray scale		90		mA
Current drain at rest *1	IDDST	Output release,V_I=V_{SS} or V_{DD}		10		µA

*1: There is an input pin incorporating pull-down resistor. Note that, depending on circuit composition, the current drain at rest may not be guaranteed.

A/D Convertor Characteristics at Ta = -30 to +70°C, DV_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol/pin	min	typ	max	Unit
Clock frequency	Fclk			27	MHz
Clamp pulse width	Tcl	0.45			µs
External capacitance					
Analog input coupling capacitance	Analog video pin	0.01		10	µF
Top level reference fixed capacitance	VRTx pin		0.01		µF
Bottom level reference capacitance	VRBx pin		0.01		µF
VREF1 bias fixed capacitance	VREF1 pin		0.01		µF
NBIAS bias fixed capacitance	NBIAS pin		0.01		µF
Analog input frequency	FAIN			4	MHz
Analog input amplitude (Max amplitude)					
In the non-AGC operation mode	FS1AIN			1.0	Vp-p
In the AGC operation mode *1	FS2AIN	0.6		1.1	Vp-p
ADC reference input voltage					
In the non-AGC operation mode					
Bottom level reference input	VRBI		0.65		V
In the AGC operation mode					
Bottom level reference input	VRBI		0.65		V

DC Characteristics at Ta=25°C, $V_{DD}3$=3.3V±5%,V_{DD}=1.8V±5%, DV_{SS} = 0V, AV_{SS} = 0V

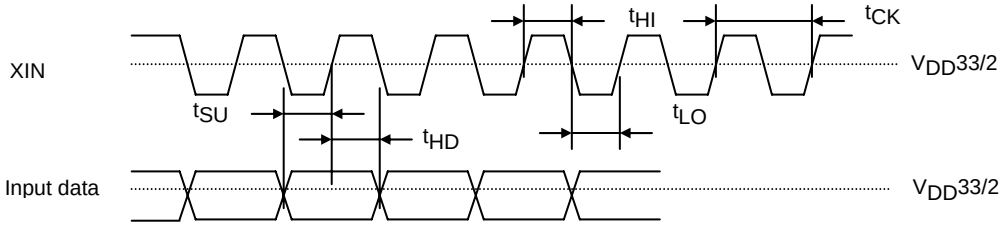
Parameter	Symbol	Conditions	min	typ	max	Unit
Operating supply current 3.3V power supply	$I_{DD}3$	$V_{DD}3$=3.3V		16		mA
1.8V power supply	I_{DD}	V_{DD}=1.8V Fclk=27MHz		16		mA
Standby supply current 3.3V power supply	ISB3	$V_{DD}3$=3.3V	-10		+10	µA
1.8V power supply	ISB	V_{DD}=1.8V Fclk=0MHz	-10		+10	µA

ADC Conversion Characteristics at Ta=25°C,$V_{DD}3$=3.3V±5%,V_{DD}=1.8V±5%, DV_{SS} = 0V, AV_{SS} = 0V

Parameter	Symbol	Conditions	min	typ	max	Unit
Resolution	RES				10	bits

I/O Data Timing

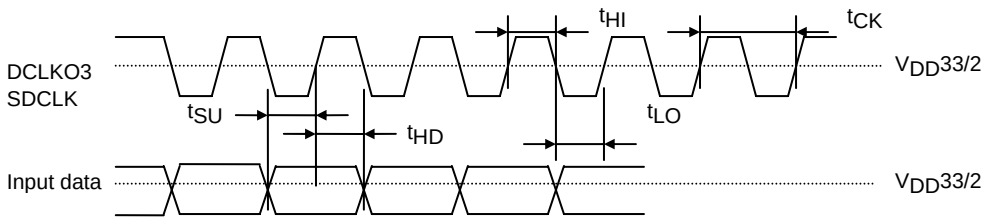
(1) Input data timing 1



Pin name	Parameter	Symbol	min	max	Unit
XIN	Clock L-level time	t_{LO}	18.5		ns
	Clock H-level time	t_{HI}	18.5		ns
	Clock cycle	t_{CK}	37		ns
VP24-34 POL, FLM, OE, CPV, STRB SP, DEXR RIN, GIN, BIN, BLKIN	Input data setup time	t_{SU}	3.5		ns
	Input data hold time	t_{HD}	3.5		ns

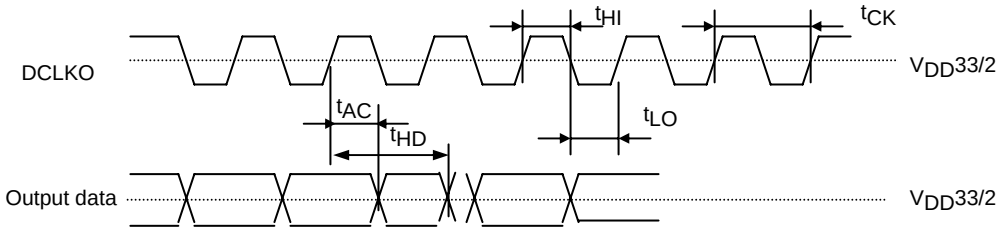
* The recommended duty ratio of input clock is 50%

(2) Input data timing 2



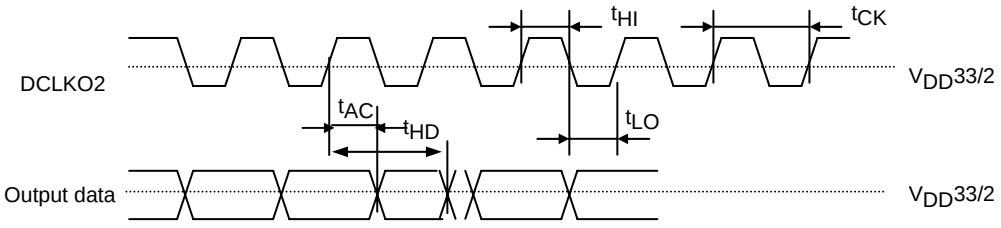
Pin name	Parameter	Symbol	min	max	Unit
DCLKO3	Clock L-level time	t_{LO}	18.5		ns
	Clock H-level time	t_{HI}	18.5		ns
	Clock cycle	t_{CK}	37		ns
VSI HSI	Input data setup time	t_{SU}	3.5		ns
	Input data hold time	t_{HD}	3.5		ns

(3) Output data timing (1)



Pin name	Parameter	Symbol	min	max	Unit
DCLKO	Clock L-level time	t_{LO}	18.5		ns
	Clock H-level time	t_{HI}	18.5		ns
	Clock cycle	t_{CK}	37		ns
VP00-31 TIM0, TIM1, TIM2 POL, FLM, OE, CPV, STRB SP, DEXR, GRST	Output data delay time	t_{AC}	-3.5	+3.5	ns
	Output data hold time	t_{HD}	30.0		ns

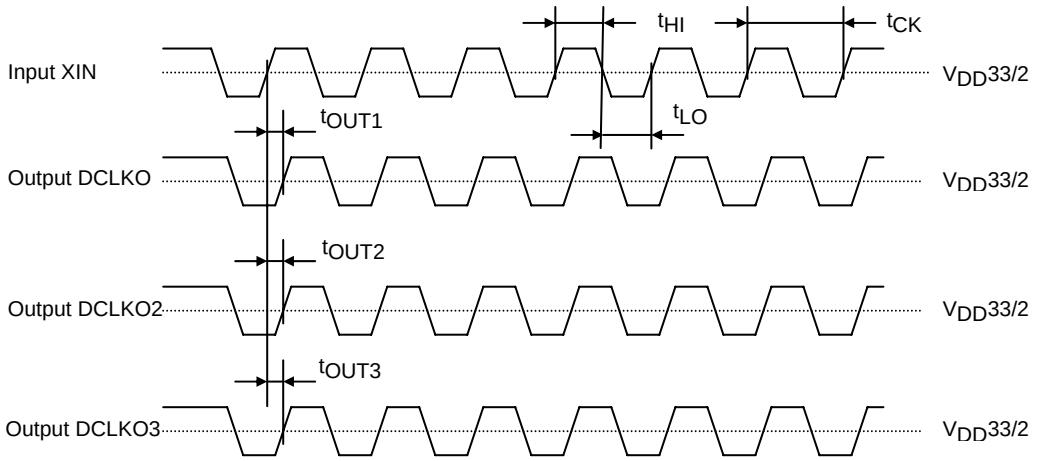
(3) Output data timing (2)



Pin name	Parameter	Symbol	min	max	Unit
DCLKO2	Clock L-level time	t_{LO}	18.5		ns
	Clock H-level time	t_{HI}	18.5		ns
	Clock cycle	t_{CK}	37		ns
VSO,HSO	Output data delay time	t_{AC}	-3.5	+3.5	ns
	Output data hold time	t_{HD}	30.0		ns

I/O Clock Timing

(1) Input system clock timing



Pin name	Parameter	Symbol	min	max	Unit
XIN	Clock L-level time	t_{LO}	18.5		ns
	Clock H-level time	t_{HI}	18.5		ns
	Clock cycle	t_{CK}	37		ns
DCLKO	DCLKO delay time	t_{OUT1}		18.5	ns
DCKLO2	DCLKO2 delay time	t_{OUT2}		18.5	ns
DCKLO3	DCLKO3 delay time	t_{OUT3}		12.5	ns

Sample Application Circuit