HAF1004(L), HAF1004(S)

Silicon P Channel MOS FET Series Power Switching

REJ03G0028-0500Z
(Previous ADE-208-629B (Z))
Rev.5.00
2003.04.29

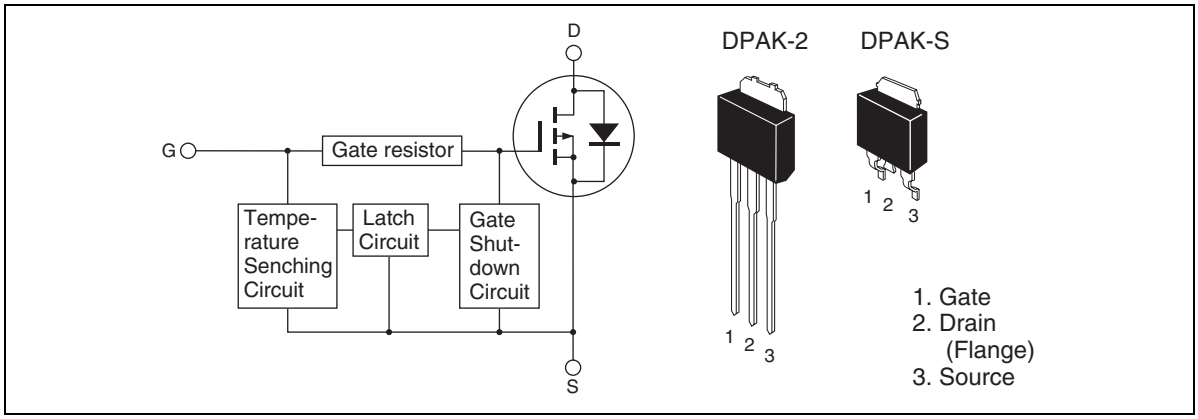
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation to (–4 to –6 V Gate drive)
- High endurance capability against to the shut-down circuit
- Built-in the over temperature shut-down circuit
- Latch type shut down operation (need 0 voltage recovery)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–60	V
Gate to source voltage	V_{GSS}	–16	V
Gate to source voltage	V_{GSS}	2.5	V
Drain current	I_D	–5	A
Drain peak current	$I_{D\ (pulse)}$ Note1	–10	A
Body-drain diode reverse drain current	I_{DR}	–5	A
Cannel dissipation	Pch Note2	20	W
Cannel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 0µs, duty cycle ≤ 1%
2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	–3.5	—	—	V	
	V_{IL}	—	—	–1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	–100	µA	Vi = –8 V, V_{DS} = 0
	I_{IH2}	—	—	–50	µA	Vi = –3.5 V, V_{DS} = 0
	I_{IL}	—	—	–1	µA	Vi = –1.2 V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	–0.8	—	mA	Vi = –8 V, V_{DS} = 0
	$I_{IH(sd)2}$	—	–0.35	—	mA	Vi = –3.5 V, V_{DS} = 0
Shut down temperature	Tsd	—	175	—	°C	Cannel temperature
Gate operation voltage	Vop	–3.5	—	–12	V	

Electrical Characteristics

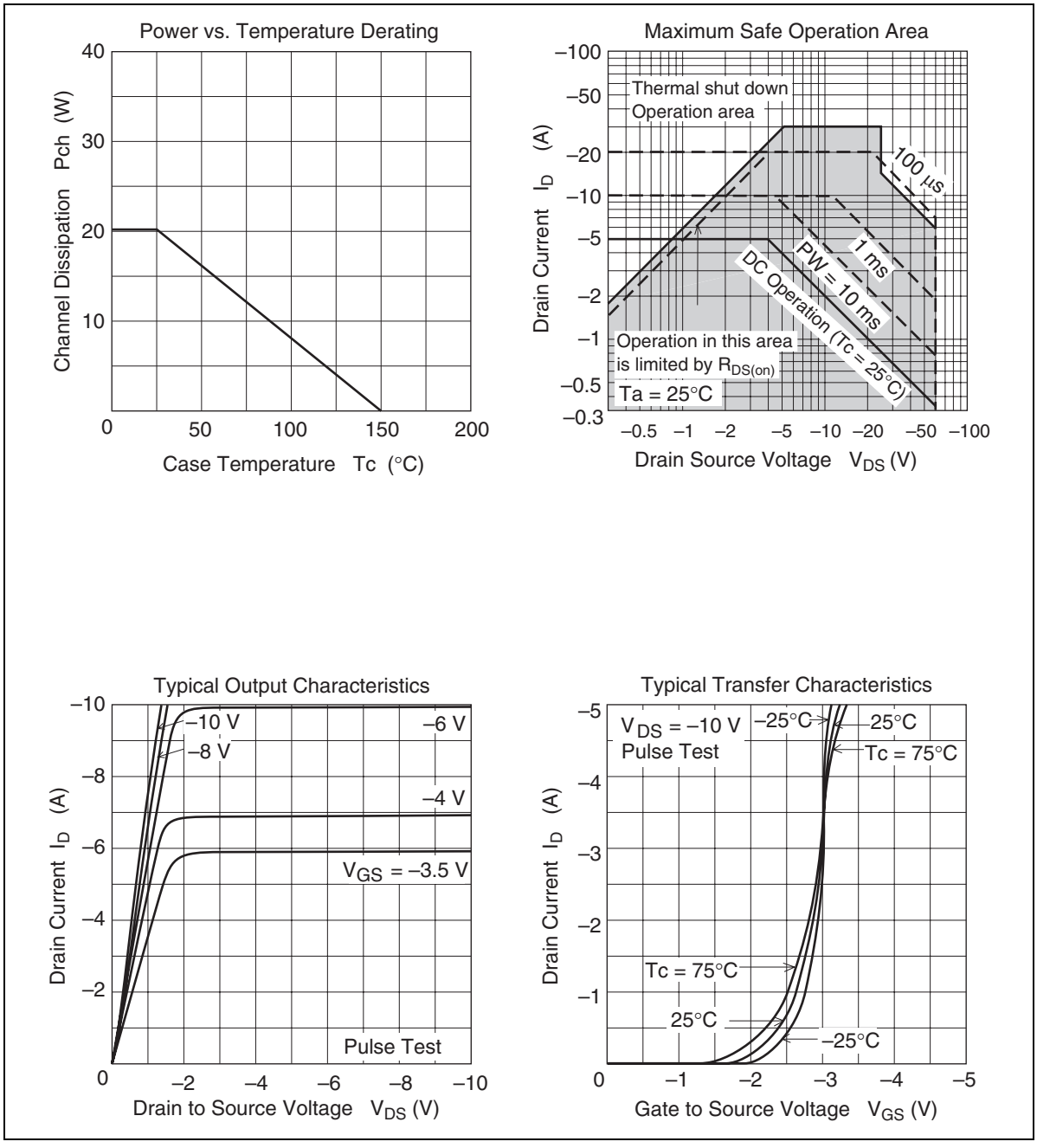
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	4	—	—	A	V_{GS} = –3.5 V, V_{DS} = –2 V
Drain current	I_{D2}	—	—	–10	mA	V_{GS} = –1.2 V, V_{DS} = –2 V
Drain to source breakdown voltage	$V_{(BR)DSS}$	–60	—	—	V	I_D = –10 mA, V_{GS} =0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–16	—	—	V	I_G = –800 µA, V_{DS} =0
Gate to source breakdown voltage	$V_{(BR)GSS}$	2.5	—	—	V	I_G = 100 µA, V_{DS} =0
Gate to source leak current	I_{GSS1}	—	—	–100	µA	V_{GS} = –8 V, V_{DS} =0
	I_{GSS2}	—	—	–50	µA	V_{GS} = –3.5 V, V_{DS} =0
	I_{GSS3}	—	—	–1	µA	V_{GS} = –1.2 V, V_{DS} =0
	I_{GSS4}	—	—	100	µA	V_{GS} = 2.4 V, V_{DS} =0
Input current (shut down)	$I_{GS(OP)1}$	—	–0.8	—	mA	V_{GS} = –8 V, V_{DS} =0
	$I_{GS(OP)2}$	—	–0.35	—	mA	V_{GS} = –3.5 V, V_{DS} =0
Zero gate voltage drain current	I_{DSS}	—	—	–10	µA	V_{DS} = –60 V, V_{GS} = 0
Gate to source cut off voltage	$V_{GS(off)}$	–1.1	—	–2.25	V	V_{DS} = –10 V, I_D = –1 mA
Forward transfer admittance	$\|y_{fs}\|$	2	4	—	S	I_D =–2.5 A, V_{DS} =–10 V [Note3]
Static drain to source on state resistance	$R_{DS(on)}$	—	140	200	mΩ	I_D = –2.5 A, V_{GS} = –10 V [Note3]
Static drain to source on state resistance	$R_{DS(on)}$	—	200	340	mΩ	I_D = –2.5 A, V_{GS} = –4 V [Note3]
Output capacitance	Coss	—	326	—	pF	V_{DS} = –10 V, V_{GS} =0, f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	2	—	µs	V_{GS} = –5 V, I_D= –2.5 A, R_L = 12 Ω
Rise time	t_r	—	7.6	—	µs	
Turn off delay time	$t_{d(off)}$	—	3.2	—	µs	
Fall time	t_f	—	3.2	—	µs	
Body-drain diode forward voltage	V_{DF}	—	–0.9	—	V	I_F = –5A, V_{GS} = 0
Body-drain diode reverse recovery time	t_{rr}	—	77	—	ns	I_F = –5 A, V_{GS} = 0 diF/dt = 50 A/µs
Over lord shut down operation time [note4]	t_{os1}	—	8.4	—	ms	V_{GS} = –5 V, V_{DD} = –16 V
	t_{os2}	—	2.4	—	ms	V_{GS} = –5 V, V_{DD} = –24 V

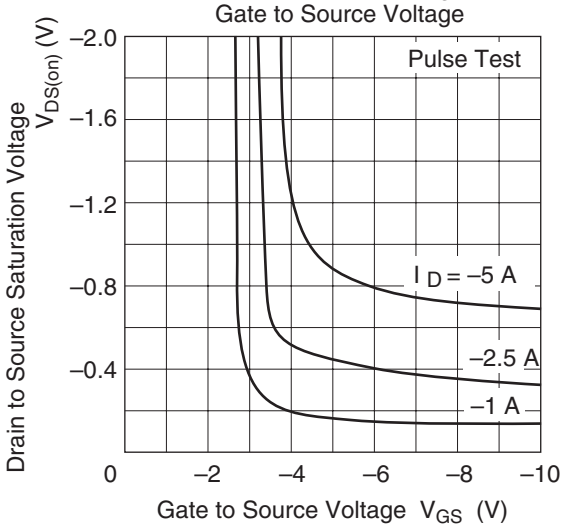
Notes: 3. Pulse test

4. Including the junction temperature rise of the lorded condition

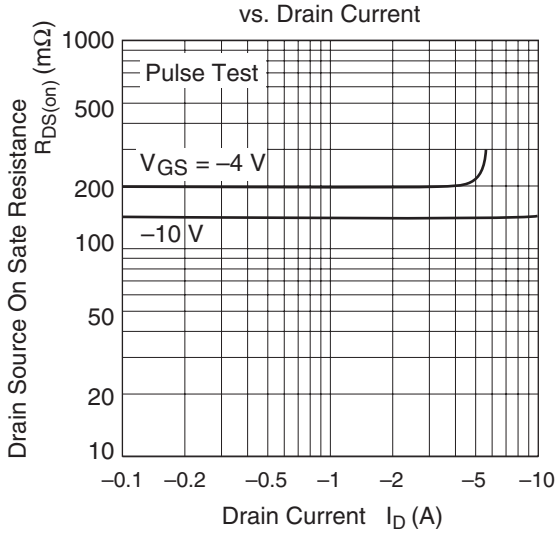
Main Characteristics



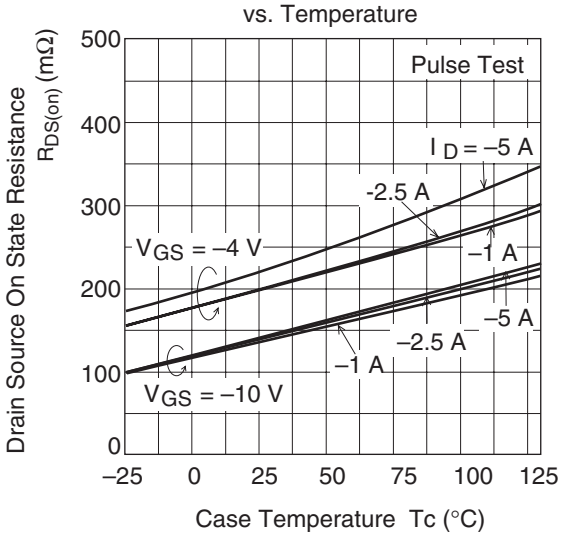
Drain to Saturation Voltage vs. Gate to Source Voltage



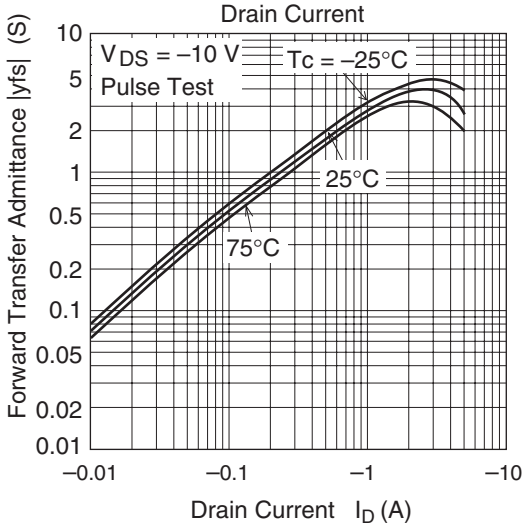
Static Drain to Source State Resistance vs. Drain Current



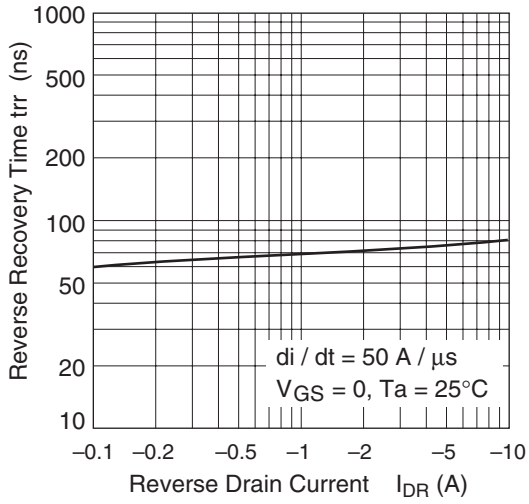
Drain to Source On State Resistance vs. Temperature



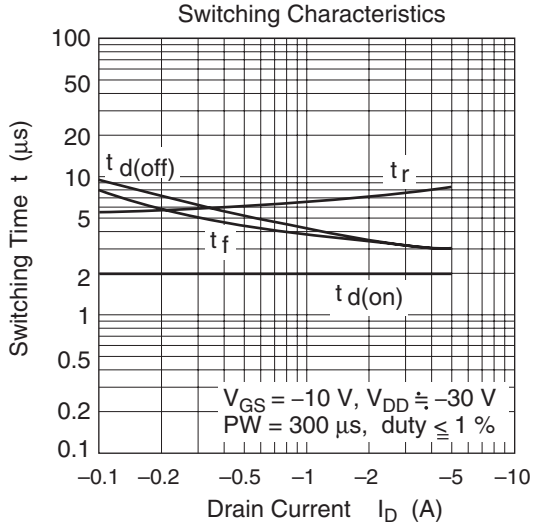
Forward Transfer Admittance vs. Drain Current



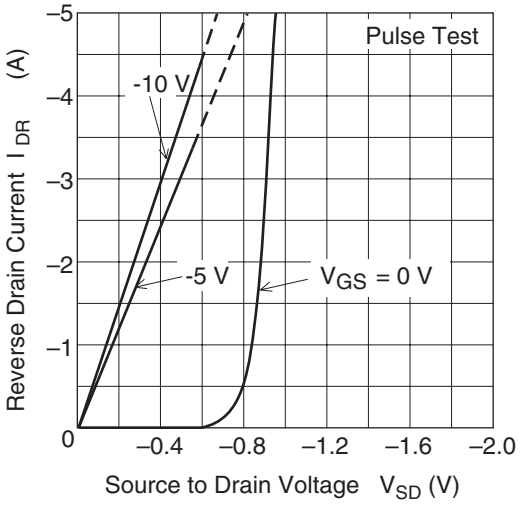
Body to Drain Diode Reverse Recovery Time



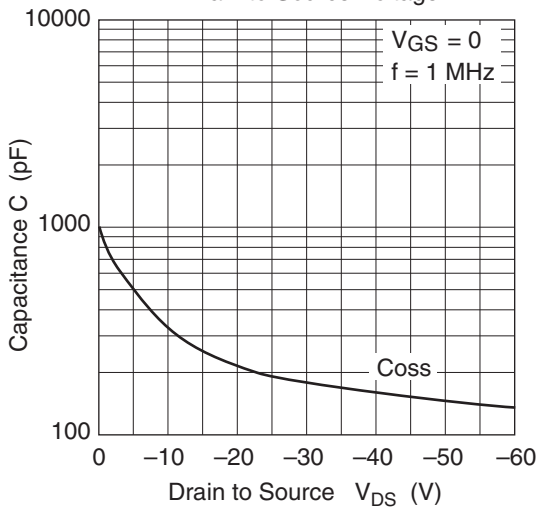
Switching Characteristics



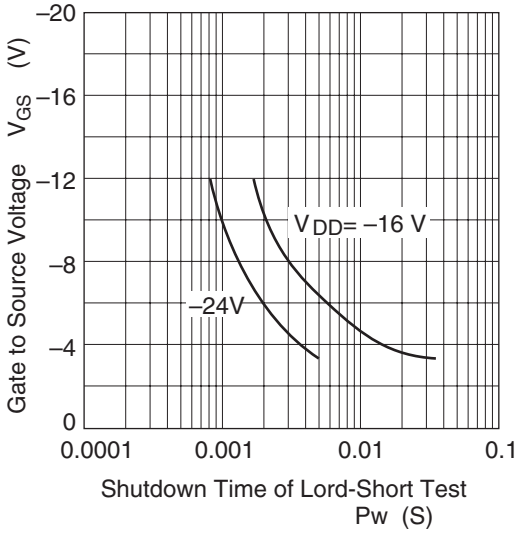
Reverse Drain Current vs. Source to Drain Voltage



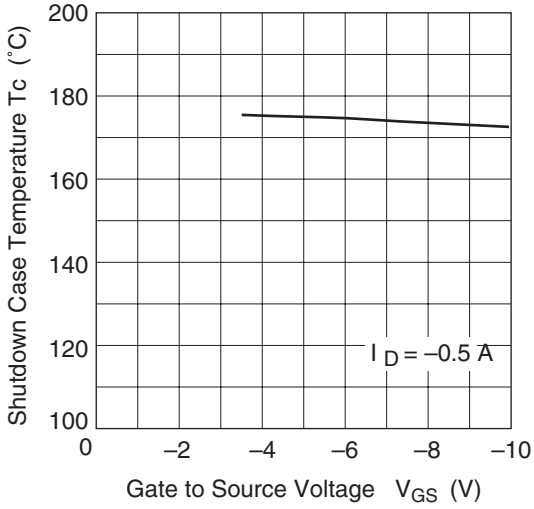
Typical capacitance vs. Drain to Source Voltage



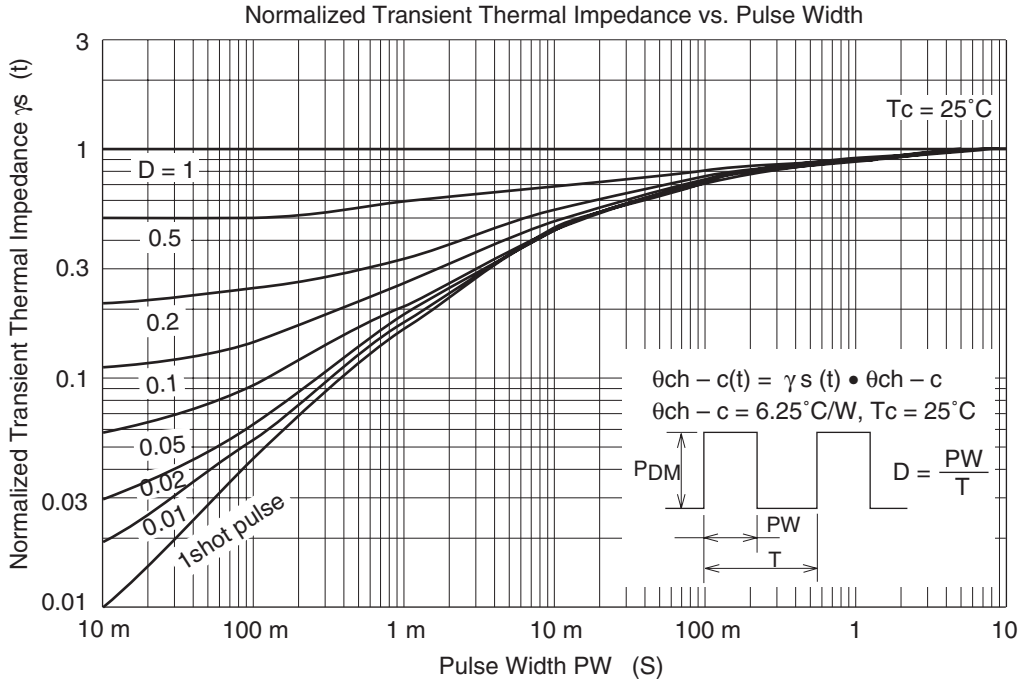
Gate to Source Voltage vs.
Shutdown Time of Load-Short Test



Shutdown Case Temperature vs.
Gate to Source Voltage



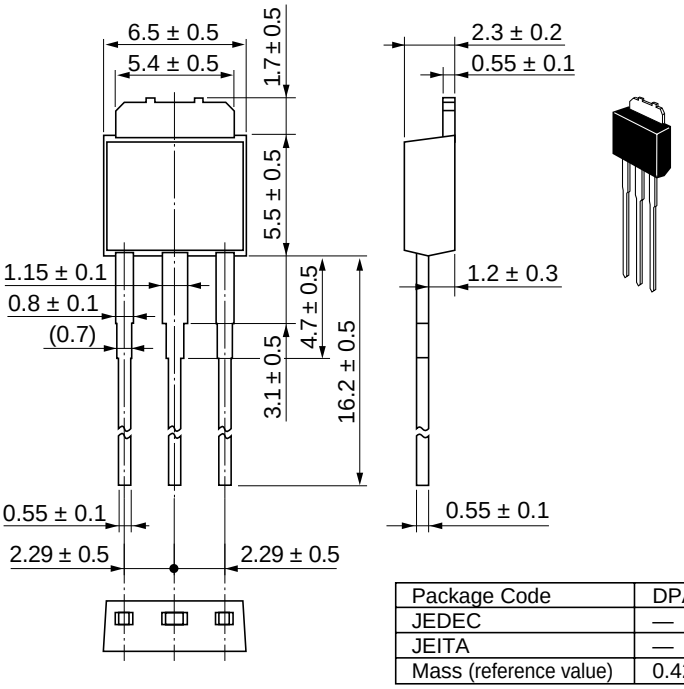
Normalized Transient Thermal Impedance vs. Pulse Width



Package Dimensions

As of January, 2003

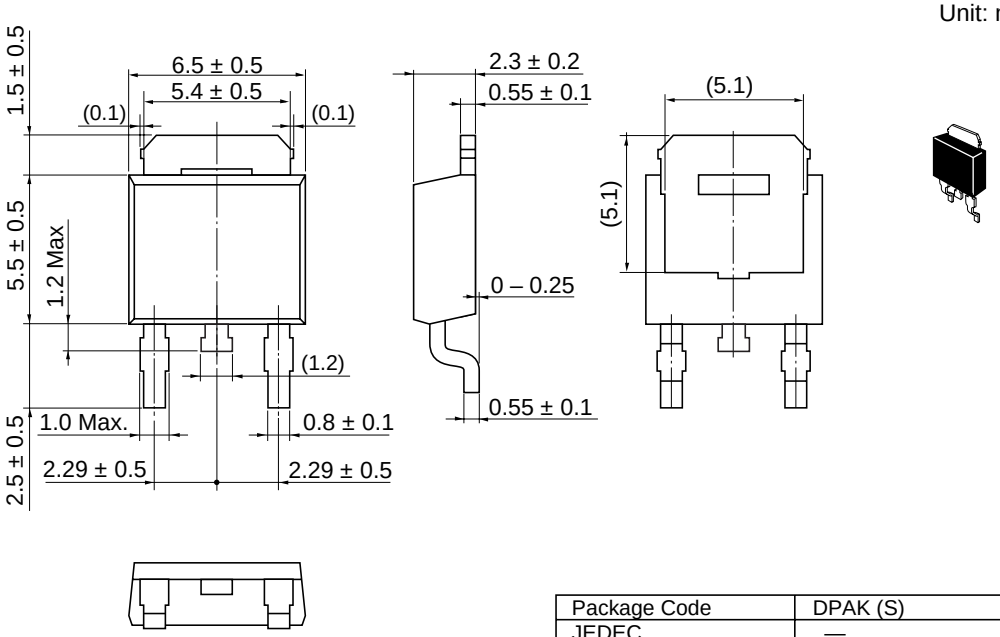
Unit: mm



Package Code	DPAK (L)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	0.42 g

As of January, 2003

Unit: mm



Package Code	DPAK (S)
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.28 g

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