**Preferred Devices** 

## **Dual Bias Resistor Transistors**

## NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base–emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT–553 package which is designed for low power surface mount applications.

#### **Features**

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- Available in 8 mm, 7 inch Tape and Reel
- Lead-Free Solder Plating
- Pb-Free Packages are Available

#### **MAXIMUM RATINGS** (T<sub>A</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current	Ic	100	mAdc

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	230 (Note 1) 338 (Note 2) 1.8 (Note 1) 2.7 (Note 2)	mW °C/W
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	540 (Note 1) 370 (Note 2)	°C/W
Thermal Resistance – Junction-to-Lead	$R_{ heta JL}$	264 (Note 1) 287 (Note 2)	°C/W
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

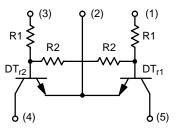
- 1. FR-4 @ Minimum Pad
- 2. FR-4 @ 1.0 x 1.0 inch Pad



#### ON Semiconductor®

http://onsemi.com

## NPN SILICON BIAS RESISTOR TRANSISTORS





SOT-553 CASE 463B

#### MARKING DIAGRAM



xx = Device Code xx= UF (EMG5) UP (EMG2)

M = Date Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

#### **DEVICE MARKING AND RESISTOR VALUES**

Device	Package	Marking	R1 (K)	R2 (K)
EMG2DXV5T1	SOT-553	UP	47	47
EMG5DXV5T1	SOT-553	UF	10	47

#### **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS (Q1 & Q2)					
Collector-Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	_	_	100	nAdc
Collector-Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	-	_	500	nAdc
Emitter-Base Cutoff Current ( $V_{EB} = 6.0 \text{ V}$ , $I_{C} = 0$ )EMG2DXV5T1 EMG5DXV5T1	I <sub>EBO</sub>	- -	- -	0.1 0.2	mAdc
Collector-Base Breakdown Voltage ( $I_C = 10 \mu A, I_E = 0$ )	V <sub>(BR)CBO</sub>	50	_	-	Vdc
Collector-Emitter Breakdown Voltage (Note 3) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	-	-	Vdc
ON CHARACTERISTICS (Q1 & Q2) (Note 3)	•	•	•	•	•
DC Current Gain ( $V_{CE} = 10 \text{ V}, I_{C} = 5.0 \text{ mA}$ ) EMG2DXV5T1 EMG5DXV5T1	h <sub>FE</sub>	80 80	140 140	_ _	
Collector-Emitter Saturation Voltage (IC = 10 mA, $I_B = 0.3$ mA)	V <sub>CE(sat)</sub>	-	-	0.25	Vdc
$ \begin{array}{ll} \text{Output Voltage (on)} \\ (\text{V}_{CC} = 5.0 \text{ V}, \text{V}_{\text{B}} = 3.5 \text{ V}, \text{R}_{\text{L}} = 1.0 \text{ k}\Omega) \\ (\text{V}_{CC} = 5.0 \text{ V}, \text{V}_{\text{B}} = 2.5 \text{ V}, \text{R}_{\text{L}} = 1.0 \text{ k}\Omega) \\ \end{array} \\ \begin{array}{ll} \text{EMG2DXV5T1} \\ \text{EMG5DXV5T1} \end{array} $	V <sub>OL</sub>	_ _	_ _	0.2 0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 k $\Omega$ )	V <sub>OH</sub>	4.9	-	_	Vdc
Input Resistor EMG2DXV5T1 EMG5DXV5T1	R <sub>1</sub>	32.9 7.0	47 10	61.1 13	kΩ
Resistor Ratio EMG2DXV5T1 EMG5DXV5T1	R <sub>1</sub> /R <sub>2</sub>	0.8 0.17	1.0 0.21	1.2 0.25	

<sup>3.</sup> Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

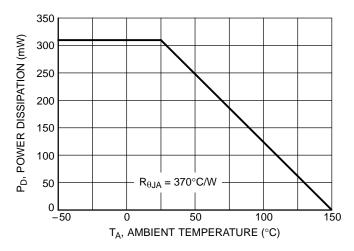


Figure 1. Derating Curve

#### TYPICAL ELECTRICAL CHARACTERISTICS — EMG2DXV5T1

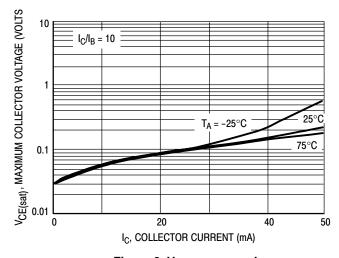


Figure 2.  $V_{CE(sat)}$  versus  $I_C$ 

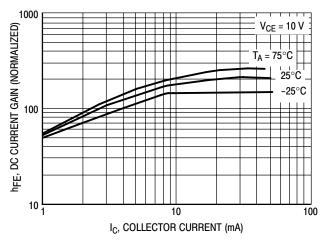


Figure 3. DC Current Gain

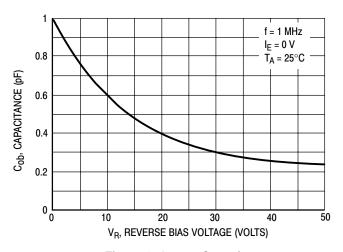


Figure 4. Output Capacitance

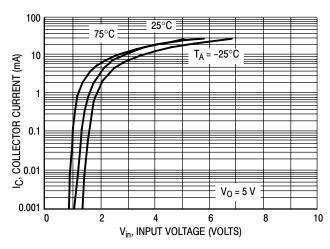


Figure 5. Output Current versus Input Voltage

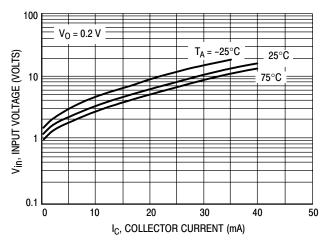


Figure 6. Input Voltage versus Output Current

#### TYPICAL ELECTRICAL CHARACTERISTICS - EMG5DXV5T1

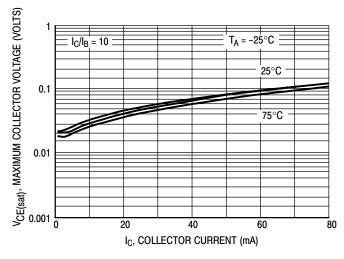


Figure 7.  $V_{CE(sat)}$  versus  $I_C$ 

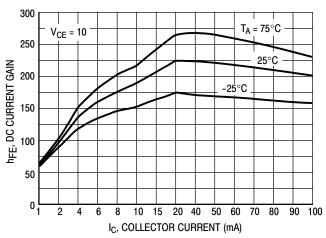


Figure 8. DC Current Gain

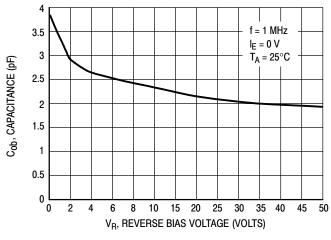


Figure 9. Output Capacitance

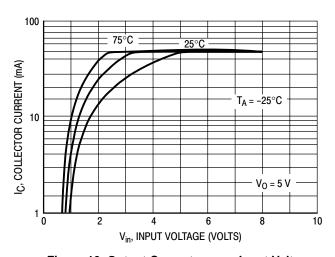


Figure 10. Output Current versus Input Voltage

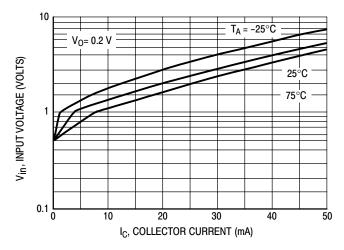


Figure 11. Input Voltage versus Output Current

#### **TYPICAL APPLICATIONS FOR NPN BRTs**

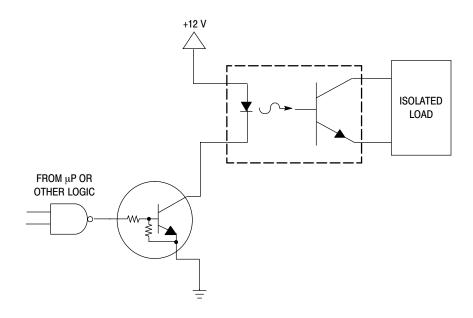


Figure 12. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

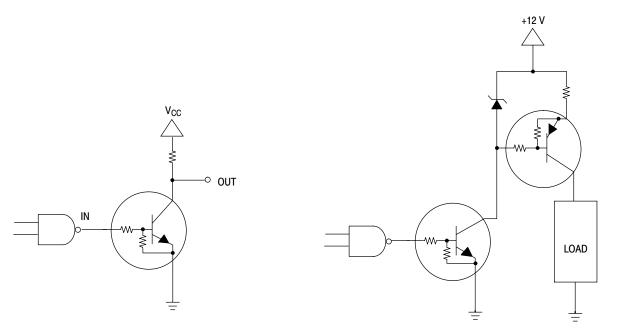


Figure 13. Open Collector Inverter: Inverts the Input Signal

Figure 14. Inexpensive, Unregulated Current Source

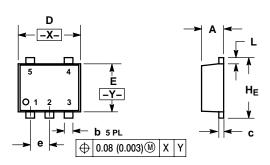
#### **DEVICE ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
EMG2DXV5T1	SOT-553	4000 / Tape & Reel
EMG2DXV5T1G	SOT-553 (Pb-Free)	4000 / Tape & Reel
EMG2DXV5T5	SOT-553	8000 / Tape & Reel
EMG2DXV5T5G	SOT-553 (Pb-Free)	8000 / Tape & Reel
EMG5DXV5T1	SOT-553	4000 / Tape & Reel
EMG5DXV5T1G	SOT-553 (Pb-Free)	4000 / Tape & Reel
EMG5DXV5T5	SOT-553	8000 / Tape & Reel
EMG5DXV5T5G	SOT-553 (Pb-Free)	8000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

SOT-553 XV5 SUFFIX 5-LEAD PACKAGE CASE 463B-01 ISSUE B

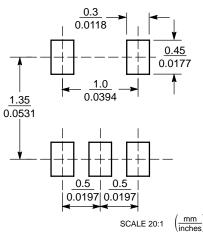


#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETERS
  3. MAXIMUM LEAD THICKNESS INCLUDES
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
С	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
е	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	1.50	1.60	1.70	0.059	0.063	0.067

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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