AmPAL*10H20EG8/AmPAL10020EG8

IMOX-III™ ECL Programmable Array Logic

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- High-performance t_{PD} = 6 ns, f_{MAX} = 125 MHz
- Eight user-programmable output logic macrocells for latched or combinatorial operation
- A registered version of the device is available as AmPAL10H20EV8 or AmPAL10020EV8 (see AMD Publication No. 06176A)
- Up to twenty inputs and eight outputs
- Individually user-programmable output polarity
- Variable product-term distribution for increased design flexibility
- Individual product term for output enable
- Asynchronous-RESET and PRESET capability
- Power-up RESET capability
- PRELOAD for improved testability
- Special designed-in test features for full AC and DC testing
- Platinum-silicide fuses ensure high programming yield, fast programming and unsurpassed reliability
- 10KH/100K ECL options
- 50-ohm drive with wired-OR capability
- 24-pin 300 mil DIPs and 28-pin chip carrier packages

GENERAL DESCRIPTION

The AmPAL10H20EG8/AmPAL10020EG8 is an advanced bipolar ECL Programmable Array Logic (PAL) device. It uses the familiar sum-of-products (AND-OR) single array logic structure, allowing users to program custom logic functions. Fabricated with AMD's new advanced bipolar IMOX-III SLOT-isolation process technology and combining the innovative architectural features of the AmPAL22V10, the AmPAL10H20EG8/AmPAL10020EG8 represents the most advanced ECL PAL device available on the market today.

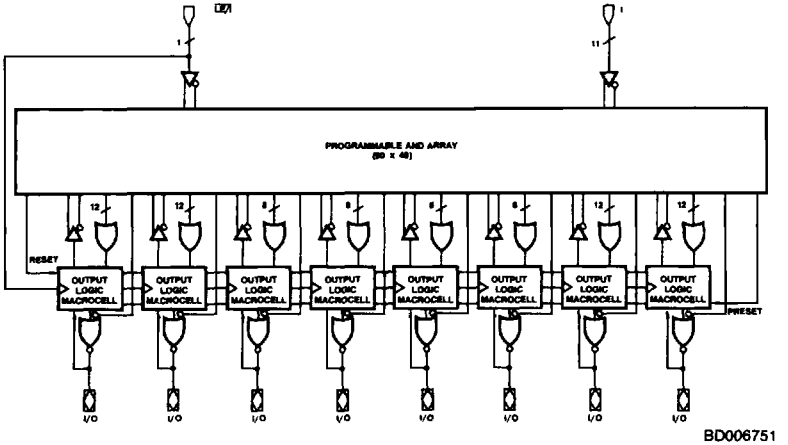
The AmPAL10H20EG8/AmPAL10020EG8 contains up to twenty inputs and eight outputs. It incorporates AMD's unique output logic macrocell (as in the AmPAL22V10), which allows the user to define and program the architecture of each output on an individual basis. Each output can be user-programmable for either latched or combinatorial operation. Each output also has user-programmable output-polarity control, further simplifying the design. The flexibility of the programmable output logic macrocells permits the system designer to tailor the device to paticular application requirements.

Increased logic power has been built into the AmPAL10H20EG8/AmPAL10020EG8 by providing a variable number of logical product terms per output. Four outputs have twelve logical product terms each, and the other four have eight logical product terms each. This variable allocation of logical product terms allows complex functions to be implemented in a single ECL PAL device. Each output also has a separate output-enable product term.

System operation has been enhanced by the addition of asynchronous-PRESET and RESET product terms for the AmPAL10H20EG8/AmPAL10020EG8. These product terms are common to all latched outputs.

The AmPAL10H20EG8/AmPAL10020EG8 incorporates power-up RESET on all latched outputs. It also has the unique capability to PRELOAD latches to any desired state during testing. PRELOAD permits full logical verification during testing.

BLOCK DIAGRAM



BD006751

*PAL is a registered trademark of and is used under license from Monolithic Memories, Inc.
IMOX is a trademark of Advanced Micro Devices, Inc.

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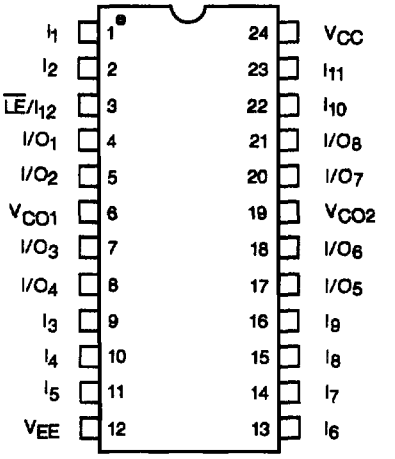
Issue Date: October 1986

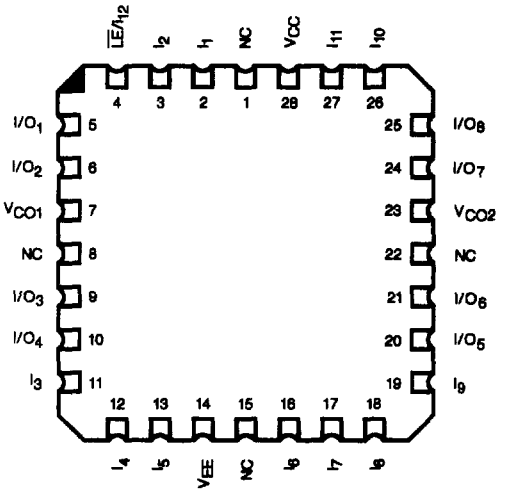
CONNECTION DIAGRAMS

DIPs



CD010170

LCC*



CD010180

*Also available in PLCC. Pinouts identical to LCC.

Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

$I_1 - I_{11}$ **Dedicated Input Pins (11)**

$I/O_1 - I/O_8$ **Bidirectional Input/Output Pins (8)**

$\overline{LE}/I_{12}$ **Latch Enable or Input Pin**

NC **No Connect**

V_{CC} **Circuit Ground**

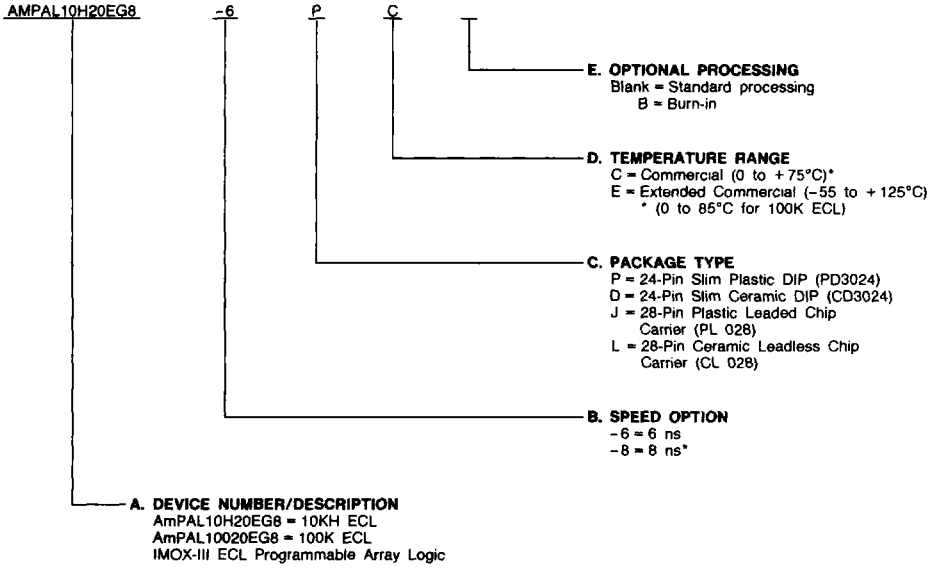
V_{CO1}, V_{CO2} **Circuit Ground Pins for Outputs (2)**

V_{EE} **Negative Supply Voltage**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



*Extended Commercial Range only.

Valid Combinations	
AMPAL10H20EG8-6	PC, DC, DCB, JC, LC, LCB
AMPAL10020EG8-6	
AMPAL10H20EG8-8	DE, LE
AMPAL10020EG8-8	

Valid Combinations

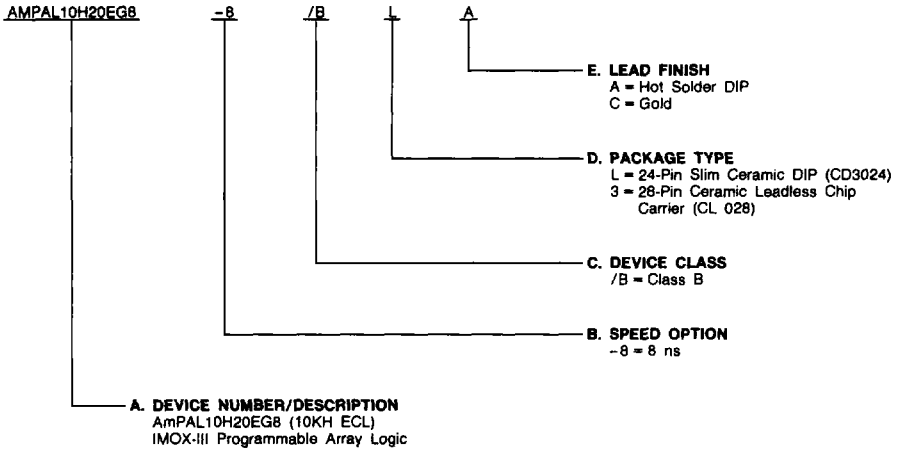
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AMPAL10H20EG8-8	/BLA, /B3C

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consists of Subgroups:
1, 2, 3, 7, 8, 9, 10 & 11.

FUNCTIONAL DESCRIPTION

The AmPAL10H20EG8/AmPAL10020EG8 is an advanced bipolar ECL I/O PAL device. It contains a programmable fuse array organized in the familiar sum-of-products (AND-OR) structure.

The block diagram in Figure 1 illustrates the basic architecture of the AmPAL10H20EG8/AmPAL10020EG8. There are up to twenty external inputs and eight outputs. The inputs are connected to a programmable-AND array. Initially, the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming (blowing) of the fuses, the AND gates may be "connected" to only the true inputs, the complement inputs, or to neither type of input. When both the true and complement fuses are left intact, a logical-FALSE results at the output of the AND gate. An AND gate with all the fuses blown will assume the logical-TRUE state. The outputs of the AND gates are connected to fixed-OR gates.

There are an average of ten product terms per OR gate (output), distributed in a variable fashion. Four outputs have eight product terms each while the other four have twelve product terms each. This variable distribution of product terms allows more complex logical functions to be implemented.

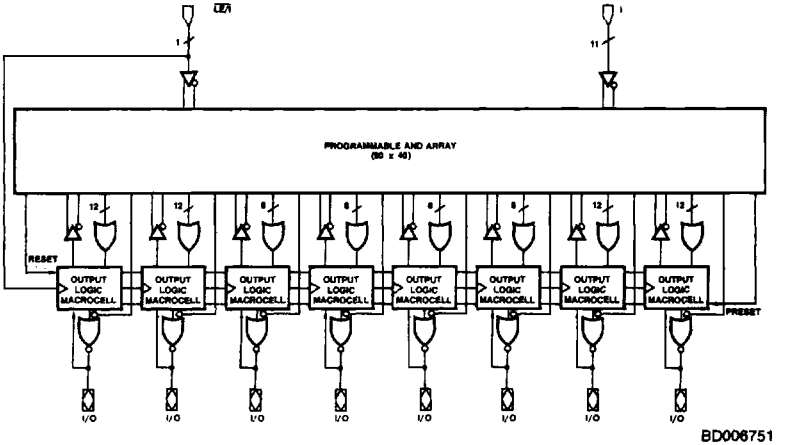


Figure 1. Block Diagram

Output Logic Macrocells

A useful feature of the AmPAL10H20EG8/AmPAL10020EG8 is its versatile programmable output-logic-macrocell structure. It allows the user to program the outputs on an individual basis in a very flexible manner.

The AmPAL10H20EG8/AmPAL10020EG8 output logic macrocell incorporates a transparent latch. As shown in the output logic macrocell diagram, each macrocell contains two programmable fuses — S_0 and S_1, for programming the output functions. S_1 controls whether the output will be latched or combinatorial. S_0 controls the output polarity (active-HIGH or active-LOW). Depending on the states of these two fuses, an individual output operates in one of four modes: Latched/Active-LOW, Latched/Active-HIGH, Combinatorial/Active-LOW, and Combinatorial/Active-HIGH. Each output is also provided with a separate output enable product term.

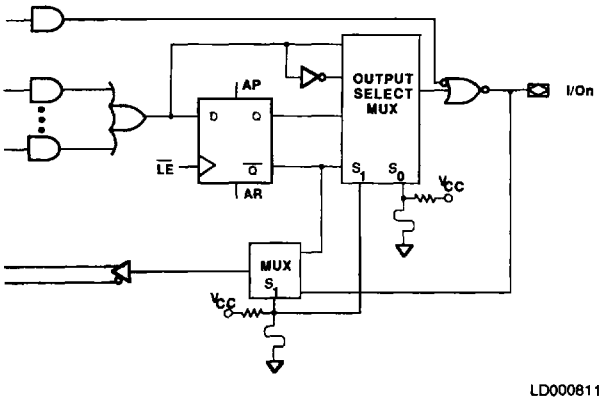


Figure 2. AmPAL10H20EG8/AmPAL10020EG8 Output Logic Macrocell

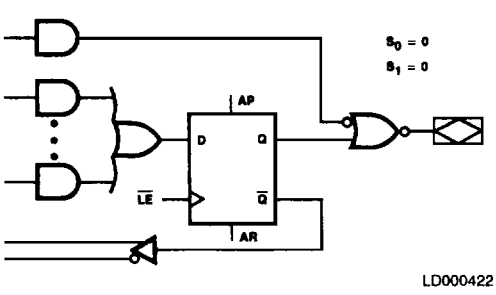


Figure 3-1. Latched/Active-LOW

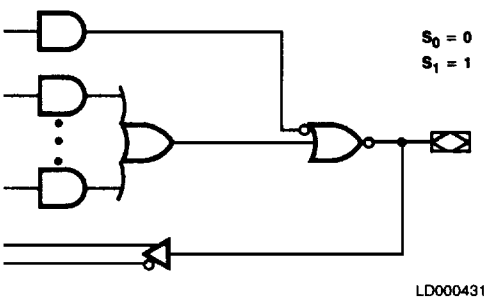


Figure 3-3. Combinatorial/Active-LOW

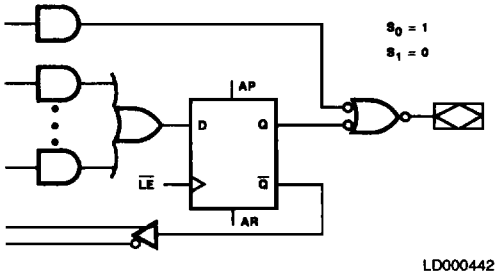


Figure 3-2. Latched/Active-HIGH

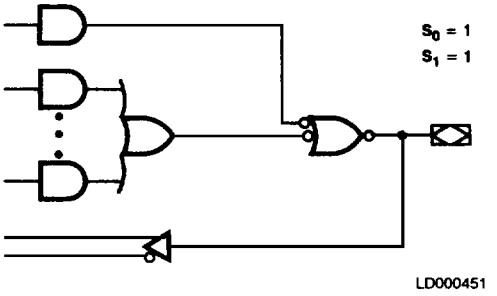


Figure 3-4. Combinatorial/Active-HIGH

S_1	S_0	Output Configuration
0	0	Latched/Active-LOW
0	1	Latched/Active-HIGH
1	0	Combinatorial/Active-LOW
1	1	Combinatorial/Active-HIGH

0 = Unblown Fuse
1 = Blown Fuse

Feedback

Another feature of the AmPAL10H20EG8/AmPAL10020EG8 output macrocell structure is the flexibility of its feedback selection. The feedback can be from either the I/O line or the latched output. The feedback multiplexer is also controlled by the S_1 fuse. The feedback path changes with the output-mode selection. If the output is selected to be latched, the feedback is latched. If the output is combinatorial, the feedback is from the I/O line. This feature enables the designer to optimally use the device to meet precise application requirements. Additionally, it also allows him/her to perform control tasks, such as arbitration functions, easily.

Output Enable

Each of the eight output logic macrocells of the AmPAL10H20EG8/AmPAL10020EG8 contains a dedicated product term for output-enable function. When this product term is asserted LOW, the output is forced into a LOW state where it remains until the output-enable product term goes HIGH.

PRESET and RESET

To improve in-system functionality, the AmPAL10H20EG8/AmPAL10020EG8 has additional PRESET and RESET product terms. Common asynchronous-RESET and PRESET are provided for all the latches of the AmPAL10H20EG8/AmPAL10020EG8. When the asynchronous PRESET product term is asserted HIGH the output latches are loaded with a HIGH and when the RESET product term is asserted HIGH the output latches are loaded with a LOW. For the RESET/PRESET to work the latches should be in latched and not transparent mode. These functions are particularly useful for system power-on and reset.

PRELOAD

To simplify testing, the AmPAL10H20EG8/AmPAL10020EG8 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. PRELOAD allows any arbitrary values to be loaded into the PAL device's output latches.

A typical functional-test sequence would be to verify all possible outputs for the device being tested. To verify these transitions requires the ability to set the latches to an arbitrary "present state" value and to set the device inputs to any arbitrary "present input" value. Once this is done, the latch enable is driven transparent to allow logic to determine the

"new state" of the outputs. These outputs can then be checked to validate the design.

Without PRELOAD capability, it is difficult and in some cases impossible to load an arbitrary value into the latches. This can lead to logic-verification sequences which are either incomplete or excessively long. With PRELOAD capability, logic verification sequences can be greatly shortened, hence reducing the test time and the development costs, and guaranteeing proper in-system operation.

Fabrication

The AmPAL10H20EG8/AmPAL10020EG8 is manufactured using Advanced Micro Devices' new IMOX-III SLOT-isolation process. This advanced process offers increased density and reduced internal capacitance resulting in the fastest possible programmable logic devices.

The AmPAL10H20EG8/AmPAL10020EG8 is fabricated with AMD's fast programming and highly reliable platinum-silicide fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Platinum-silicide was selected as the fuse-link material to achieve a well controlled melt rate resulting in large non-conductive gaps which ensure very stable, long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible-link programmable logic.

Testing

The AmPAL10H20EG8/AmPAL10020EG8 contains many internal test features, including circuitry and extra fuses which allow AMD to test each part before shipping. This ensures extremely high post-programming functional yields. The test fuses are programmed to assure the ability of each part to perform correct programming. There are extra test words which are preprogrammed during manufacturing and tested to ensure correct logical operation and provide extra test paths to achieve excellent parametric correlation.

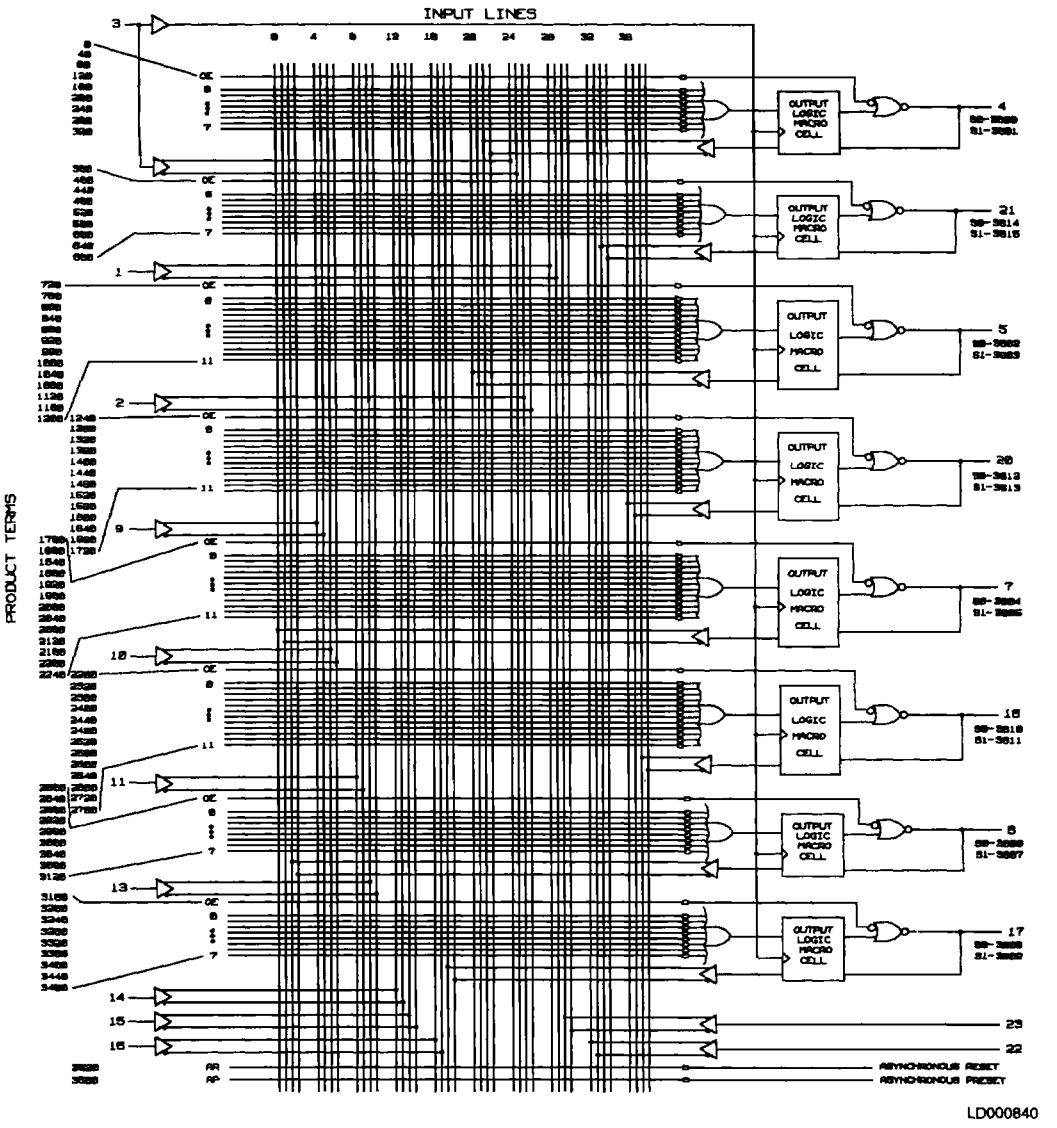


Figure 4. Logic Diagram — JEDEC Fuse Numbering for AmPAL10H20EG8/10020EG8

Note: Pin out for DIP only.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage (V_{EE})
with Respect to Ground ..... −8 V to 0 V
DC Input Voltage
with Respect to Ground ..... V_{EE} to 0 V
Output Current
-Continuous ..... 35 mA
-Surge ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices — 100K Devices
Temperature (T_A) Operating Free Air ..... 0 to +85°C
Supply Voltage (V_{EE}) ..... −5.7 to −4.2 V

Commercial (C) Devices — 10KH Devices
Temperature (T_A) Operating Free Air ..... 0 to +75°C
Supply Voltage (V_{EE}) ..... −5.46 to −4.94 V

Extended Commercial (E) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) Operating Case ..... +125°C Max.
Supply Voltage (V_{EE}) ..... −5.72 to −4.68 V

Military* (M) Devices
Temperature (T_A) ..... −55°C Min.
Temperature (T_C) ..... +125°C Max.
Supply Voltage (V_{EE}) ..... −5.72 to −4.68 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified

AmPAL10H20EG8 (Commercial)

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	T_A = 0°C	−1020	−840	mV
				T_A = +25°C	−980	−	
				T_A = +75°C		−	
V_{OL}	Output LOW Voltage			T_A = 0°	−	80	mV
				= +25		0	
				+75	−19	−1	
V_{IH}	Input HIGH Voltage	Guaranteed Input (Note 3)			−1170	−840	mV
					−1130	−810	
				T_A = +75°C	−1070	−735	
V_{IL}	Input LOW Voltage	Gu (No		T_A = 0°C	−1950	−1480	mV
				T_A = +25°C	−1950	−1480	
				T_A = +75°C	−1980	−1450	
I_{IH}	Input HIGH Current	= V_{IH} (Max.)		T_A = 0°C		220	µA
				T_A = +25°C		220	
				T_A = +75°C		220	
	Input LOW Current	V_{IN} = V_{IL} (Min.)		T_A = 0°C	0.5		µA
				T_A = +25°C	0.5		
				T_A = +75°C	0.3		
I_{EE}	Power Supply Current	All Inputs and Outputs Open		T_A = 0°C	−230		mA
				T_A = +25°C	−230		
				T_A = +75°C	−230		

Table continues on following page.
Notes: See notes following Military DC characteristics table.

AmPAL10H20EG8 (Military); included in Group A, Subgroup 1, 2, 3 tests unless otherwise noted.

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	$T_A = 0°C$	TBD	TBD	V
				$T_A = +25°C$	TBD	TBD	
				$T_A = +75°C$	TBD	TBD	
V_{OL}	Output LOW Voltage			$T_A = 0°C$	TBD		
				$T_A = +25°C$	TBD	TBD	V
				$T_A = +75°C$		TBD	
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage (Note 3)		$T_A = 0°C$			mV
				T_A = [illegible]°C		TBD	
				T_A = [illegible]	TBD	TBD	
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage (Note 3)		T_A = [illegible]°C	TBD	TBD	mV
				T_A = [illegible]		TBD	
				T_A = [illegible]°C	TBD	TBD	
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		T_A = [illegible]	TBD	TBD	μA
				T_A = [illegible]25°C	TBD	TBD	
				$T_A = +75°C$	TBD	TBD	
I_{IL}	Input LOW Current	V_{IN} = [illegible]		$T_A = 0°C$	TBD	TBD	μA
				$T_A = +25°C$	TBD	TBD	
				$T_A = +75°C$	TBD	TBD	
I_{EE}	Power Supply Current	All Inputs [illegible] Outputs Open		$T_A = 0°C$	TBD	TBD	mA
				$T_A = +25°C$	TBD	TBD	
				$T_A = +75°C$	TBD	TBD	

AmPAL10020EG8 (Commercial)

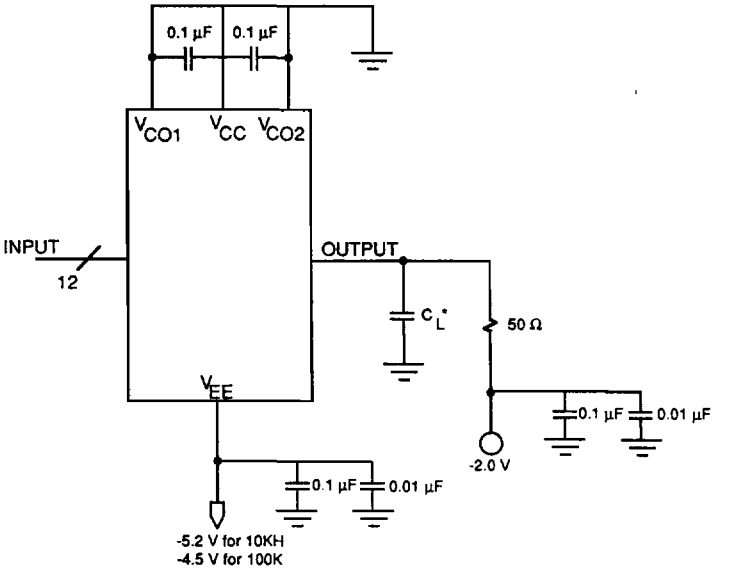
Parameter Symbols	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Max.) or V_{IL} (Min.)	Loading is 50 Ω to −2.0 V	−1025	−880	mV
V_{OL}	Output Voltage LOW			−1810	−1620	mV
V_{OH}	Output Voltage HIGH	$V_{IN} = V_{IH}$ (Min.) or V_{IL} (Max.)		−1035		mV
V_{OL}	Output Voltage LOW				−1610	mV
V_{IH}	Input Voltage HIGH	Guaranteed Input Voltage HIGH (Note 3)		−1165	−880	mV
V_{IL}	Input Voltage LOW	Guaranteed Input Voltage LOW (Note 3)		−1810	−1475	mV
I_{IH}	Input Current HIGH	$V_{IN} = V_{IH}$ (Max.)			220	μA
I_{IL}	Input Current LOW	$V_{IN} = V_{IL}$ (Min.)		0.5		μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open		−230		mA

Notes: 1. Guaranteed with transverse air flow exceeding 400 linear F.P.M.
2. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are:
"Max." the value closest to positive infinity.
"Min." the value closest to negative infinity.
3. These are absolute voltages with respect to the device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment and fixturing.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified; included in Group A, Subgroup 9, 10, 11 tests unless otherwise noted

No.	Parameter Symbol	Parameter Description	Test Conditions	C Devices				E/M Devices				Units
				-6		TBD		-8		TBD		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{PD}	Input or Feedback to Output			6				8			ns
2	t_{EA}	Input to Output Enable			6				8			ns
3	t_{ER}	Input to Output Disable			6				8			ns
4	t_{LEO}	$\overline{LE}$ to Output			5				4.5			ns
5	t_S	Input or Feedback Setup Time		5				5.5				ns
6	t_H	Hold Time		0				0				ns
7	t_W	$\overline{LE}$ Width		3				5				ns
8	t_{AW}	Asynchronous RESET/PRESET Width		6				8				ns
9	t_{SR}	Asynchronous RESET/PRESET Recovery Time		6				8				ns
10	t_{AP}	Asynchronous RESET/PRESET to Latched Output RESET/PRESET			6				8			ns

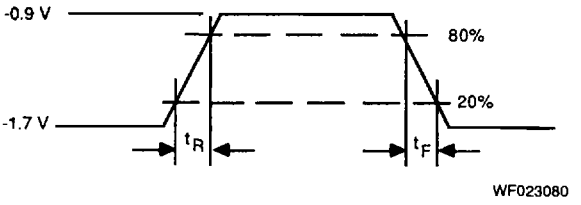
SWITCHING TEST CIRCUIT



*C_L = 5 pf for 10KH
C_L = 3 pf for 100KH

SWITCHING TEST WAVEFORM

INPUT PULSE



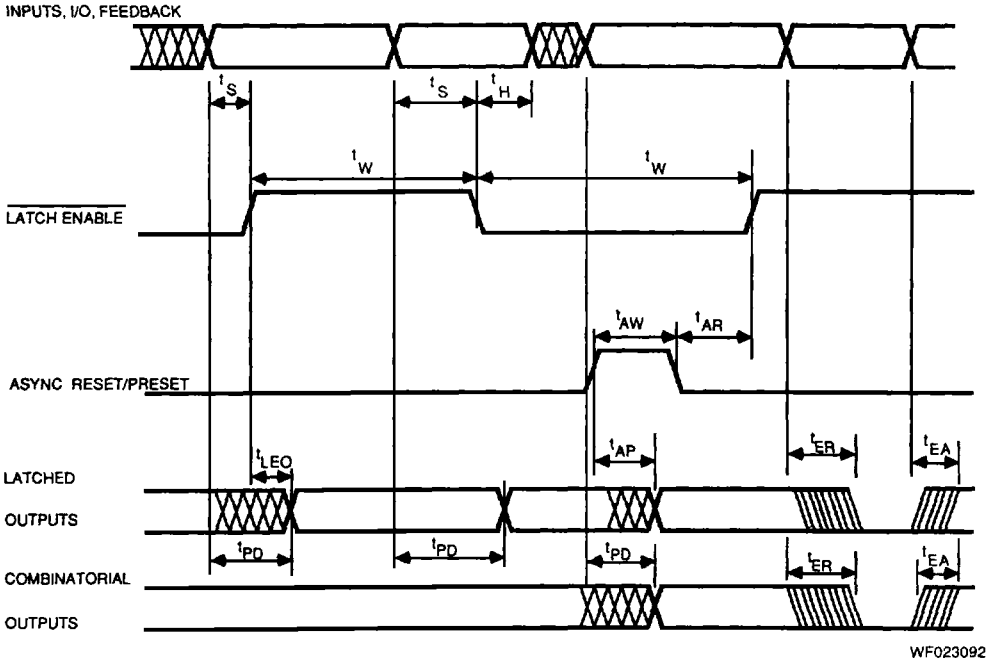
$t_R = t_F$ = 2.2 ns Max. for 10KH
$t_R = t_F$ = 1.0 ns Max. for 100K

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010

SWITCHING WAVEFORMS



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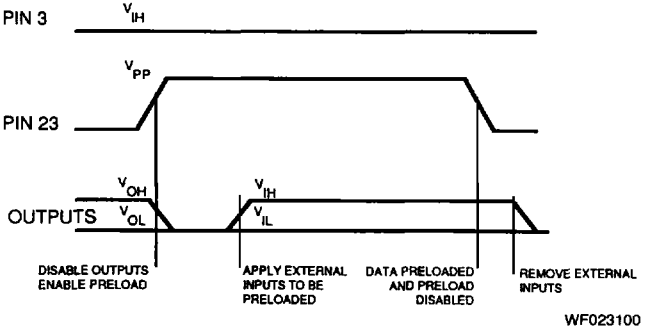
PRELOAD OF LATCHED OUTPUTS

The AmPAL10H20EG8/AmPAL10020EG8 latched outputs are provided with circuitry to allow loading each latch to either a HIGH or LOW state. This simplifies testing as any state can be loaded into the latches to control outputs. The pin levels and the timing necessary to perform the PRELOAD function are detailed below.

PRELOAD is accessed by applying V_{PP} on pin 23. The data to be preloaded is set on the output pins. Bringing pin 23 back to a logic-LOW level latches the data into the output latches.

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Level During PRELOAD and Verify	−1.1	−0.9	−0.7	V
V_{IL}	Input LOW Level During PRELOAD and Verify	−1.85	−1.65	−1.45	V
V_{PP}	PRELOAD Enable Voltage Applied to Pin 23	1.8	2.0	2.2	V

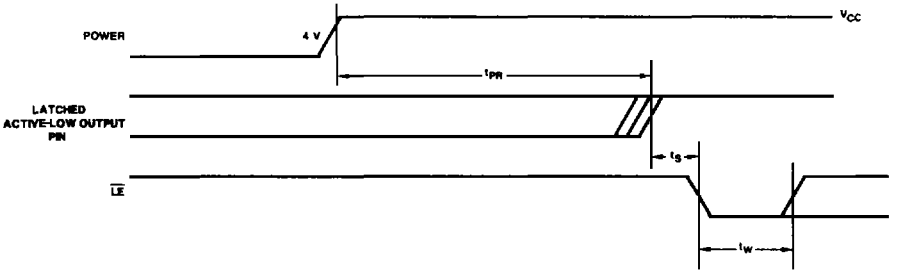


PRELOAD Timing Waveform

POWER-UP RESET

The latches in the AmPAL10H20EG8/AmPAL10020EG8 have been designed with the capability to RESET during system power-up. Following power-up, all latches will be LOW. The output state will depend upon the state of the output buffer and the polarity fuse. This feature provides extra flexibility to the designer. A timing diagram and a parameter table are shown below. Due to the asynchronous operation of the power-up RESET and the wide range of ways V_{CC} can rise to steady state, two conditions are required to insure a valid power-up RESET. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following RESET, the $\overline{\text{Latch Enable}}$ must not be driven transparent until all applicable input and feedback setup times are met.



Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
t_{PR}	Power-Up RESET Time		600	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics			
t_W	$\overline{\text{LE}}$ Width				

PROGRAMMING AND VERIFICATION

The AmPAL10H20EG8/AmPAL10020EG8 is programmed and verified using AMD's ECL programmable-logic-programming algorithm. The fuse to be programmed is selected by its input line number (array row), its product-term number (array column), and by the output associated with it (one at a time). The levels for addressing the rows and columns are all in ECL (10KH) levels. The fuse is then programmed and verified by applying a simple sequence of voltages as shown in the programming waveform diagram. The values of the programming voltages are shown in the table of programming parameters.

Input line numbers (0 to 39) are addressed using a full decode scheme via ECL levels on pins 9 – 11 and 13 – 15 where pin 15 is the LSB and pin 9 is the MSB. Input line addressing is shown in Table 1. Note that one input line is given to select all the architectural fuses.

Product terms are addressed using a full decode scheme via ECL levels on pins 1, 2, 22 and 23 where pin 23 is the LSB and pin 1 is the MSB. Product terms (column number) addressing is shown in Table 2.

The sequence of signals and events associated with them during programming and verification modes is shown in the Programming Waveforms. The row and column addresses are set up on the corresponding input pins. Then V_{CO1} (pin 6) is brought to a programming voltage of V_{COP}. The normal I/O pins are now disabled and the address decode is enabled. The device is now in a verification mode. V_{CO2} (pin 19) is now brought to the V_{COP} programming voltage. The programming mode is enabled. A high voltage of V_{OP} (Fuse-Enable Voltage) on the output pin corresponding to the fuse to be blown activates the programming voltage, and the fusing is started.

After a certain programming time, the fuse is blown and the programming voltage is removed from V_{CO2}. The device is back in the verification mode. Latch Enable is HIGH during programming. It is then brought LOW to enable the latches and verify for V_{Blown} level (V_{IHP} or V_{ILP}). After verification is done, the programming voltage is removed from V_{CO1} and the part is back in normal mode.

Security Programming

A security fuse is provided on each AmPAL10H20EG8/AmPAL10020EG8 to protect any user proprietary logic design. It is addressed and programmed like any other fuse in the array. Once blown, the circuitry enabling any fuse verification and latch PRELOAD is permanently disabled. The security fuse is verified by verifying the whole fuse array as if every fuse was blown.

Programming Yield

AMD PAL devices have been designed to ensure extremely high programming yields. To help ensure that a part was correctly programmed, once the programming is completed the entire fuse array should be re-verified at both LOW and HIGH V_{CC}. Re-verification can be accomplished by reading all eight outputs in parallel rather than one at a time. This verification cycle checks that the array fuses have been blown and can be sensed by the outputs under varying conditions.

AMD PAL devices contain many internal features, including circuitry and extra fuses to test the ability of each part to perform programming before shipping, and to assure a correct logical operation for a correctly programmed part. Programming-yield losses are most likely due to poor programming socket contact, programming equipment out of calibration, or improper usage of said equipment.

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PROGRAMMING PARAMETERS (T_A = 25°C)

Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Units
V_{IHP}	Input HIGH Level During Programming & Verify	−1.1	−0.9	−0.7	V
V_{ILP}	Input LOW Level During Programming & Verify	−1.85	−1.65	−1.45	V
V_{OP}	Fuse Enable Voltage Applied to Output Being Programmed @ 1 – 25 mA (Additional 80 mA if Output Terminated to 50-ohm Load)	1.8	2.0	2.2	V
V_{COP}	Programming Voltage Applied to V_{CO1}, V_{CO2} @ 15 – 200 mA	14.0	15.0	16.0	V
V_{CO1} & V_{CO2}	Power Supply for the Output Stage Sourcing	−0.1	0	0.1	V
V_{CCP}	V_{CC} During Programming & Verify I_{CC} = 50 – 250 mA Sourcing I_{CC} = 50 – 150 mA Sinking	−0.3	0	0.3	V
V_{EEP}	V_{EE} During Programming & Verify	−5.4	−5.2	−5.0	V
V_{ONP}	Termination Voltage for Output-Load Resistor	−2.1	−2.0	−1.9	V
R	Output-Load Resistor	47.5	50.0	52.5	Ω
t_P	Fusing Time First Attempt	40	50	100	μs
	Fusing Time Second Attempt	4	5	10	ms
t_D	Delays Between Various Level Changes	100	200	1000	ns
t_V	PRELOAD During Which Output is Sensed for V_{BLOWN} (V_{IHP} or V_{ILP}) Level			500	ns

TABLE 1. INPUT ADDRESSING

Input Line Number	Address Pin States					
	9	10	11	13	14	15
0	L	L	L	L	L	L
1	L	L	L	L	L	H
2	L	L	L	L	H	L
3	L	L	L	L	H	H
4	L	L	L	H	L	L
5	L	L	L	H	L	H
6	L	L	L	H	H	L
7	L	L	L	H	H	H
8	L	L	H	L	L	L
9	L	L	H	L	L	H
10	L	L	H	L	H	L
11	L	L	H	L	H	H
12	L	L	H	H	L	L
13	L	L	H	H	L	H
14	L	L	H	H	H	L
15	L	L	H	H	H	H
16	L	H	L	L	L	L
17	L	H	L	L	L	H
18	L	H	L	L	H	L
19	L	H	L	L	H	H
20	H	L	L	L	L	L
21	H	L	L	L	L	H
22	H	L	L	L	H	L
23	H	L	L	L	H	H
24	H	L	L	H	L	L
25	H	L	L	H	L	H
26	H	L	L	H	H	L
27	H	L	L	H	H	H
28	H	L	H	L	L	L
29	H	L	H	L	L	H
30	H	L	H	L	H	L
31	H	L	H	L	H	H
32	H	L	H	H	L	L
33	H	L	H	H	L	H
34	H	L	H	H	H	L
35	H	L	H	H	H	H
36	H	H	L	L	L	L
37	H	H	L	L	L	H
38	H	H	L	L	H	L
39	H	H	L	L	H	H
	RESERVED					
63*	H	H	H	H	H	H

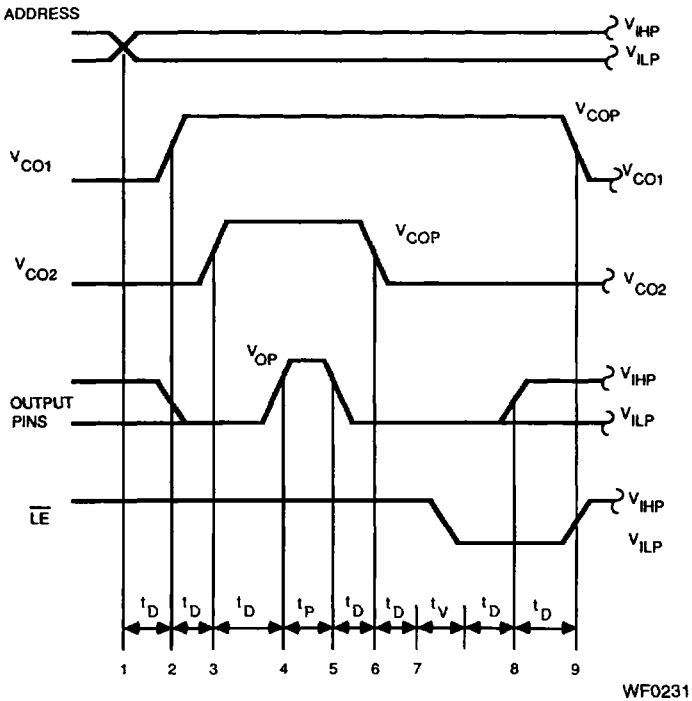
*Architecture Row

TABLE 2. COLUMN NUMBER ADDRESSING

Address	Output Pins							
1 2 22 23	4 OUT1	5 OUT2	7 OUT3	8 OUT4	17 OUT5	18 OUT6	20 OUT7	21 OUT8
L L L L	0	0	0	0	0	0	0	0
L L L H	1	1	1	1	1	1	1	1
L L H L	2	2	2	2	2	2	2	2
L L H H	3	3	3	3	3	3	3	3
L H L L	4	4	4	4	4	4	4	4
L H L H	5	5	5	5	5	5	5	5
L H H L	6	6	6	6	6	6	6	6
L H H H	7	7	7	7	7	7	7	7
H L L L	–	8	8	–	–	8	8	–
H L L H	–	9	9	–	–	9	9	–
H L H L	–	10	10	–	–	10	10	–
H L H H	–	11	11	–	–	11	11	–
H H L L	OE	OE	OE	OE	OE	OE	OE	OE
H H L H	OP	OP	OP	OP	OP	OP	OP	OP
H H H L	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C
H H H H	SF	AR	–	–	–	–	AP	–

AR = Async. RESET
AP = Async. PRESET
OE = Output Enable
R/C = Reg/Comb Fuse
OP = Output Polarity Fuse
SF = Security Fuse

PROGRAMMING WAVEFORMS



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1. Row and Column addresses applied.
2. Normal I/O pins disabled.
3. Programming Voltage applied address decode enable.
4. Output associated with fuse to be blown selected. Fusing time started.
5. Fusing time ended.
6. Programming Voltage removed. Device in Verification Mode.
7. $\overline{LE}$ Pulse.
8. Verify for V_{BLOWN} level.
9. End of Programming and Verification Cycle.

AmPAL10H20EG8/AmPAL10020EG8 PROGRAMMING SUPPORT INFORMATION

Hardware Vendor	Programmer Model(s)	Personality Module	Socket Adaptor
Data I/O 10525 Willow Road N.E. Redmond, WA 98052 (206) 881-6444	System 29	Under Development	Not Required
	UNISITE 40	Not Required	Not Required
Stag Microsystems 528-5 Weddell Drive Sunnyvale, CA 94089 (408) 745-1991 or (800) 227-8836	Model PPZ	Under Development	Not Required
	Model ZL30A	Under Development	Not Required

The machines noted above have been qualified by AMD to ensure high programming yields. Check with the factory to determine current status of equipment noted as "Under Development," or for other available models.

Design-Aid Software for AmPAL10H20EG8/AmPAL10020EG8

Software Vendor	Software Package	Comments
P-CAD Systems, Inc. 1290 Parkmoor Ave. San Jose, CA 95126 (408) 971-1300	CUPL	
Advanced Micro Devices, Inc. 901 Thompson Pl. Sunnyvale, CA 94088 (408) 732-2400	AmCUPL	Supported by P-CAD Systems, Inc.
Data I/O 10525 Willow Road N.E. Redmond, WA 98052 (206) 881-6444	ABEL	