Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP 5330
Monolithic Sample–and–Hold Amplifier

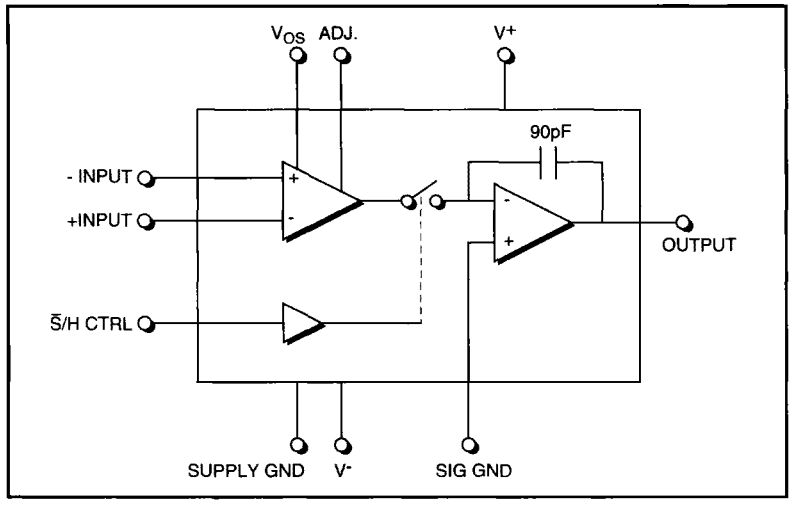
FEATURES
- Very Fast Acquisition Time
- 0.1μV/μs Droop Rate
- Very Low Offset 0.2mV
- 90V/μs Slew Rate
- Wide Supply Range ±12V to ±18V
- –100dB Hold–Mode–Feedthrough
- ±.0015% Pedestal Non–linearity
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

APPLICATIONS
- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto–Zero Circuits
- Peak Detectors

DESCRIPTION
The **SP5330** is a very fast sample–and–hold amplifier designed primarily for use in precision high speed signal processing and signal conversion applications. It is manufactured with **Sipex**'s high performance complementary bipolar dielectric isolation process. Notable performance features of the **SP5330** include a typical 12–bit accurate acquisition time of 500ns, 0.1μV/μS droop rate and 0.001% FS linearity.

Architecturally, the **SP5330** consists of an input transconductance amplifier capable of delivering high output charging current, a low leakage analog switch, and an integrating output stage that includes a 90pF hold capacitor. Since the analog switch operates into a virtual ground, charge injection on the hold capacitor is constant and independent of V_{IN}. Compensation circuits are used to minimize charge injection and thereby limit hold step (pedestal) error to 0.5 mV. Additionally, this error can be adjusted to zero via the offset adjust pins. Compensation circuits are also used to reduce the hold mode droop rate.

The **SP5330** will operate at reduced supply voltages with reduced signal swing. The **SP5330** is available as die or packaged as either a 14-pin Cerdip or 20–pin ceramic LCC. MIL–STD–883 screened devices are available. Contact the factory for specification information.



ABSOLUTE MAXIMUM RATINGS[1]

Voltage between V+ and PWR/SIG GND ..... *+20V*
Voltage between V– and PWR/SIG GND ..... *–20V*
Voltage between PWR GND and SIG GND ..... *±2.0V*
Differential Input Voltage ..... *±24V*
Voltage between $\overline{S}$/H Control and PWR/SIG GND ..... *+8V, –6V*
Output Current, continuous[2] ..... *±17mA*
Total Power Dissipation ..... *+1.33W*
Derate 12.2 mW/°C above 75°C
Storage Temperature ..... *–65°C to 150°C*

SPECIFICATIONS

Test conditions (unlesss otherwise specified) V_{SUPPLY} = ±15V ±3%; Digital Input (Pin 8): V_{IL} < +0.8V (Sample), V_{IN} < +2.0V (Hold); SIG GND = PWR GND.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
INPUT CHARACTERISTICS					
Input Voltage Range	±10			V	$T_{MIN} \le T_A \le T_{MAX}$
Input Resistance[5]	5	15		MΩ	T_A = 25°C
Input Capacitance		3		pF	T_A = 25°C
Offset Voltage		0.2		mV	T_A = 25°C
			2.0	mV	$T_{MIN} \le T_A \le T_{MAX}$
Offset Voltage T.C.		1	10	µV/°C	$T_{MIN} \le T_A \le T_{MAX}$
Bias Current		±20		nA	T_A = 25°C
–2,–4			±500	nA	$T_{MIN} \le T_A \le T_{MAX}$
–5			±300	nA	$T_{MIN} \le T_A \le T_{MAX}$
Offset Current		±20			T_A = 25°C
–2,–4			±500	nA	$T_{MIN} \le T_A \le T_{MAX}$
–5			±300	nA	$T_{MIN} \le T_A \le T_{MAX}$
Common Mode Range	±10			V	$T_{MIN} \le T_A \le T_{MAX}$
CMRR	86	104		dB	V_{CM} = ±10Vdc; $T_{MIN} \le T_A \le T_{MAX}$
TRANSFER CHARACTERISTICS					
Gain, DC	$2x10^6$	$2x10^7$		V/V	$T_{MIN} \le T_A \le T_{MAX}$
Gain Bandwidth Product		4.5		MHz	V_O = 200 mV_{P-P}; R_L = 2KΩ; C_L = 50pF; T_A = 25°C
Linearity		0.001		%FSR	V_O = 20V_{P-P}; T_A = 25°C
OUTPUT CHARACTERISTICS					
Output Voltage Swing	±10	±11		V	$T_{MIN} \le T_A \le T_{MAX}$
Output Current	±10	±20		mA	$T_{MIN} \le T_A \le T_{MAX}$
Full Power Bandwidth		1.6		MHz	FPBW = Slew Rate/2πV peak T_A = 25°C
Output Resistance					
Hold Mode		0.2		Ω	T_A = 25°C
Sample Mode[6]		10^5	0.001	Ω	T_A = 25°C
Total Output Noise, DC to 4.0 MHz					
Hold Mode		190		µV RMS	T_A = 25°C
Sample Mode		200		µV RMS	T_A = 25°C
TRANSIENT RESPONSE					
Rise Time		55		ns	V_O = 200 mV_{P-P}; R_L = 2KΩ; C_L = 50pF; T_A = 25°C
Overshoot		13		%	V_O = 200 mV_{P-P}; R_L = 2KΩ; C_L = 50pF; T_A = 25°C
Slew Rate		100		V/µs	V_O = 20V Step; R_L = 2KΩ; C_L = 50pF; T_A = 25°C

SPECIFICATIONS

Test conditions (unlesss otherwise specified) V_{SUPPLY} = ±15V ±3%; Digital Input (Pin 8); V_{IL} < +0.8V (Sample), V_{IN} < +2.0V (Hold); SIG GND = PWR GND.

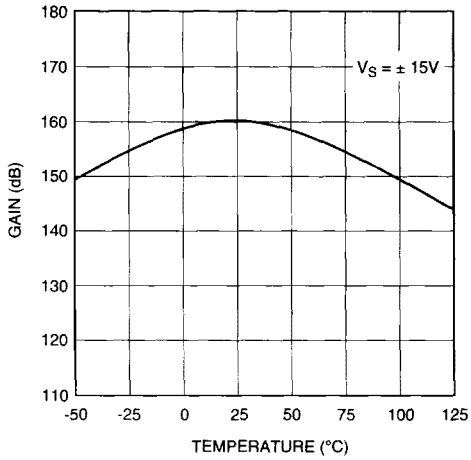
PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL INPUT CHARACTERISTICS					
Input Voltage (High), V_{IH}	2.0			V	$T_{MIN} \le T_A \le T_{MAX}$
Input Voltage (Low), V_{IL}			0.8	V	$T_{MIN} \le T_A \le T_{MAX}$
Input Current (V_{IL} = 0V)		10	40	µA	$T_{MIN} \le T_A \le T_{MAX}$
Input Current (V_{IH} = +5V)		10	40	µA	$T_{MIN} \le T_A \le T_{MAX}$
SAMPLE/HOLD CHARACTERISTICS					
Acquisition Time[7]:					
0.1%		350		ns	T_A = 25°C
			500	ns	$T_{MIN} \le T_A \le T_{MAX}$
0.01%		500		ns	T_A = 25°C
			900	ns	$T_{MIN} \le T_A \le T_{MAX}$
Aperture Time[5]		40		ns	T_A = 25°C
Effective Aperture Delay Time[7]	–80	–40	0	ns	T_A = 25°C
Aperture Uncertainty		0.1		ns	T_A = 25°C
Droop Rate[3]		0.1		µV/µs	T_A = 25°C
–2,–4			100	µV/µs	$T_{MIN} \le T_A \le T_{MAX}$
–5			10	µV/µs	$T_{MIN} \le T_A \le T_{MAX}$
Hold Step Error		0.5		mV	V_{IN} = 0V; V_{IH} = ±3.5V; T_R = 20ns (V_{IL} to V_{IH})
Hold Mode Setting Time[7]		–100	200	ns	T_A = 25°C; 0.01%
Hold Mode Feedthrough		–120		dB	$T_{MIN} \le T_A \le T_{MAX}$; $20V_{PP}$, 100kHz
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current					
–2,–4		13	20	mA	$T_{MIN} \le T_A \le T_{MAX}$
–5		13	22	mA	$T_{MIN} \le T_A \le T_{MAX}$
Negative Supply Current					
–2,–4		13	21	mA	$T_{MIN} \le T_A \le T_{MAX}$
–5		13	23	mA	$T_{MIN} \le T_A \le T_{MAX}$
Power Supply Rejection V+, V–[4]	86	100		dB	$T_{MIN} \le T_A \le T_{MAX}$

NOTES:

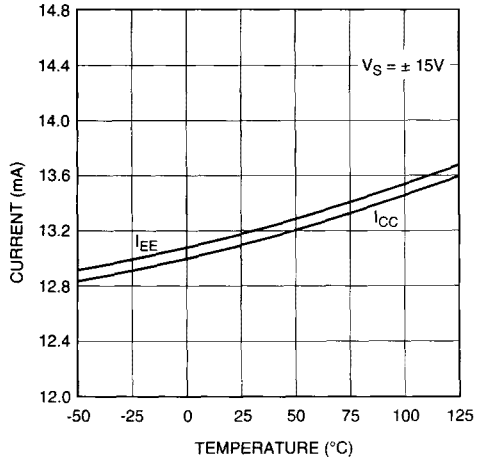
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. This parameter is measured at ambient temperature extremes in a high speed test environment, consequently, steady-state heating effects from internal power dissipation are not included.
4. Based on a three volt delta in each supply, i.e. 15V = ±1.5VDC.
5. This parameter is based on computer simulations and is not normally tested.
6. This parameter is guaranteed based on Hold-Mode output resistance and DC Gain measurements using: R_O (Sample Mode) = $\frac{R_O \text{ (Hold) mode}}{1 + A_{VOL}}$ (unity gain configuration).
7. This parameter is controlled by design and process control and is not normally tested.

TYPICAL PERFORMANCE CHARACTERISTICS

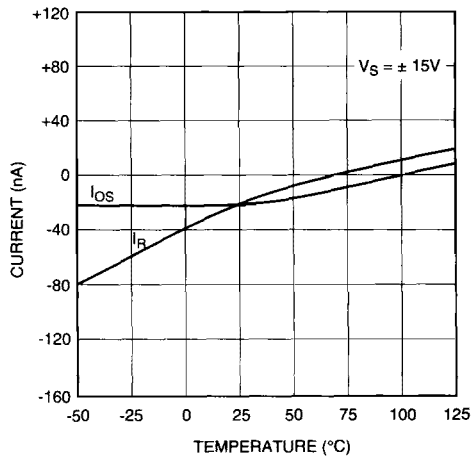
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



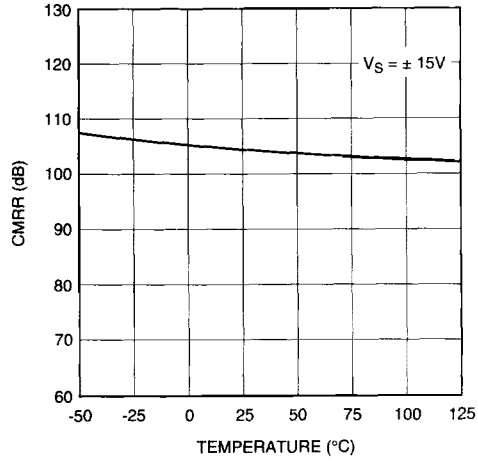
POWER SUPPLY CURRENT vs. TEMPERATURE



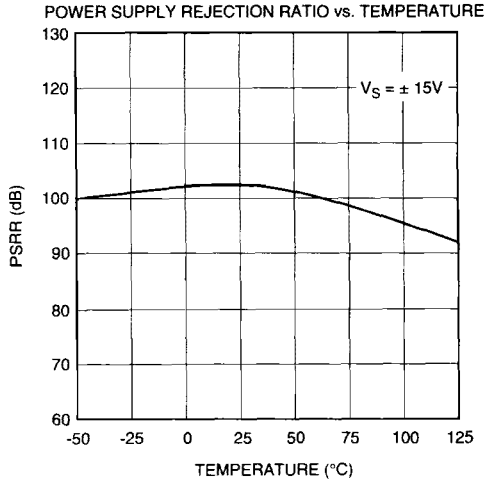
POWER SUPPLY CURRENT vs. TEMPERATURE



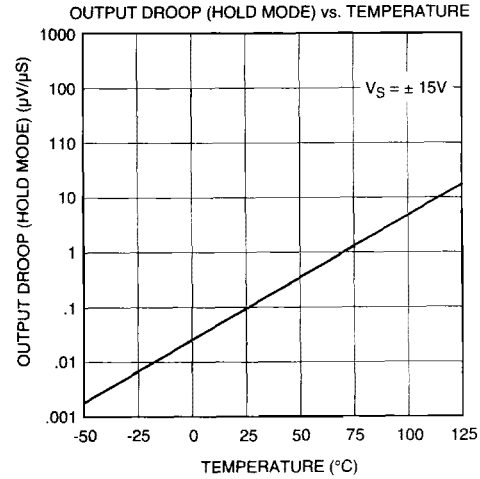
COMMON MODE REJECTION RATIO vs. TEMPERATURE



POWER SUPPLY REJECTION RATIO vs. TEMPERATURE

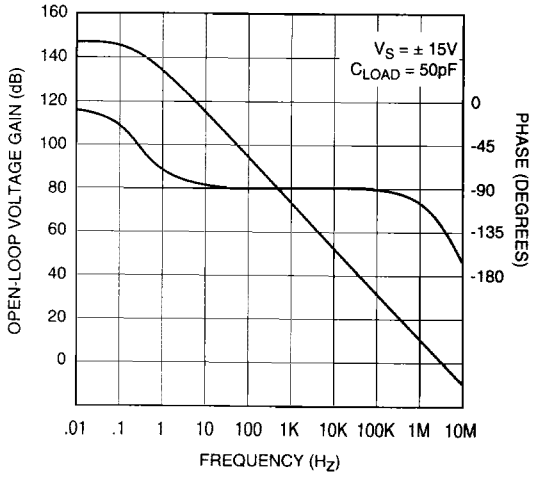


OUTPUT DROOP (HOLD MODE) vs. TEMPERATURE

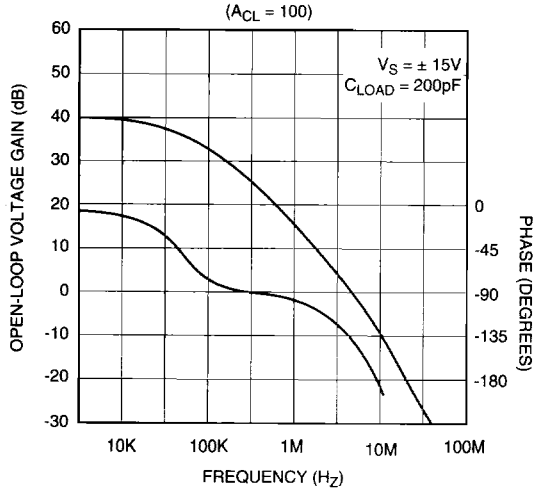


TYPICAL PERFORMANCE CHARACTERISTICS

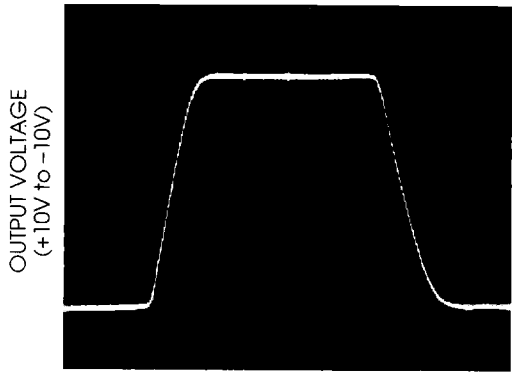
OPEN-LOOP FREQUENCY RESPONSE



CLOSED-LOOP FREQUENCY RESPONSE
(A_{CL} = 100)

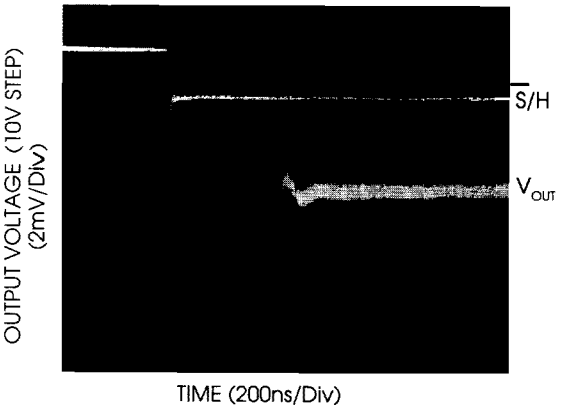


LARGE SIGNAL PULSE RESPONSE

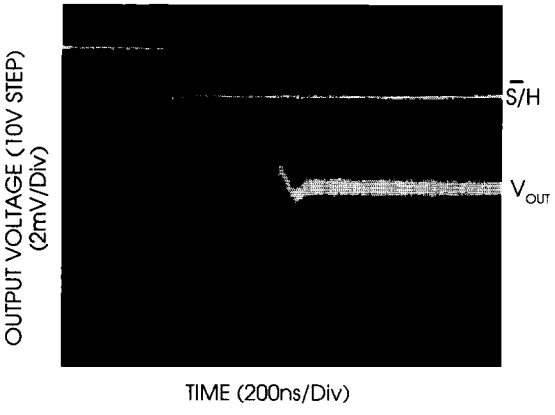


SMALL SIGNAL PULSE RESPONSE

POSITIVE ACQUISIION TIME



NEGATIVE ACQUISITION TIME



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GENERAL APPLICATION INFORMATION

The opamp like uncommitted differential pair input stage of the **SP5330** allows this sample–and–hold device to be combined with a variety of conventional opamp circuit configurations. for example, to configure the **SP5330** as a unity gain non-inverting amplifier, simply connect the output to the input.

The **SP5330** pedestal error is factory–trimmed and is typically less than 0.5mV (25°C). This error can also be adjusted to zero by connecting a 10KΩ to 50KΩ offset adjust potentiometer between the offset adjust pins. The potentiometer center tap must be connected to V–.

The high speed and precision offered by the **SP5330** make it especially attractive for application as an input device to high speed 12–bit A/D converters and data acquisition systems.

Board Layout Considerations

For best results, the **SP5330** should be used on a printed circuit board with a ground plane. The recommended ground connections are the device signal ground tied directly to the system signal ground (analog ground) and the device power ground tied directly to the system power ground

For best operation of the **SP5330**, effective supply bypassing is required. Ceramic bypass capacitors (0.01μF to 0.1μF) should be connected from each power supply terminal to the power ground terminal.

Hold Capacitor

An external hold capacitor is not required when using the **SP5330**. The **SP5330** includes an on chip 90pF MOS hold capacitor. The performance specified in the electrical characteristics table is based on this internal hold capacitor.

Output Stage

The output stage of the **SP5330** has been designed to maintain low output impedance even at high frequencies. This feature is especially attractive in high speed conversion applications where step changes in load current will introduce a voltage error term. It's low output impedance allows the **SP5330** to absorb these load changes with minimum voltage error.

In order to achieve it's low output impedance, the **SP5330** does not utilize short circuit protection. Consequently, care should be taken in using the device. A momentary short circuit to ground is permissible but a short of indefinite duration may lead to degradation or destruction of the device.

GLOSSARY OF TERMS

Acquisition Time:

The time required following a "sample" command, for the output to reach it's final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time, and setting time.

Aperture Time:

The time required for the sample–and–hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer form the saple to the hold mode. It is also referred to as "offset step" or "pedestal error".

Effective Aperture Delay Time (EADT):

The difference between propagation time of the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occured before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DIE TOPOLOGY

DIMENSIONS:
149 x 98 x 21 MILS

PROCESS:
Complementary Bipolar Di,
Nichrome Thin Film Resistors

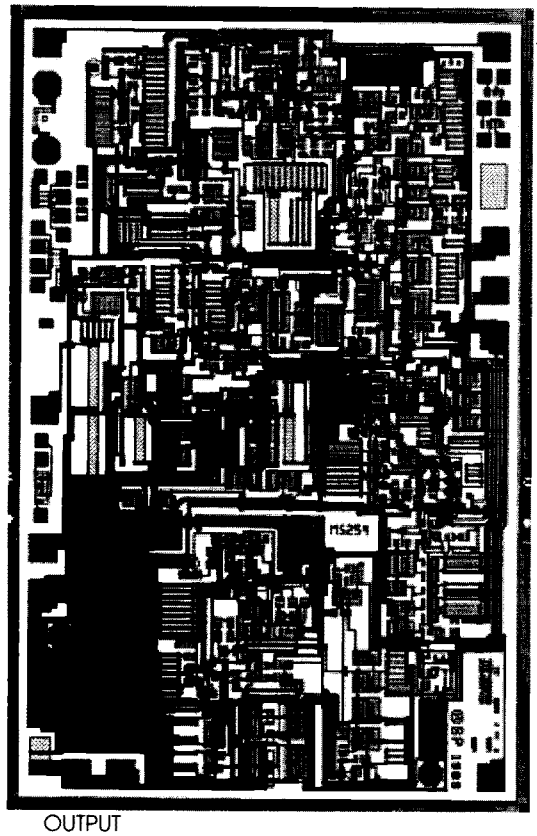
PASSIVATION:
12KÅ ±2KÅ, Vapox

WORST-CASE CURRENT DENSITY:
1.0×10^5 A/cm²

METALLIZATION:
12KÅ ±2KÅ, Aluminum

SUBSTRATE CONNECTION:
Substrate is not powered up.
Recommended conection is to Signal Gnd.

METALLIZATION PATTERN



ORDERING INFORMATION	
0°C to +75°C:	
SP1–5330–5	14 Pin Cerdip
SP4–5330–5	20 Pin LCC
–25°C to +85°C:	
SP1–5330–4	14 Pin Cerdip
SP4–5330–4	20 Pin LCC
–55°C to +125°C:	
SP1–5330–2	14 Pin Cerdip
SP4–5330–2	20 Pin LCC
Room Temp, Probe Test:	
SP0–5330–5	Chip Form
Full Compliance to MIL-STD-883:	
SP1–5330/883	14 Pin Cerdip
SP4–5330/883	20 Pin LCC

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