PYRAMID SEMICONDUCTOR CORPORATION

P4C1049/P4C1049L

HIGH SPEED 512K X 8 STATIC CMOS RAM

FEATURES

- **High Speed (Equal Access and Cycle Times)**
  - **— 15/20/25 ns (Commercial)**
  - **— 20/25/35 ns (Industrial)**
  - **— 20/25/35/45/55/70 ns (Military)**
- **Low Power**
- **Single 5V±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  - **—32-Pin Ceramic DIP (600 mil)**
  - **—36-Pin SOJ (400 mil)**
  - **—36-Pin FLATPACK**
  - **—36-Pin LCC (452 mil x 920 mil)**

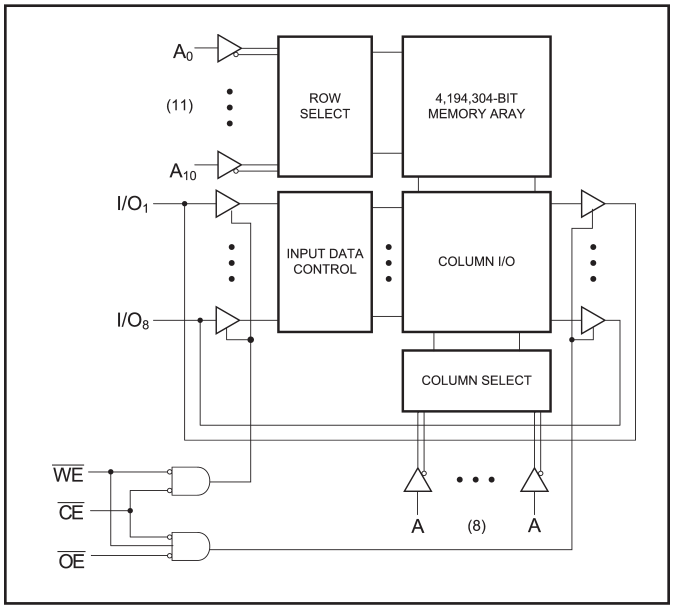
DESCRIPTION

The P4C1049 is a 4 Megabit high-speed CMOS static RAM organized as 512Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

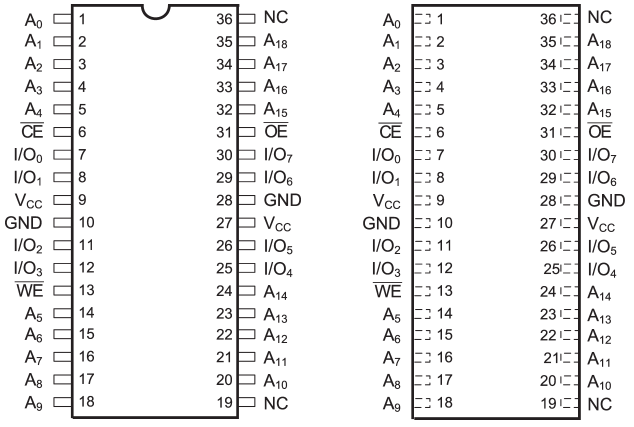
Access times as fast as 15 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1049 is a member of a family of PACE RAM™ products offering fast access times.

The P4C1049 device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{18}. Reading is accomplished by device selection ($\overline{CE}$) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



SOLDER-SEAL FLAT-PACK (FS-4), SOJ (J9, CJ2)

LCC (L11)

DIP PIN-OUT INSIDE DATASHEET

MAXIMUM RATINGS[1]

Sym	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	-0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	GND	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Sym	Parameter	Conditions	Typ	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	pF

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

Sym	Parameter	Test Conditions		P4C1049		P4C1049L		Unit
				Min	Max	Min	Max	
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3[3]	0.8	-0.3[3]	0.8	V
V_{HC}	CMOS Input High Voltage			V_{CC} - 0.2	V_{CC} + 0.3	V_{CC} - 0.2	V_{CC} + 0.3	V
V_{LC}	CMOS Input Low Voltage			-0.3[3]	0.2	-0.3[3]	0.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min			0.4		0.4	V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = -4 mA, V_{CC} = Min		2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max, V_{IN} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{LO}	Output Leakage Current	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	-10	+10	-5	+5	µA
			IND/COM	-5	+5	N/A	N/A	
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max, f = Max, Outputs Open	MIL	—	45	—	40	mA
			IND/COM	—	40	—	N/A	
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max, f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	MIL	—	15	—	10	mA
			IND/COM	—	10	—	N/A	

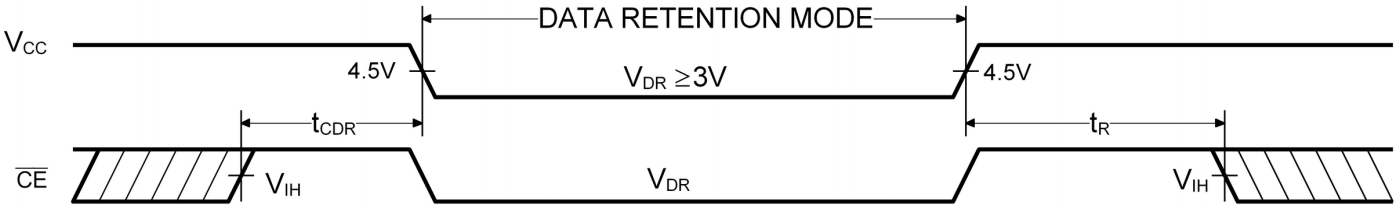
N/A = Not applicable

DATA RETENTION CHARACTERISTICS (P4C1049L Military Temperature Only)

Sym	Parameter	Test Conditions	Min	Typ* V_{cc}=	Max V_{cc}=	Unit
				2.0V	2.0V	
V_{DR}	V_{CC} for Data Retention		3.0			V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2	3	mA
t_{CDR}	Chip Deselect to Data Retention Time		0			ns
t_R†	Operation Recovery Time		t_{RC}§			ns

* T_A = +25°C
§ t_{RC} = Read Cycle Time
† This Parameter is guaranteed but not tested

DATA RETENTION WAVEFORM



POWER DISSIPATION CHARACTERISTICS VS. SPEED

Sym	Parameter	Temperature Range	-15	-20	-25	-35	-45	-55	-70	Unit
I_{CC}	Dynamic Operating Current*	Commercial	220	185	180	N/A	N/A	N/A	N/A	mA
		Industrial	N/A	190	185	175	N/A	N/A	N/A	mA
		Military	N/A	200	195	185	175	170	165	mA

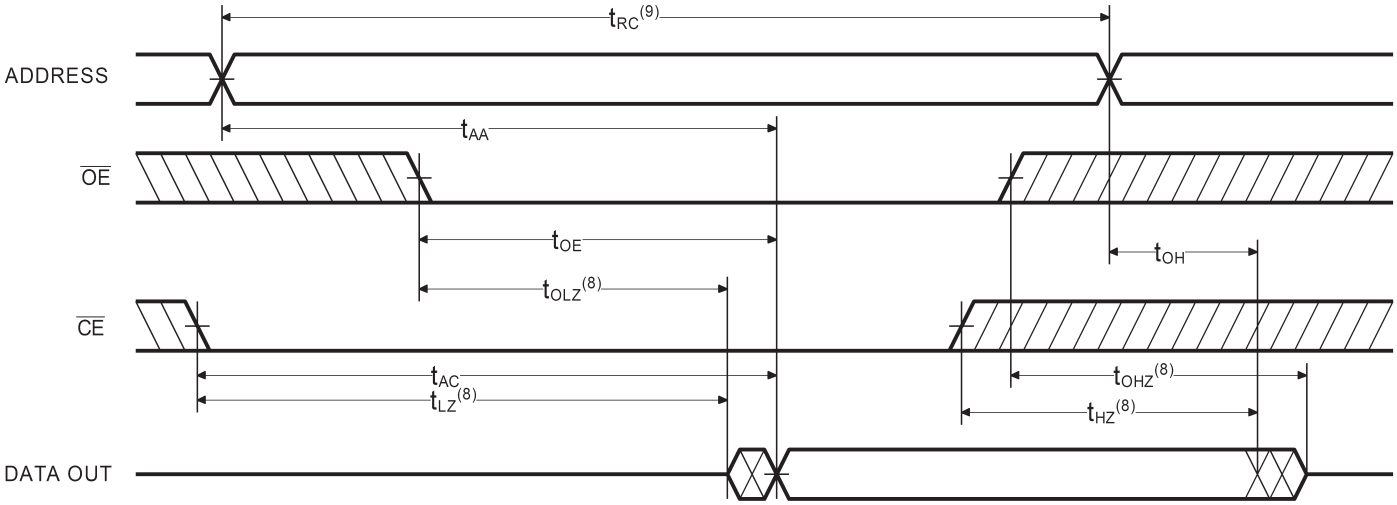
* V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

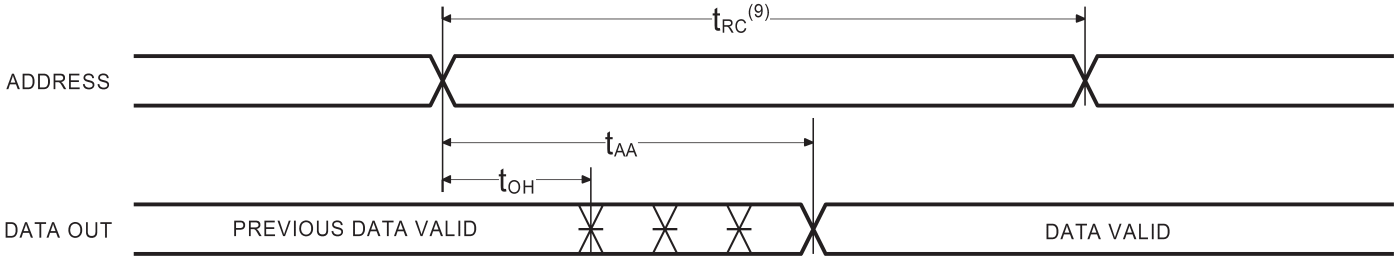
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		25		35		45		55		70		ns
t_{AA}	Address Access Time		15		20		25		35		45		55		70	ns
t_{AC}	Chip Enable Access Time		15		20		25		35		45		55		70	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		8		9		11		15		20		25		30	ns
t_{OE}	Output Enable Low to Data Valid		7		9		10		15		20		25		30	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		7		9		10		15		20		25		30	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		15		20		25		35		45		55		70	ns

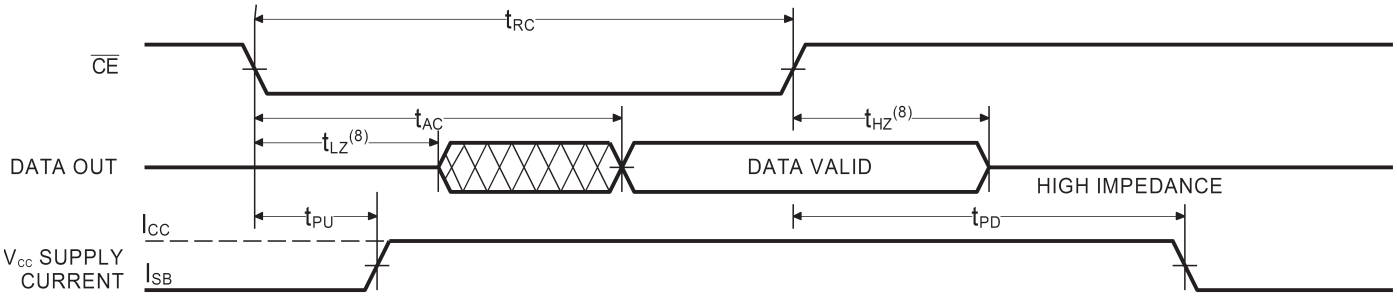
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED) (5, 7)



AC CHARACTERISTICS—WRITE CYCLE

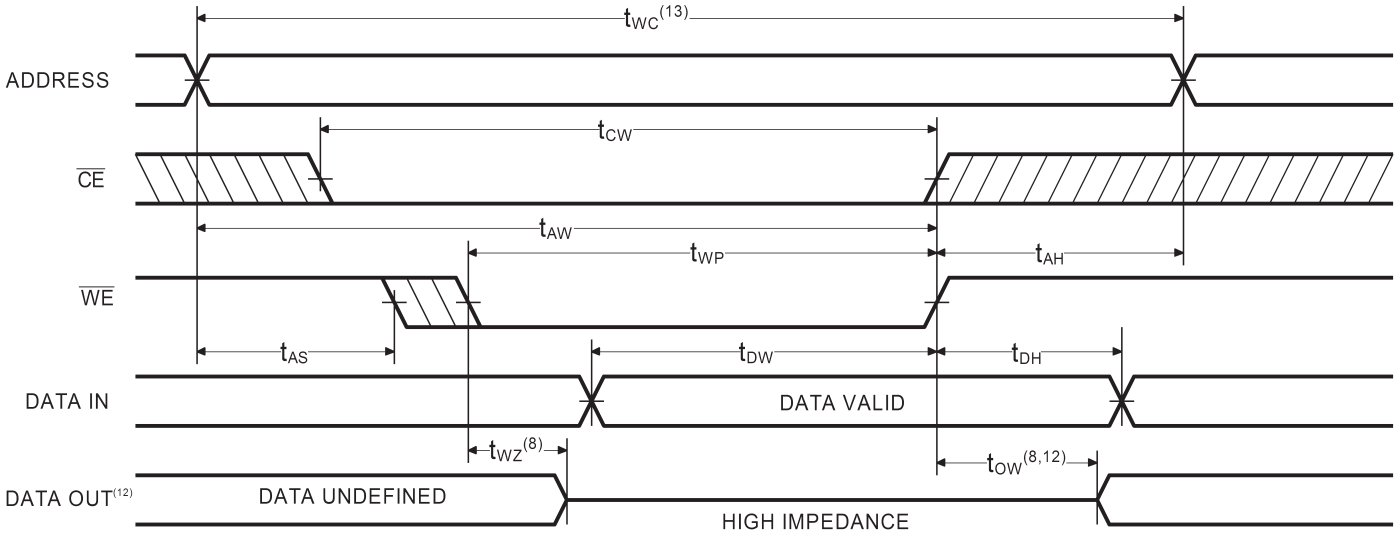
(V_{CC} = 5V ± 10%, All Temperature Ranges)(2)

Sym	Parameter	-15		-20		-25		-35		-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		25		35		45		55		70		ns
t_{CW}	Chip Enable Time to End of Write	12		14		18		22		30		35		40		ns
t_{AW}	Address Valid to End of Write	12		14		16		20		25		35		40		ns
t_{AS}	Address Setup Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		14		16		22		25		30		35		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	9		11		13		15		20		25		30		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		8		10		11		15		18		25		30	ns
t_{OW}	Output Active from End of Write	3		3		3		5		5		5		5		ns

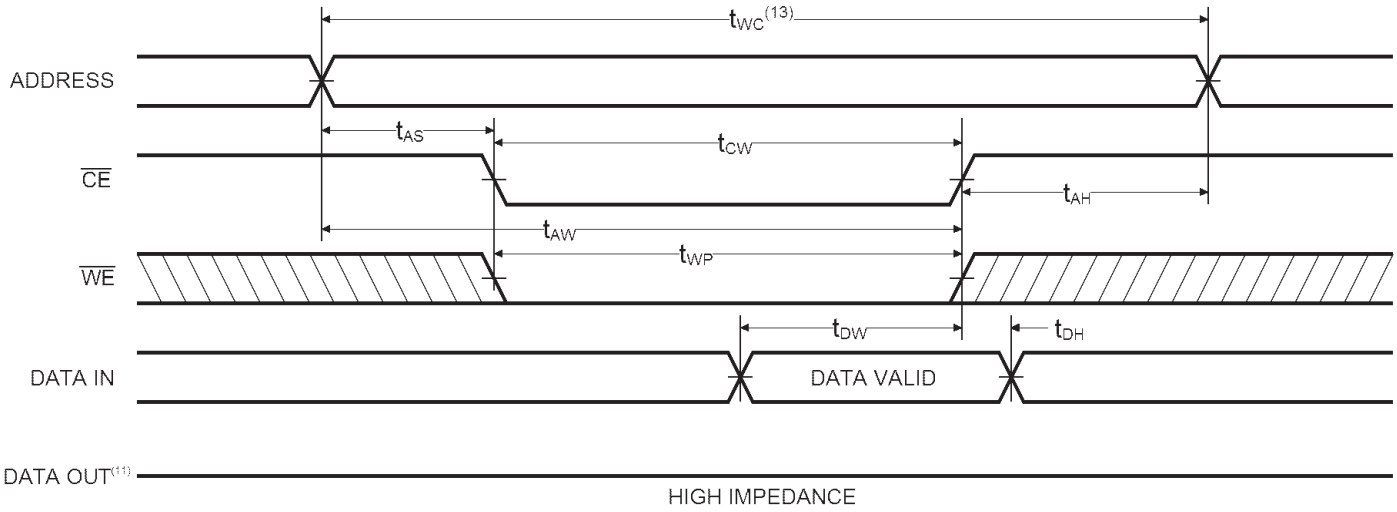
Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –2.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10,11]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[10]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**I/O**	**Power**
Standby	H	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	High Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	High Z	Active

Notes:
10. $\overline{CE}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
13. Write Cycle Time is measured from the last valid address to the first transitioning address.

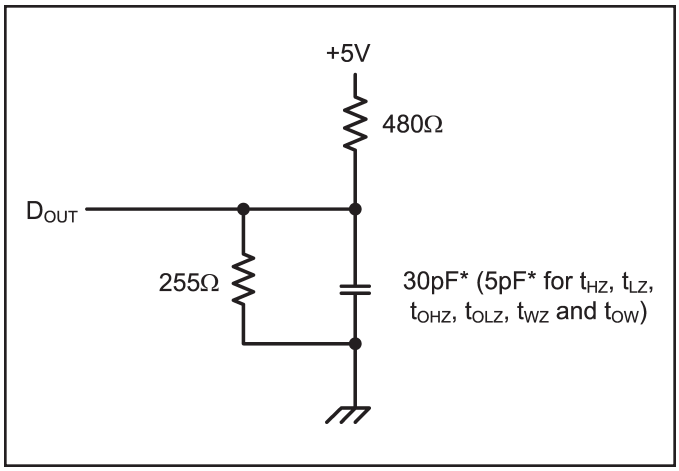


Figure 1. Output Load

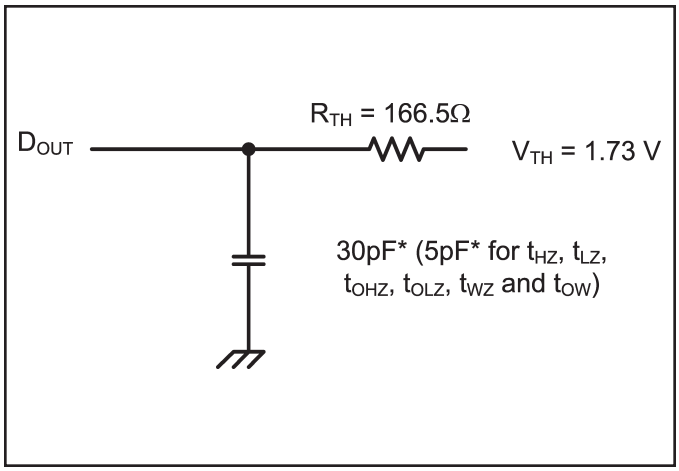
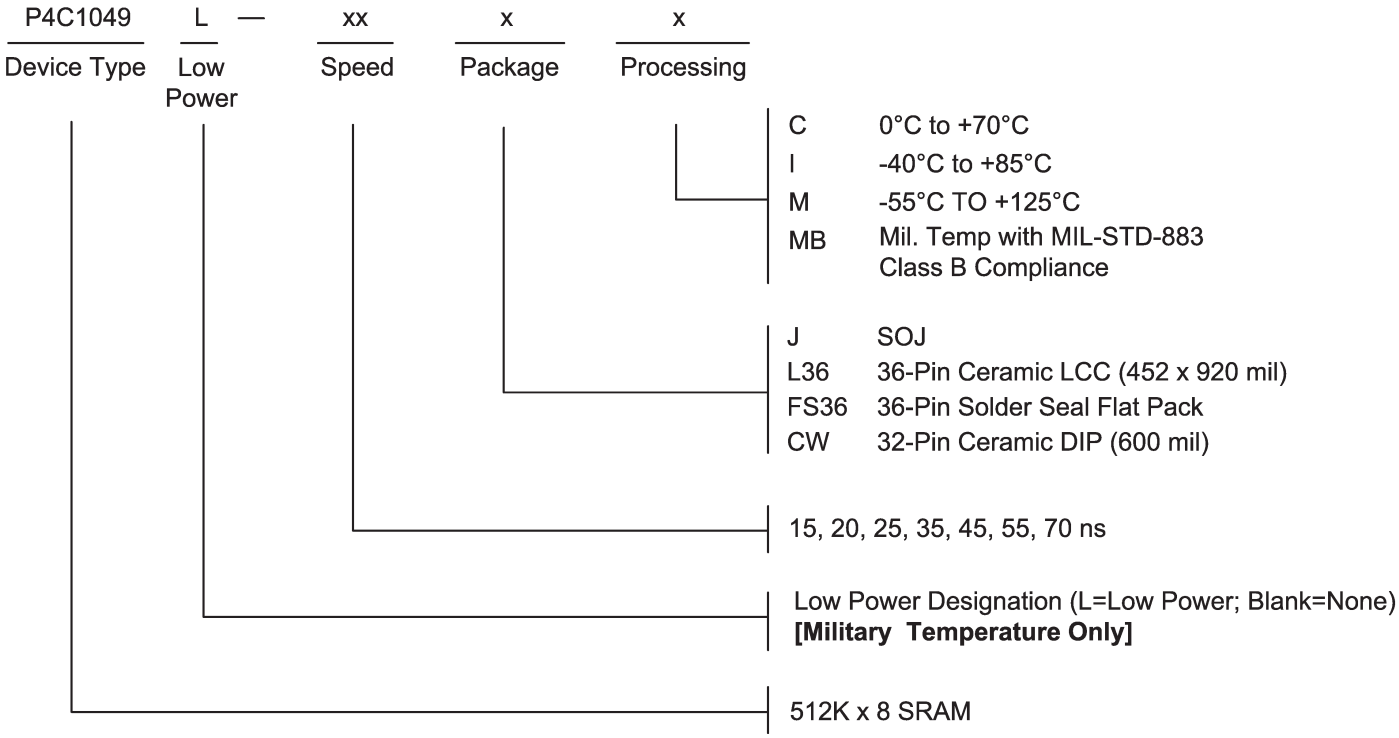


Figure 2. Thevenin Equivalent

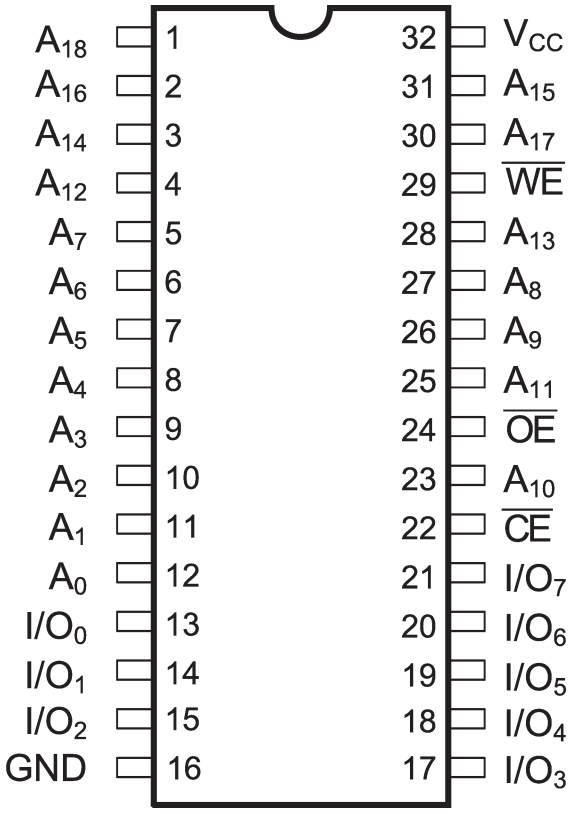
* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C1049/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



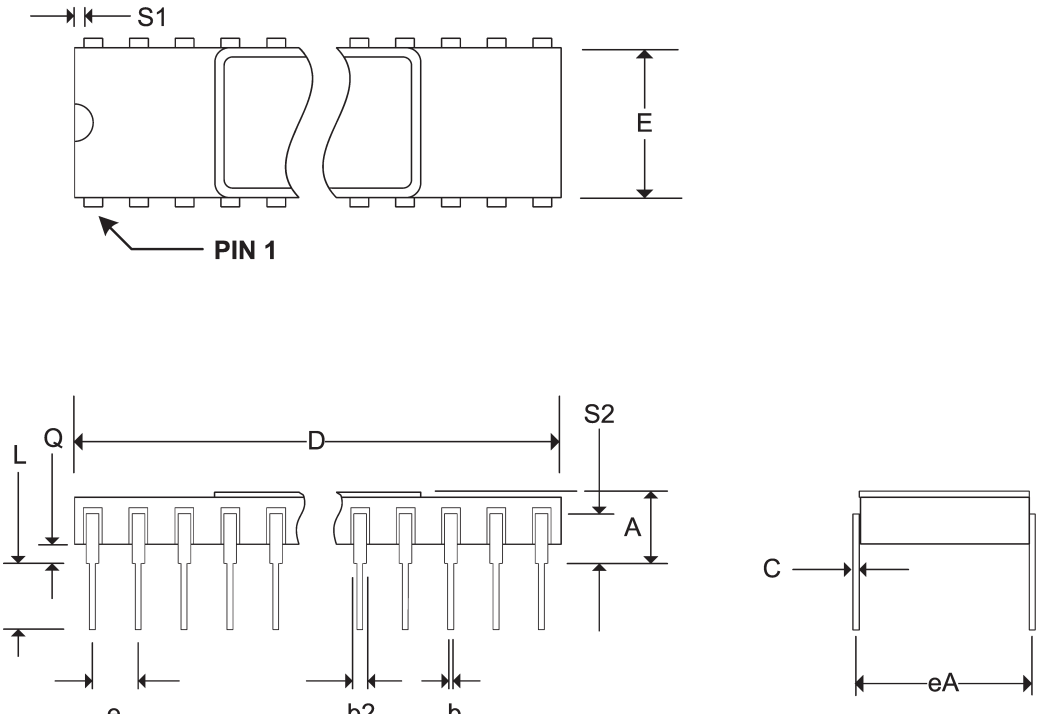
32-PIN CERAMIC DIP PIN CONFIGURATION



32-Pin DIP (C10)

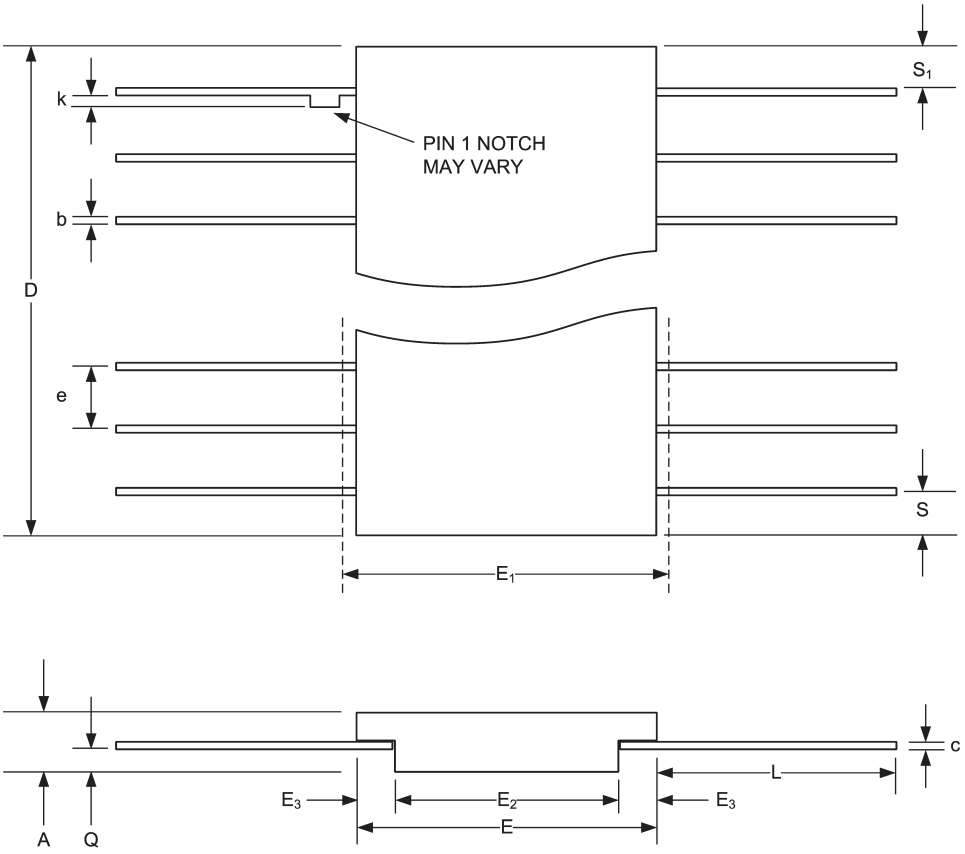
Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

SIDEBRAZED DUAL IN-LINE PACKAGE



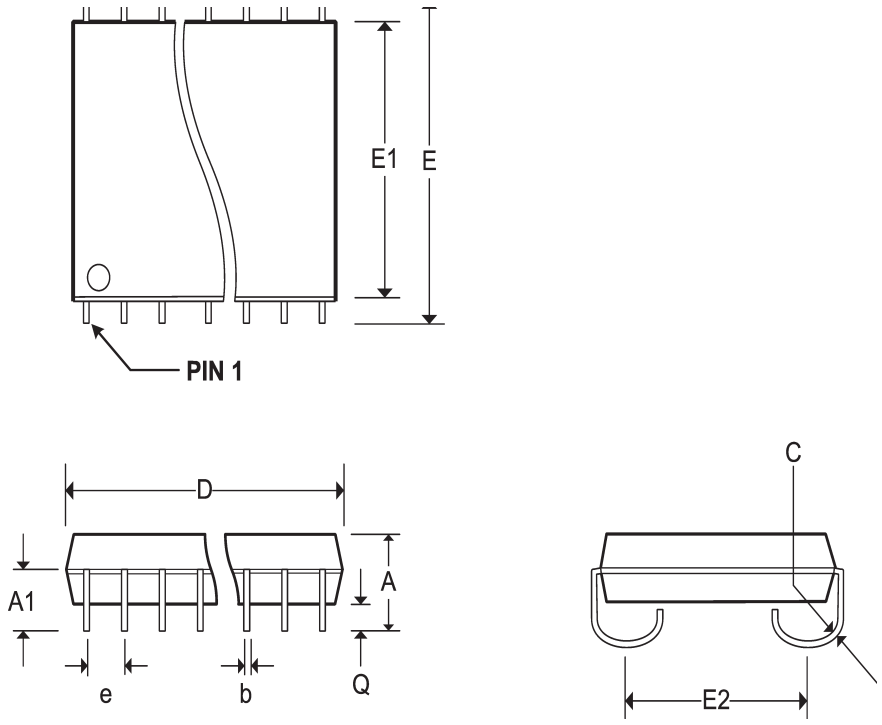
Pkg #	FS-4	
# Pins	36	
Symbol	**Min**	**Max**
A	0.089	0.125
b	0.015	0.019
c	0.003	0.007
D	0.910	0.930
E	0.505	0.515
E1	-	0.530
E2	0.385	0.395
E3	0.055	0.065
e	0.050 BSC	
L	0.300	0.350
Q	0.015	0.038
S	-	0.045
M	-	0.002
N	36	

SOLDER SEAL FLATPACK



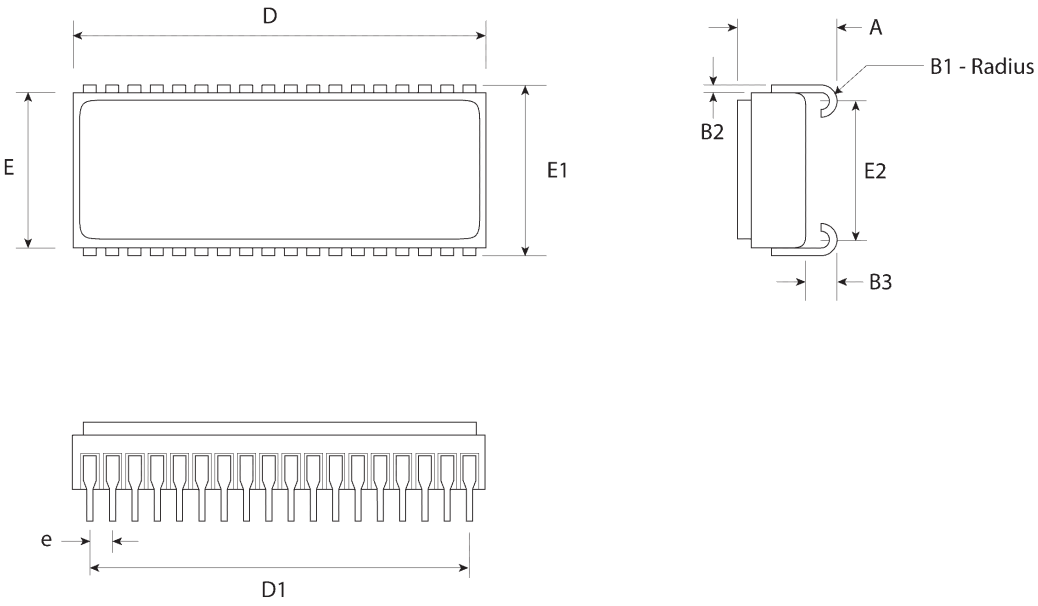
Pkg #	J9	
# Pins	36	
Symbol	**Min**	**Max**
A	0.130	0.145
A1	0.082	-
b	0.015	0.020
C	0.007	0.013
D	0.920	0.930
e	0.050 BSC	
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
Q	0.045	0.055

SOJ SMALL OUTLINE IC PACKAGE



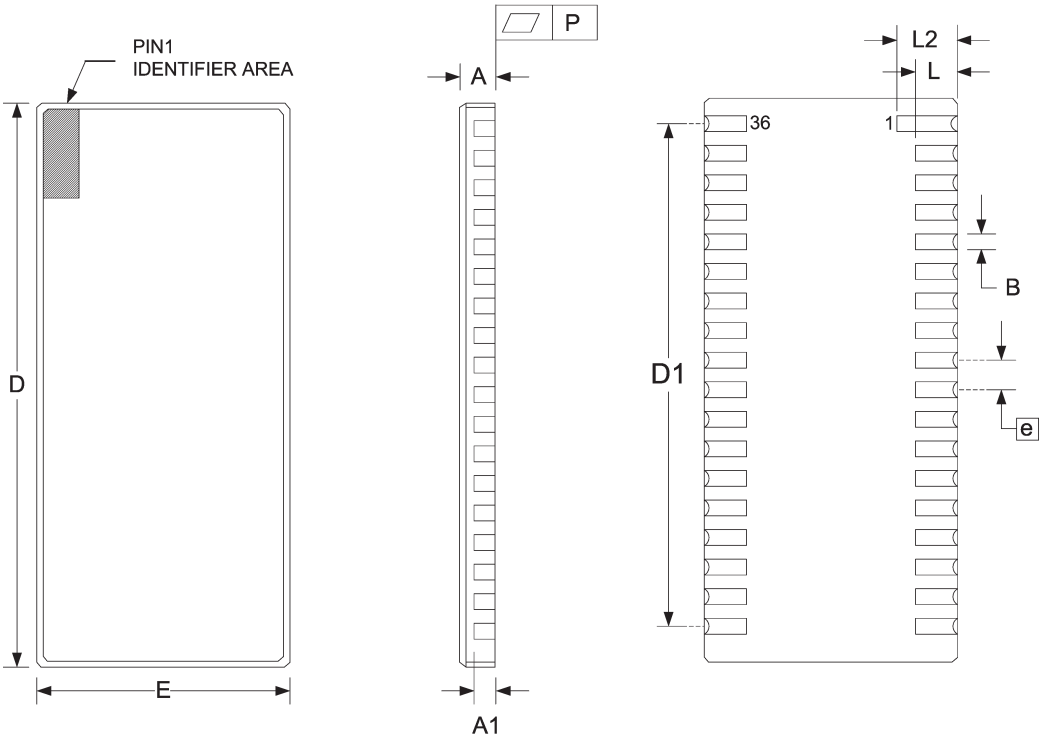
Pkg #	CJ2	
# Pins	36	
Symbol	**Min**	**Max**
A	0.120	0.165
B1	0.030R TYP	
B2	0.020 REF	
B3	0.025	0.045
D	0.816	0.838
E	0.419	0.431
E2	0.360	0.380
e	0.050 BSC	
E1	0.430	0.454

CERAMIC SOJ SMALL OUTLINE IC PACKAGE



Pkg #	L11	
# Pins	36	
Symbol	**Min**	**Max**
A	0.080	0.100
A1	0.054	0.066
B	0.022	0.028
D	0.910	0.930
D1	0.840	0.860
E	0.445	0.460
e	.050 BSC	
L	.100 TYP	
L2	0.115	0.135
P	-	0.006
R	.009 TYP	

RECTANGULAR LEADLESS CHIP CARRIER



REVISIONS

DOCUMENT NUMBER	SRAM 128
DOCUMENT TITLE	P4C1049/P4C1049L - HIGH SPEED 512K X 8 STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Oct-2005	JDB	New Data Sheet
A	Jan-2008	JDB	Added CJ2 Ceramic SOJ Package
B	Mar-2009	JDB	Added C10 Ceramic DIP Package