

P35-4210

GaAs MMIC RF SWITCH

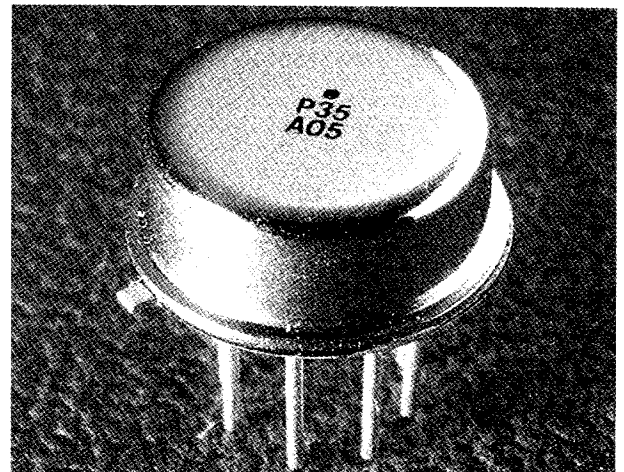
2GHz SPDT/SPST

Applications

- R.F. switch to 1000MHz in T05 package 2000MHz in chip form
- Ideal for PIN switch replacement where minimal current is required (typically $< 10\mu A$)
- Fast switching speeds ($< 1ns$) with driver waveform enhancement
- Low loss signal routing
- Usable as a voltage controlled rf attenuator
- Fast modulator

Features

- All gold bonding pads
- Silicon nitride chip passivation for improved handling and long term reliability
- Available in either chip form or hermetically packaged (T05) in SPDT and SPST configurations
- No off chip decoupling components required
- Can be combined to configure multifunction switches



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P35-4210-0 SPDT Chip
RF Electrical Specification (at 25 °C)

Sym	Parameter and Conditions	Units	Min	Typ	Max
L	Insertion loss $RF_{IN} \rightarrow RF_1$ or 2	dB			
	10MHz		-	0.5	0.6
	100MHz		-	0.5	0.6
	500MHz		-	0.6	0.7
	1GHz		-	0.6	0.7
I	Isolation $RF_{IN} \rightarrow RF_1$ or 2	dB			
	10MHz		45	55	-
	100MHz		40	45	-
	500MHz		30	33	-
	1GHz		25	28	-
S	Input V.S.W.R. (low loss into termination)				
	10-1000MHz		-	1.13	1.2
	1-2GHz		-	1.2	1.3
P_{OUT}	Input power	+dBm			
	1 dB Compression point				
	at 10MHz		20	22	-
	250MHz		25	29	-
	1GHz	28	33	-	

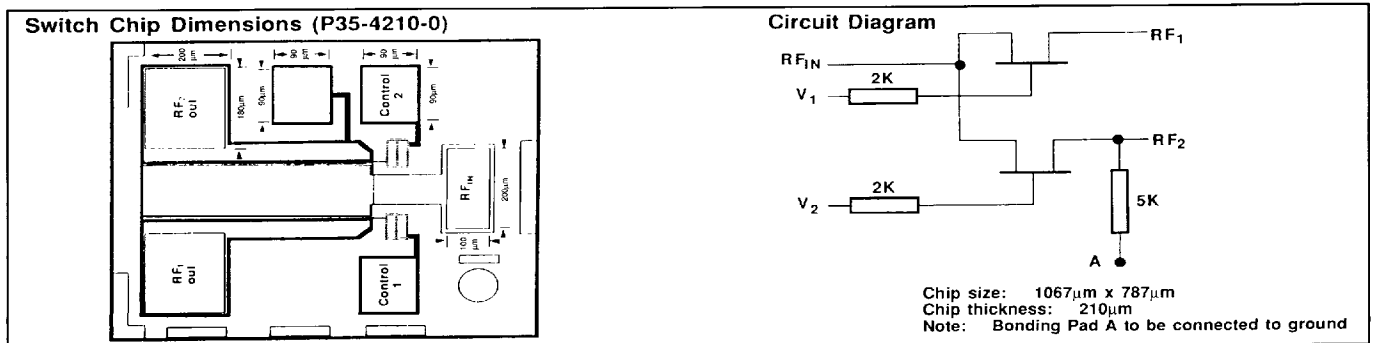
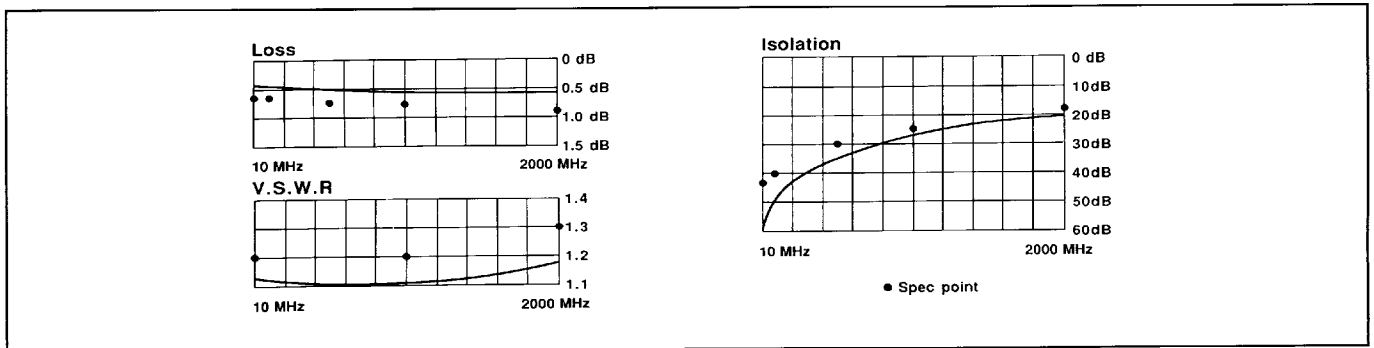
Description

The P35-4210-0 is an integrated circuit GaAs MESFET SPDT switch usable at frequencies up to 2GHz

Notes:

1. Isolation $RF_1 \rightarrow RF_2$ typically better than - 30dB.
2. Chip thermal impedance 120°C/W

Typical RF Characteristics



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P35-4210-1 SPDT T05 Package
RF Electrical Specification (at 25 °C)

Sym	Parameter and Conditions	Units	Min	Typ	Max
L	Insertion loss $RF_{IN} \rightarrow RF_1$ or 2 10MHz 100MHz 500MHz 1GHz	dB	-	0.5 0.6 0.7 0.8	0.7 .9 1.0 1.1
I	Isolation $RF_{IN} \rightarrow RF_1$ or 2 10MHz 100MHz 500MHz 1GHz	dB	50 40 29 25	60 48 33 30	- - - -
S	Input V.S.W.R. (50 ohm terminations) 10-1000MHz		-	1.2	1.3
P_{IN}	Input power at which insertion loss compresses by 1 dB at 10MHz 250MHz 1GHz	+dBm	20 25 28	22 29 33	- - -

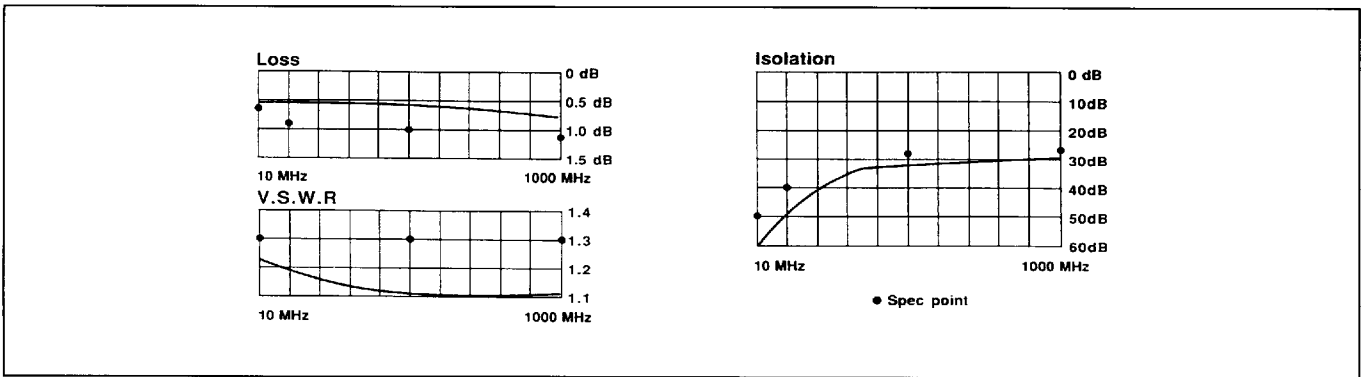
Description

The P35-4210-1 utilises the P35-4210-0 chip, hermetically sealed in an 8-lead T05 package bonded in the SPDT configuration, usable to 1GHz.

Notes:

1. Isolation $RF_1 \rightarrow RF_2$ typically better than -30dB.

Typical RF Characteristics



Pin Configuration

Ground plane
5mm PCD
RF₂ 2 RF₁ 6
V₂ 1 V₁ 7
RF_{IN} 8
Tag
Bottom view of T05 can

Pin Identification

Pin	Function
1	V ₂
2	RF ₂
3	NC
4	GND
5	NC
6	RF ₁
7	V ₁
8	RF _{IN}

Circuit Diagram

RF_{IN} RF₁
V₁ 2K
V₂ 2K
RF₂ 5K
GND

P35-4210-2 SPST Reflective T05 Package
RF Electrical Specification (at 25 °C)

Sym	Parameter and Conditions	Units	Min	Typ	Max
L	Insertion loss $RF_{IN} \rightarrow RF_1$ or 2	dB			
	10MHz		-	0.4	0.6
	100MHz		-	0.5	0.8
	500MHz		-	0.6	0.9
	1GHz	-	0.7	1.0	
I	Isolation $RF_{IN} \rightarrow RF_1$ or 2	dB			
	10MHz		60	>60	-
	100MHz		55	60	-
	500MHz		35	40	-
	1GHz	25	30	-	
S	Input V S W R (50 ohm terminations) 10-1000MHz			1.2	1.3
P_{IN}	Input power at which insertion loss compresses by 1 dB at	+dBm			
	10MHz		20	22	-
	250MHz		25	29	-
	1GHz		28	33	-

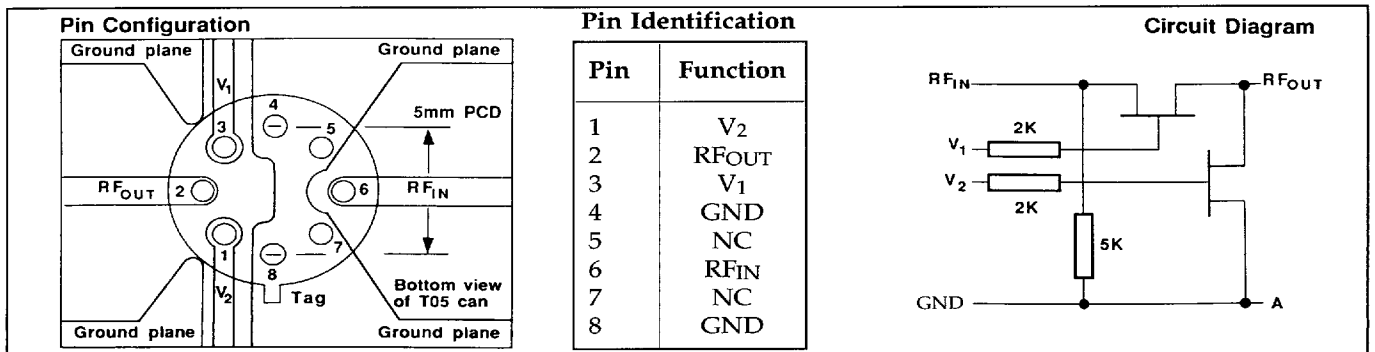
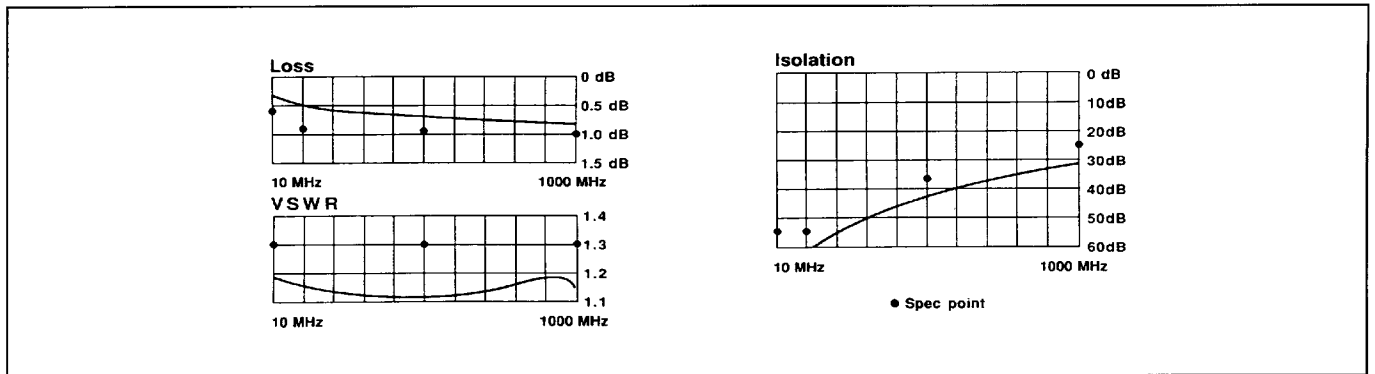
Description

The P35-4210-2 utilises the P35-4210-0 chip, hermetically sealed in an 8-lead T05 package. A serial/shunt bonding configuration is employed to provide an SPST function with a higher degree of isolation.

Notes:

1. It is important that pin 6 is used as RF_{IN}

Typical RF Characteristics



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P35-4210-3 SPST Non-Reflective T05 Package
RF Electrical Specification (at 25 °C)

Sym	Parameter and Conditions	Units	Min	Typ	Max
L	Insertion loss $RF_{IN} \rightarrow RF_1$ or 2	dB	-	0.5	0.7
	10MHz				
	100MHz				
	500MHz				
I	Isolation $RF_{IN} \rightarrow RF_1$ or 2	dB	50	60	-
	10MHz				
	100MHz				
	500MHz				
S _{IN}	Input V S W R (50 ohm terminations)		-	1.2	1.3
	10-1000MHz				
S _{OUT}	Output V S W R		-	1.3	1.8
P	Input power at which insertion loss compresses by 1 dB at	+dBm	20	22	-
	10MHz				
	250MHz				
	1GHz				

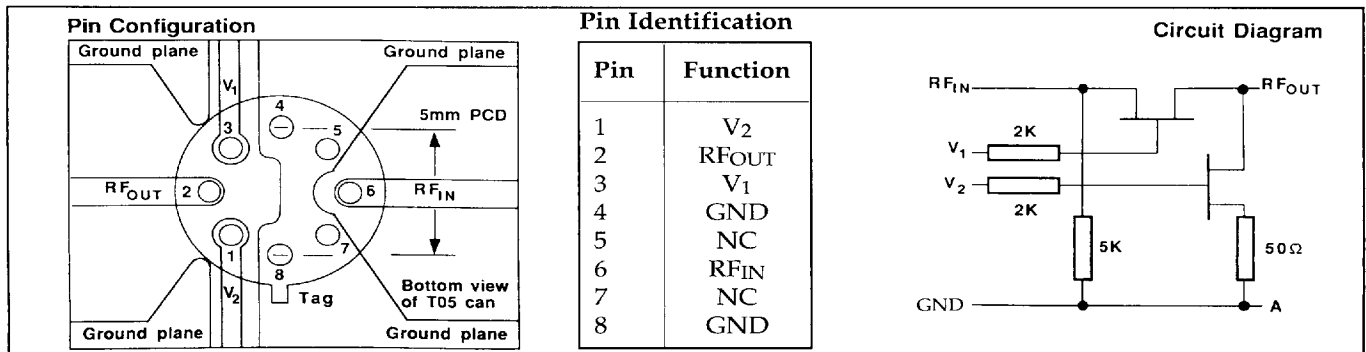
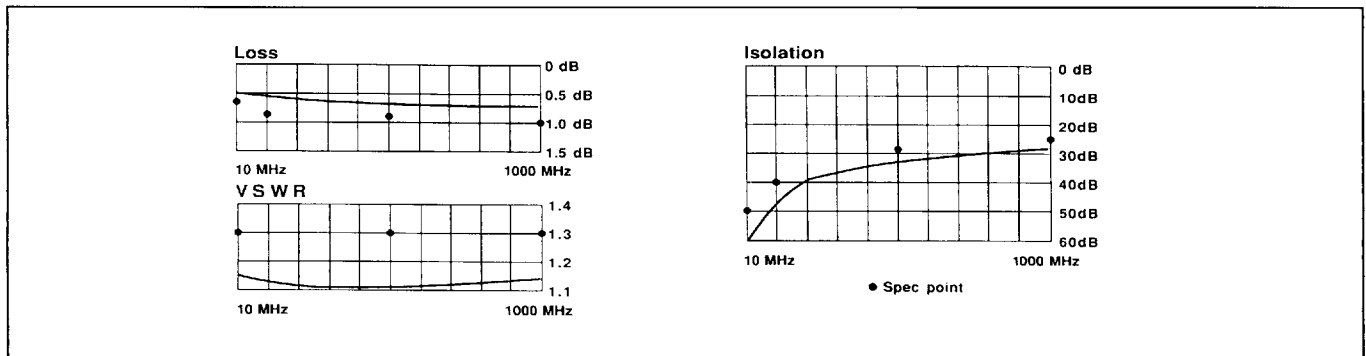
Description

The P35-4210-3 utilises the P35-4210-0 chip, hermetically sealed in an 8-lead T05 package. An integral, thin film chip resistor provides a matched 50ohm termination at the output port.

Notes:

1. It is important that pin 6 is used as RF_{IN} .
2. The maximum power at RF_{OUT} in the isolated state is +20dBm.

Typical RF Characteristics

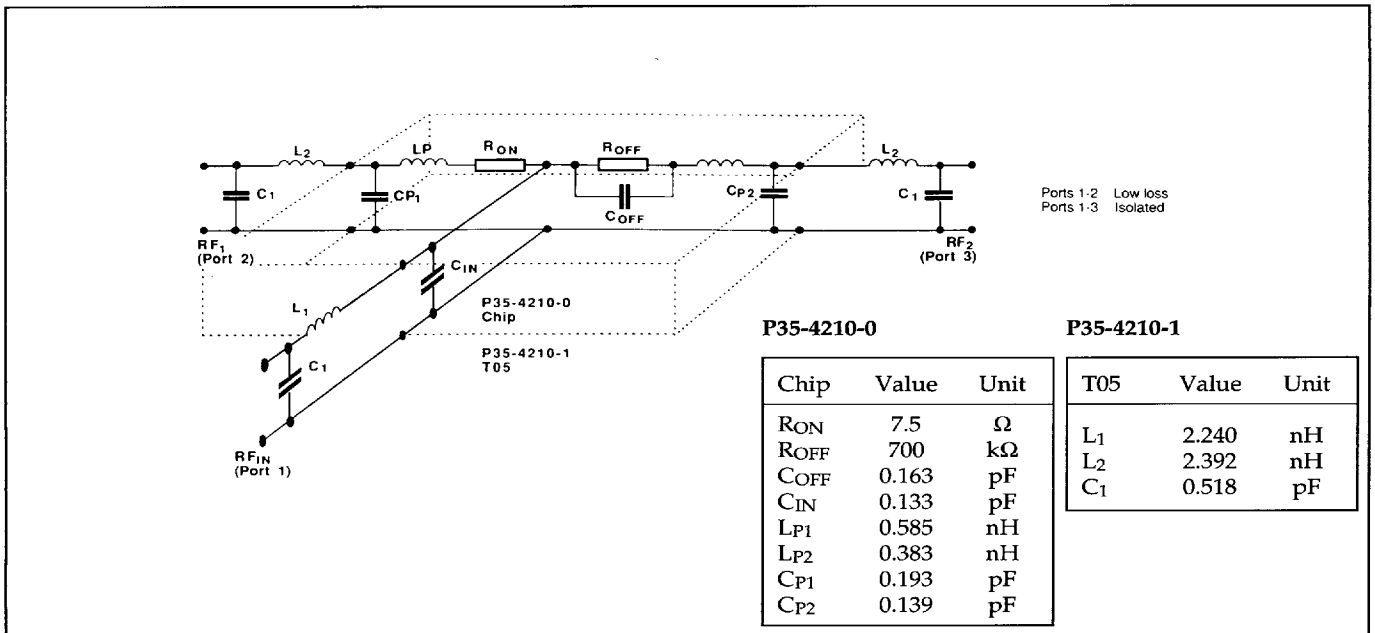


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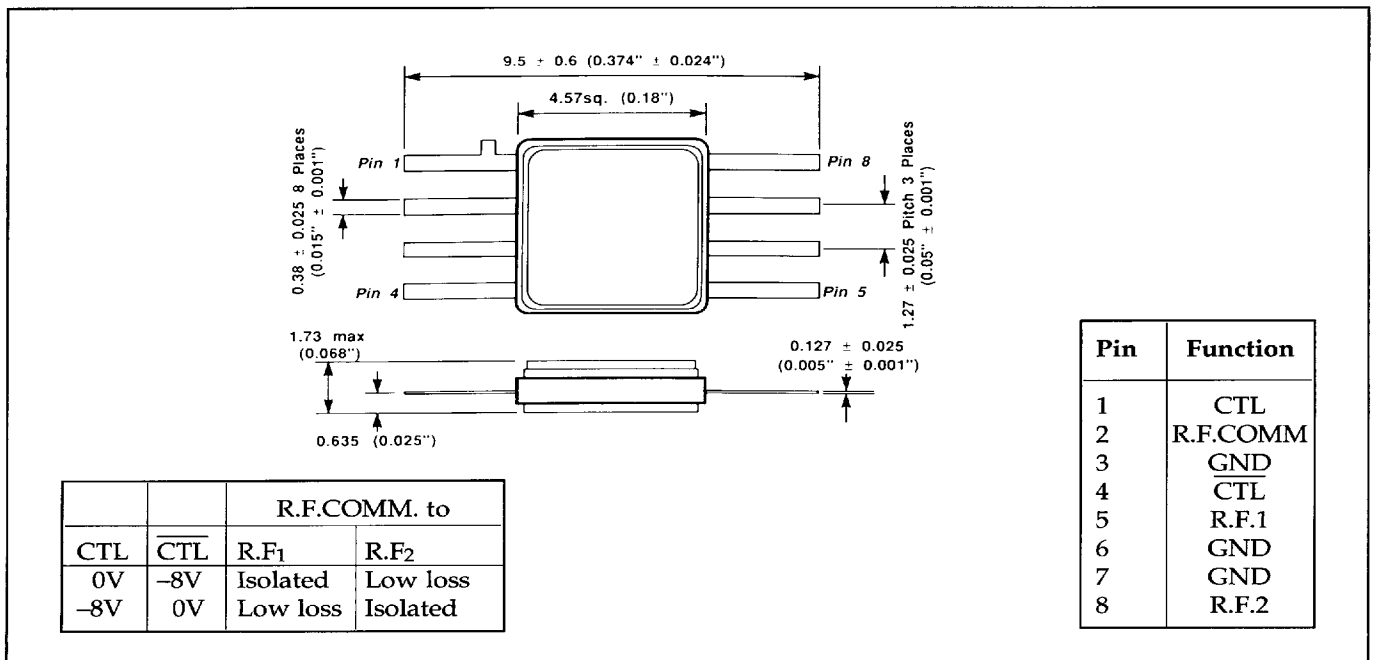
Equivalent Circuit Model (P35-4210-0/1) SPDT Switches



Notes:

The performance specification for the P35-4210-4 is as for the chip (P35-4210-0) to 2GHz

P35-4210-4 Surface Mount Package SPDT



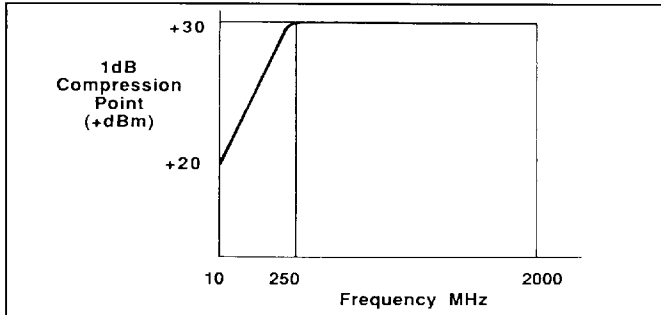
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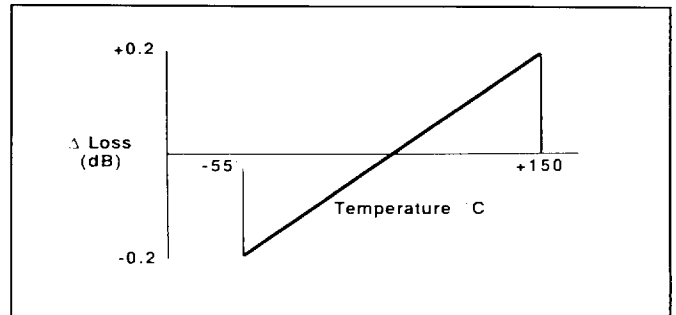
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General Characteristics

Compression Point Characteristics



Loss/Temperature Characteristics



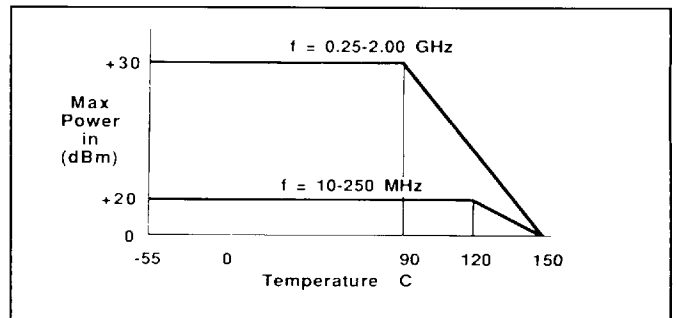
Intermodulation Distortion

Two tone input at 500 MHz and 1.0 watt power total

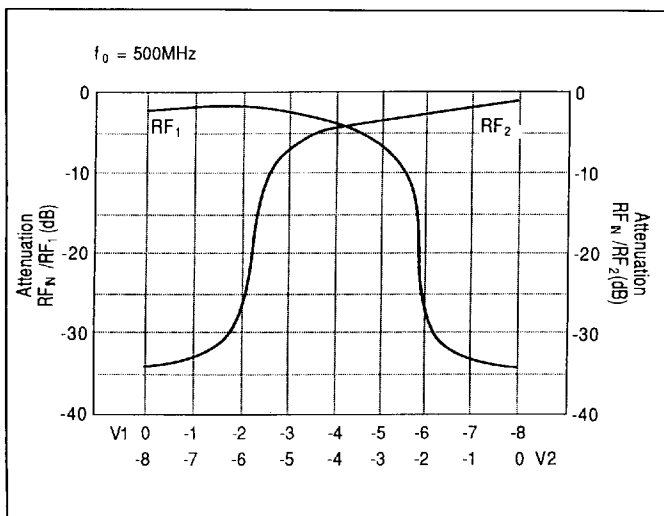
2nd order intercept point +51 dBm typ

3rd order intercept point +40 dBm typ

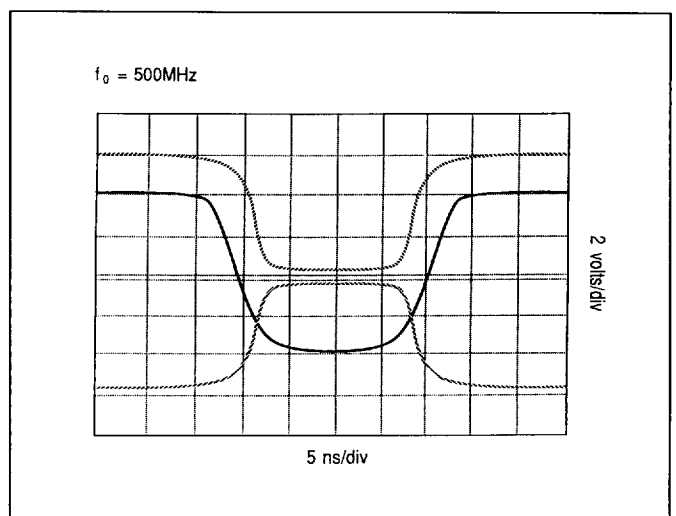
Maximum Power/Temperature Derating



Attenuation Characteristics



RF Switching Characteristics



Chip Handling, Mounting and Bonding

The back of the chip is metallized with Au-Ge and can be die-attached onto gold manually, eutectically, with Au-Ge or Au-Sn eutectic preforms or with low temperature conductive epoxy. The maximum allowable chip temperature is 280°C. The chip is fully passivated with silicon nitride and should be bonded onto the exposed gold pads with 15 or 25 microns pure gold, half-hard wire or gold mesh. Bonding should be achieved with the chip face at 225°C to 275°C with a heated thermosonic wedge (approx 125°C) and a maximum force of 60 grams. Ball bonds may be used but care must be taken to ensure the ball size is compatible with the bonding pads shown. The length of bond wires to RF ports should be minimised where possible. Bonding pad A should be bonded to ground to provide a D.C. return path. All wire bond lengths should be minimised to reduce parasitic inductance.

Handling Precautions

The FET switch device is static sensitive and can be damaged or destroyed by large transient voltages. Such transients can be generated by some bonding equipments and power supplies when switched on. It is also possible to induce large spikes from other equipment into long unscreened bias leads. The following precautions should be observed.

1. D.C. ground all equipment and operators.
2. Control pins V_1 and V_2 should be either grounded or negatively biased ($-12V$ max) and should not be either positively biased or allowed to 'float'.
3. D.C. voltages should not be applied to the RF ports of the device.
4. For slow switching or c.w. application, decoupling capacitors (eg low inductance $1\mu F$ tantalum) should be connected to the bias control lines V_1 and V_2 near to the device.

Absolute Maximum Ratings

Control voltage (V_1 or V_2)	-12V
Input power (peak or avg.)	+25dBm (100MHz-500MHz) +33dBm (500MHz-2GHz)
Storage temperature	-65°C to + 150°C
Channel temperature	+ 150°C
Chip thermal impedance	+ 120°C/W

Switch Control Functions

Control 1 (V_1)	Control 2 (V_2)	RF _{IN} →RF ₁	RF _{IN} →RF ₂ *
0V	-8V	Low Loss	Isolated
-8V	0V	Isolated	Low Loss

Control voltages V_1 and V_2 applied in complement.
* Applies to SPDT configurations only.

Notes for PCB Implementation

When using the T05 packaged FET switch in PCB applications, the following points must be observed in order to achieve the optimum performance:

1. Lead lengths should be minimised (<2mm)
2. The distance between the ground pins and RF ground should be minimised. Best results are achieved if the rim of the package is soldered to an RF ground plane around the complete circumference.
3. Control bias lines should be designed and positioned to minimise RF coupling between the RF input and output lines.

General Device Notes

1. The output in the isolated state for the P35-4210-0, P35-4210-1 and P35-4210-2 is reflective. The output of the P35-4210-3 is matched to 50ohms.
2. At the 1dB compression point, the control current is typically a few μA . At low frequencies, self detection can cause this current to increase typically to $150\mu A$. (Maximum specification to $0.5mA$.)
3. Consideration must be given to internal power dissipation when operating the device at high levels of incident RF power and high ambient temperature.
4. Isolation characteristics will degrade at incident power levels in excess of + 20dBm in the range 10MHz to 250MHz and + 25dBm when greater than 250MHz.
5. Recommended TTL compatible driver circuits are available on request.

Ordering Information

P35-4210-0 Chip
P35-4210-1 T05 Package SPDT
P35-4210-2 T05 Package SPST – Reflective
P35-4210-3 T05 Package SPST – Non-reflective
P35-4210-4 Surface Mount Package SPDT