

CMOS 4-BIT D-TYPE REGISTER

FEATURES

- ◆ 3-State Outputs with Gated Control Lines
- ◆ Fully Independent Clock
- ◆ Asynchronous Reset
- ◆ Fully Static Operation - DC to 12MHz @ 10Vdc

DESCRIPTION

The 4076B 4-bit Register consists of four D-Type flip-flops operating synchronously from a common Clock. OR-gated Output Disable inputs force the outputs into a high-impedance state for use in bus-organized systems. OR-gated Data Disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus, they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous Master Reset is provided to clear all four flip-flops simultaneously independent of the Clock or Disable inputs.

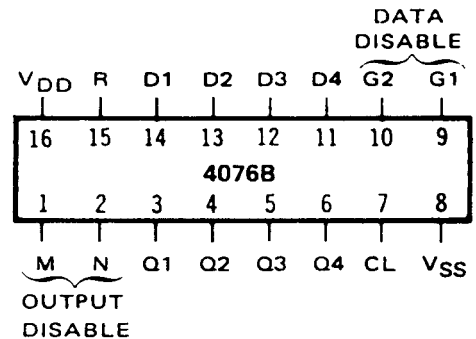
TRUTH TABLE

Reset	Clock	Data Input Disable		Data D	Next State Output Q	
		G1	G2			
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0		1	X	X	Q	NC
0		X	1	X	Q	NC
0		0	0	1	1	
0		0	0	0	0	
0	1	X	X	X	Q	NC
0		X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level X = Don't Care
0 ≡ Low Level NC = No Change

CONNECTION DIAGRAM (all packages)



Add suffix for package:

C 16-pin Cerdip

E 16-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

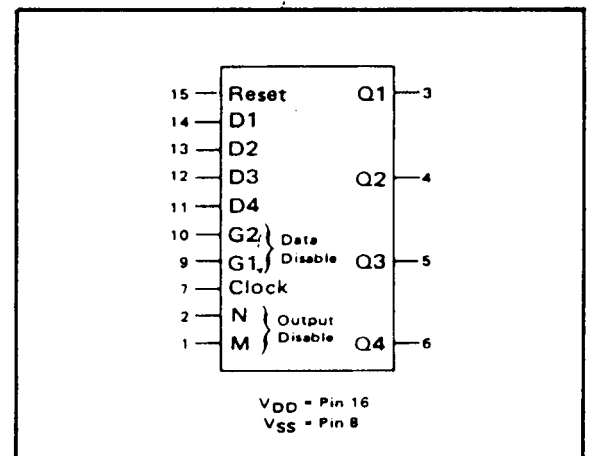
For maximum reliability:

DC Supply Voltage $V_{DD} - V_{SS}$ 3 to 15 Vdc

Operating Temperature T_A -55 to +125 °C

C -55 to +125 °C
E -40 to +85 °C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	5	—	5	—	0.05	5	—	150	μAdc
		10	—	10	—	0.1	10	—	300	
		15	—	20	—	0.2	20	—	600	
3-STATE OUTPUT LEAKAGE CURRENT	I _{ZL}	15	—	±0.1	—	±10 ⁻⁴	±0.1	—	±1.0	μAdc

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C

= -40°C for E

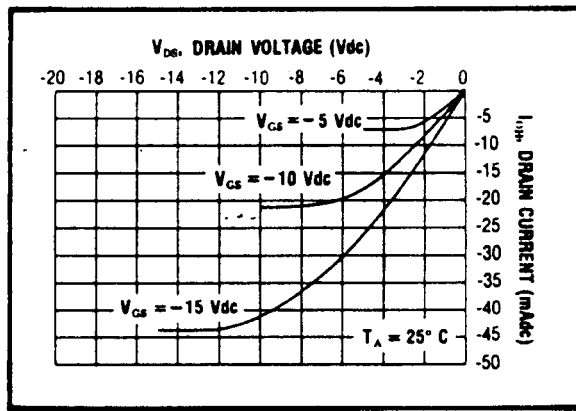
T_{HIGH} = +125°C for C

= + 85°C for E

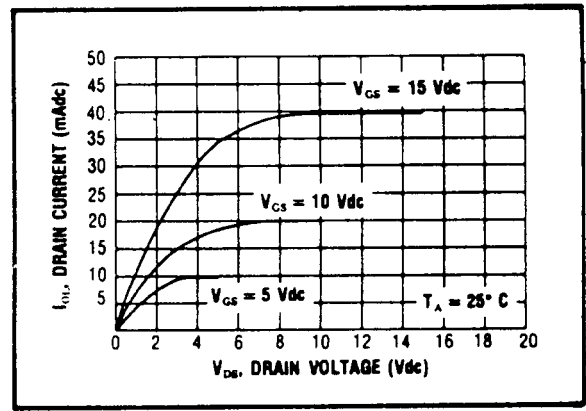
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (V _{dc})	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Q Output Disable to Q	t _{PLH} , t _{PHL}	5	—	150	300	ns
		10	—	70	140	
		15	—	45	90	
	t _{PHZ} , t _{PLZ}	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
	t _{PZH} , t _{PZL}	5	—	80	160	ns
		10	—	35	70	
		15	—	25	50	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
10	—	50	100			
15	—	40	80			
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	80	160	ns
		10	—	40	80	
		15	—	30	60	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	3.0	6.0	—	MHz
		10	6.0	12	—	
		15	8.0	16	—	
MAXIMUM CLOCK RISE & FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	15	—	—	
MINIMUM SETUP TIME Data Inputs Data Disable Inputs	t _{setup}	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
	t _{setup}	5	—	100	200	ns
		10	—	60	120	
		15	—	45	90	
MINIMUM HOLD TIME All Inputs	t _{hold}	5	—	75	150	ns
		10	—	35	70	
		15	—	30	60	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5	—	200	400	ns
		10	—	100	200	
		15	—	75	150	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	75	150	ns
		10	—	40	80	
		15	—	30	60	
RESET REMOVAL TIME	t _{rem}	5	—	100	200	ns
		10	—	60	120	
		15	—	45	90	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

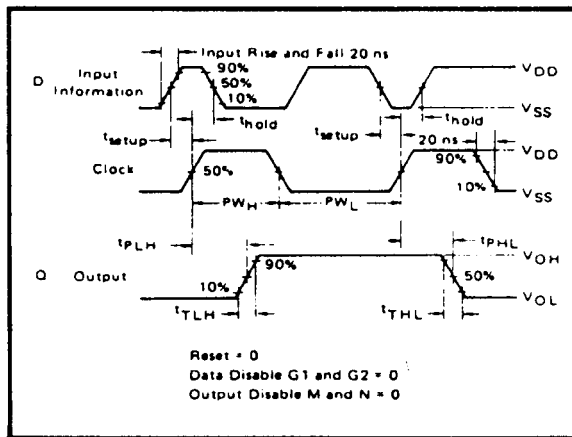


Typical P-Channel
Source Current Characteristics

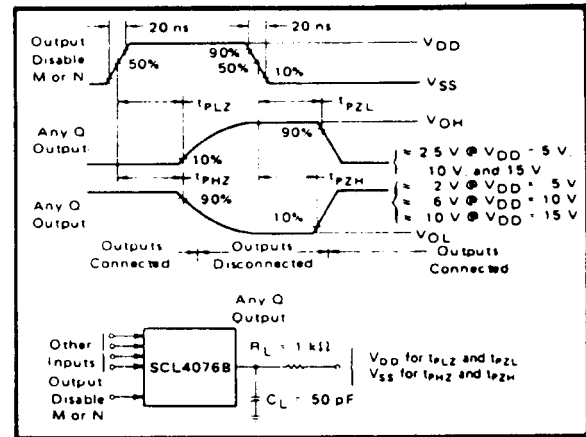


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



THREE-STATE PROPAGATION DELAY WAVESHAVE AND CIRCUIT



LOGIC DIAGRAM

