THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

JTSPC603e

PowerPC 603e™ MICROPROCESSOR DICE
PID6-603e Specification

DESCRIPTION

The PID6-603e implementation of PC603e (after named 603e) is a low-power implementation of reduced instruction set computer (RISC) microprocessors PowerPC™ family. The 603e implements 32-bit effective addresses, integer data types of 8, 16 and 32 bits, and floating-point data types of 32 and 64 bits.The 603e is a low-power 3.3-volt design and provides four software controllable power-saving modes.

The 603e is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance ; however, the 603e makes completion appear sequential. The 603e integrates five execution units and is able to execute five instructions in parallel.

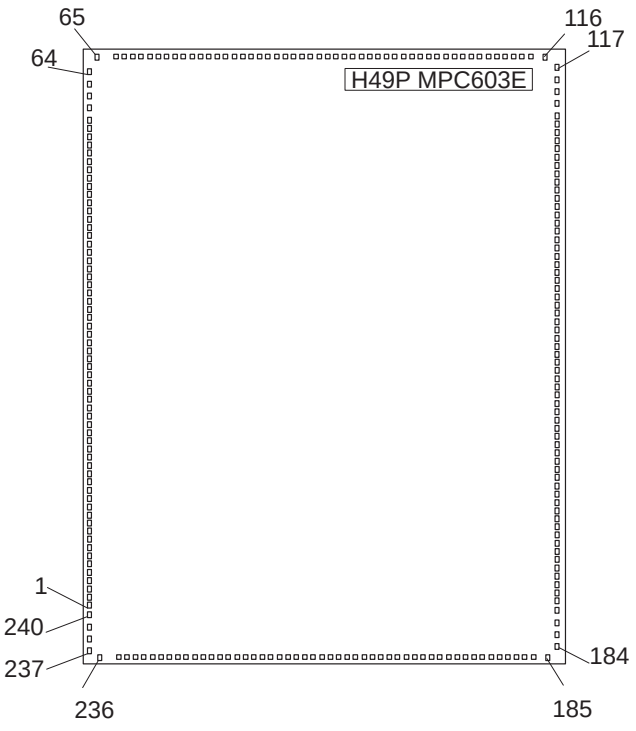
The 603e provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data and on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers that provide support for demand-paged virtual memory address translation and variable-sized block translation.

The 603e has a selectable 32 or 64-bit data bus and a 32-bit address bus. The 603e interface protocol allows multiple masters to complete for system resources through a central external arbiter. The 603e supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The 603e uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.The 603e integrates in system testability and debugging features through JTAG boundary-scan capability.

MECHANICAL DATA SPECIFICATION

Techno	HCMOS 0.5 µm
Mask	H49P
Pad size	0.1*0.1 mm
Die size	8.507 mm x 11.780 mm
Die thickness . .	0.630 mm
Metallization . . .	Naked Si (back side) Al (front side)
Passivation	6KÂ SI3N4 + 4KÂ SiO
Mask revision . .	4.1 (N suffix)



MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	-0.3	4.0	V
Input voltage	V_{in}	-0.3	5.5	V
Storage temperature range	T_{stg}	-55	+150	°C
Power dissipation	P_D		6.65	W
Operating temperature (junction)	T_j	-55	+130	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3 V ± 5 % ; GND = 0 V dc)

Characteristics		Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSCLK)		V_{IH}	2.0	5.5	V
Input low voltage (all inputs except SYSCLK)		V_{IL}	GND	0.8	V
SYSCLK input high voltage		CV_{IH}	2.4	5.5	V
SYSCLK input low voltage		CV_{IL}	GND	0.4	V
Input leakage current	V_{in} = 3.465 V	I_{in}	-	10	µA
	V_{in} = 5.5 V	I_{in}	-	245	µA
Hi-Z (off-state) leakage current	V_{in} = 3.465 V	I_{TSI}	-	10	µA
	V_{in} = 5.5 V	I_{TSI}	-	245	µA
Output high voltage	I_{OH} = –9 mA	V_{OH}	2.4	-	V
Output low voltage	I_{OL} = 14 mA	V_{OL}	-	0.4	V
Capacitance, V_{in} = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{in}	-	10.0	pF
Capacitance, V_{in} = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)		C_{in}	-	15.0	pF

AC ELECTRICAL CHARACTERISTICS -- Input AC specifications

Table 1 provides the input AC timing specifications for the 603e as defined in Figure 1 and Figure 2.

Table 1 : ***Input AC timing specifications***

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, –55°C ≤ T_J ≤ 125°C

Num	Characteristics	100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	4.0	-	4.0	-	4.0	-	ns	2
10b	All other inputs valid to SYSCLK (input setup)	5.0	-	5.0	-	5.0	-	ns	3
10c	Mode select inputs valid to HRESET (input setup) (for DRTRY, QACK and TLBISYNC)	8* t_{sys}	-	8* t_{sys}	-	8* t_{sys}	-	ns	4,5,6,7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	-	1.0	-	1.0	-	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	-	1.0	-	1.0	-	ns	3
11c	HRESET to mode select inputs invalid (input hold) (for DRTRY, QACK, and TLBISYNC)	0	-	0	-	0	-	ns	4, 6, 7

Notes:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin. See Figure 2.
2. Address/data/transfer attribute input signals are composed of the following: A0–A31, AP0–AP3, TT0–TT4, TC0–TC1, TBST, TSIZ0–TSIZ2, GBL, DH0–DH31, DL0–DL31, DP0–DP7.
3. All other input signals are compsed of the following: TS, ABB, DBB, ARTRY, BG, AACK, DBG, DBWO, TA, DRTRY, TEA, DBDIS, HRESET, SRESET, INT, SMI, MCP, TBEN, QACK, TLBISYNC.
4. The setup and hold time is with respect to the rising edge of HRESET. See Figure 2.
5. t_{SYS} is the period of the external clock (SYSCLK) in nanoseconds.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode only. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL relock time (100 μs) during the power-on reset sequence.

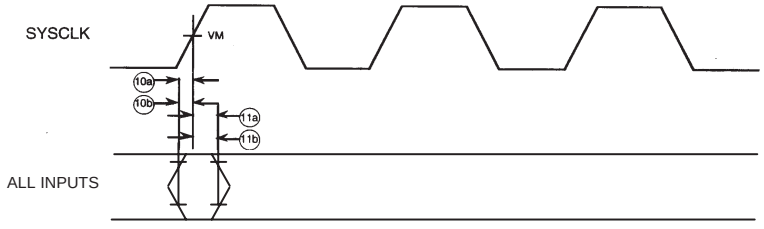


Figure 1 : ***Input timing diagram***

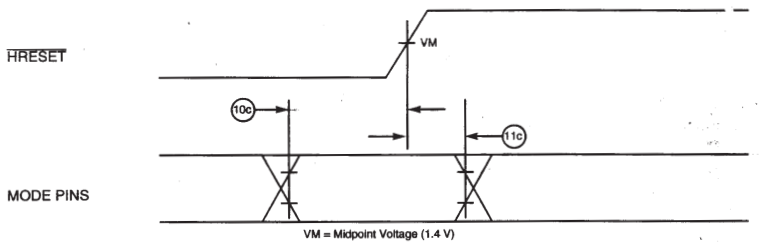


Figure 2 : ***Mode select input timing diagram***

AC ELECTRICAL CHARACTERISTICS -- Output AC specifications

Table 2 provides the output AC timing specifications for the 603e (shown in Figure 3).

Table 2 : ***Output AC timing specifications***

Vdd = 3.3 ± 5 % V dc, GND = 0 V dc, C_L = 50 pF, –55°C ≤ T_J ≤ 125°C

Num	Characteristic	100 MHz		120 MHz		133 MHz		Unit	Note
		Min	Max	Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	–	1.0	–	1.0	–	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V – $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	11.0	–	11.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	10.0	–	10.0	–	10.0	ns	6
14a	SYSCLK to output valid (5.5 V to 0.8 V – all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	13.0	–	13.0	–	13.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	–	11.0	–	11.0	–	11.0	ns	6
15	SYSCLK to output invalid (output hold)	0.5	–	0.5	–	0.5	–	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	–	9.5	–	9.5	–	9.5	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	–	1.2	–	1.2	–	1.2	t_{sys}	5, 7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	–	9.0	–	9.0	–	9.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * t_{sys} + 1.0	–	0.2 * t_{sys} + 1.0	–	0.2 * t_{sys} + 1.0	–	ns	3, 5, 8
20	Maximum dalay to $\overline{ARTRY}$ precharge	–	1.2	–	1.2	–	1.2	t_{sys}	5, 8
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	–	2.25	–	2.25	–	2.25	t_{sys}	5, 8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin. See.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).
5. t_{sys} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.

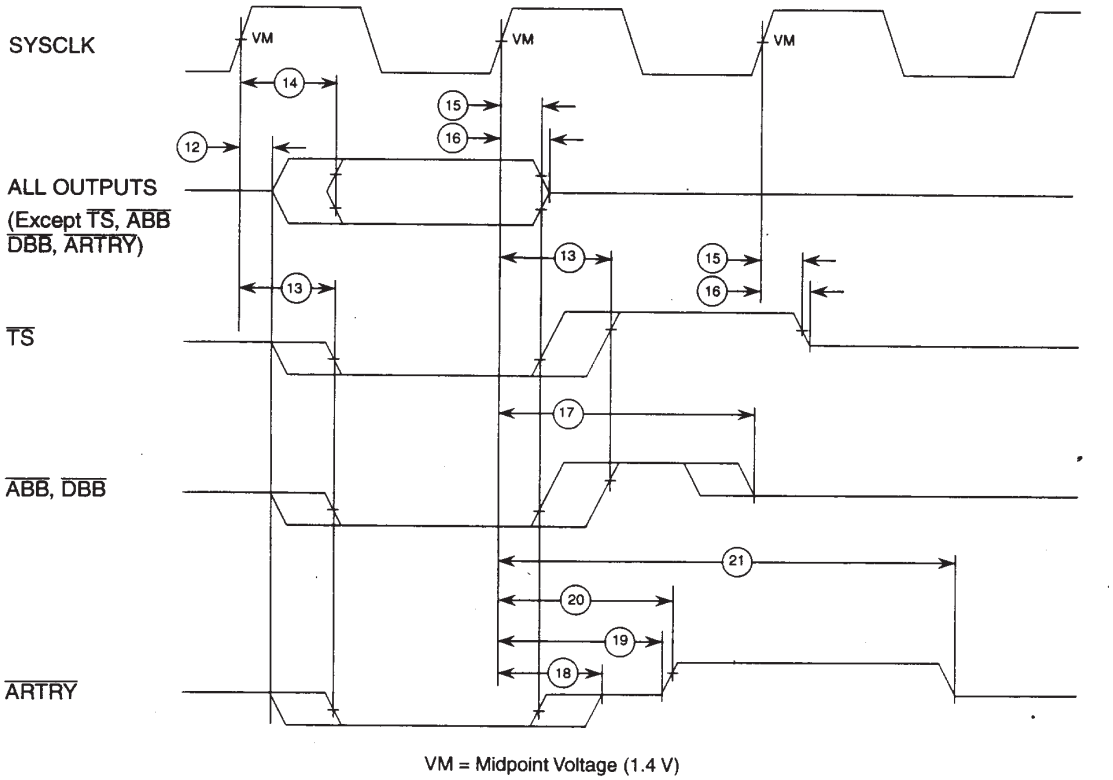


Figure 3 : ***Output timing diagram***

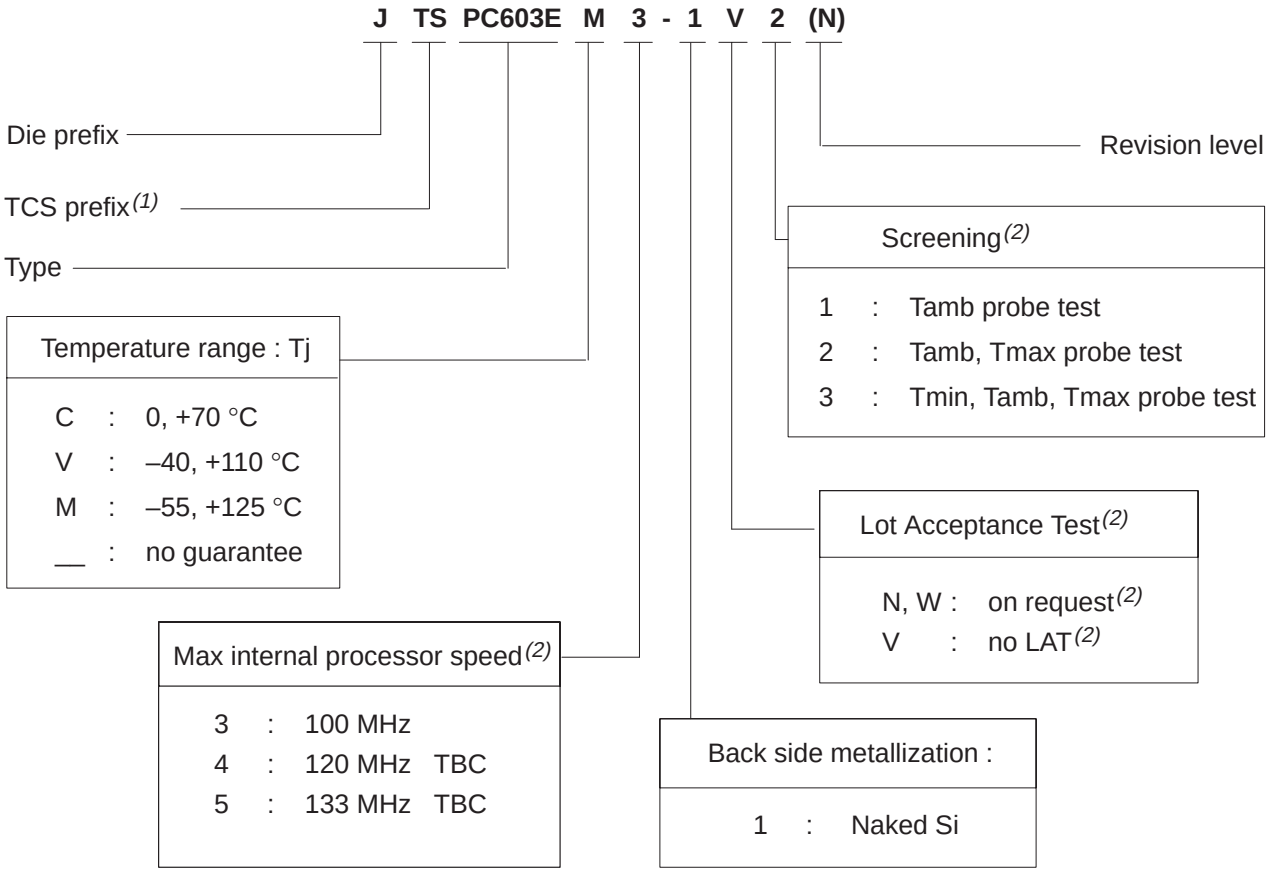
PAD LAYOUT

Here below are listed all the 240 pads and the name of relevant function. The pad numbers refer to the bounding diagram on page 1.

Die	Name	Die	Name	Die	Name	Die	Name	Die	Name
1	$\overline{GBL}$	49	GND	97	DH8	145	$\overline{DBB}$	193	OGND
2	A1	50	DP7	98	DH7	146	OGND	194	OVDD
3	A3	51	DL23	99	DH6	147	VDD	195	TSIZ2
4	VDD	52	DL24	100	DL22	148	OVDD	196	TSIZ1
5	A5	53	OGND	101	DL21	149	$\overline{TS}$	197	TSIZ0
6	A7	54	OVDD	102	DL20	150	CSE1	198	TDO
7	A9	55	DL25	103	OGND	151	A28	199	TDI
8	OGND	56	DL26	104	OVDD	152	GND	200	TMS
9	GND	57	DL27	105	DL19	153	$\overline{DBDIS}$	201	TCK
10	OVDD	58	DL28	106	DL18	154	$\overline{TEA}$	202	$\overline{TRST}$
11	A11	59	VDD	107	DL17	155	$\overline{TA}$	203	L2_TSTCLK
12	A13	60	OGND	108	DH5	156	$\overline{DRTRY}$	204	L1_TSTCLK
13	A15	61	OVDD	109	DH4	157	VDD	205	LSSD_MODE
14	VDD	62	DL29	110	DH3	158	A26	206	GND
15	A17	63	DL30	111	OGND	159	A24	207	VDD
16	A19	64	DL31	112	OVDD	160	A22	208	PLL_CFG3
17	A21	65	GND	113	DH2	161	OGND	209	AVDD
18	OGND	66	DH31	114	DH1	162	GND	210	PLL_CFG2
19	GND	67	DH30	115	DH0	163	OVDD	211	PLL_CFG1
20	OVDD	68	DH29	116	GND	164	A20	212	SYSCLK
21	A23	69	OGND	117	DL16	165	A18	213	PLL_CFG0
22	A25	70	OVDD	118	DL15	166	A16	214	$\overline{HRESET}$
23	A27	71	DH28	119	DL14	167	VDD	215	$\overline{CKSTP\_IN}$
24	VDD	72	DH27	120	OGND	168	A14	216	$\overline{CKSTP\_OUT}$
25	$\overline{DBWO}$	73	DH26	121	OVDD	169	A12	217	$\overline{DPE}$
26	$\overline{DBG}$	74	DH25	122	VDD	170	A10	218	$\overline{APE}$
27	$\overline{BG}$	75	DH24	123	DL13	171	OGND	219	$\overline{BR}$
28	$\overline{AACK}$	76	DH23	124	DL12	172	GND	220	OGND
29	GND	77	OGND	125	DL11	173	OVDD	221	CLK_OUT
30	A29	78	DH22	126	DL10	174	A8	222	OVDD
31	$\overline{QREQ}$	79	OVDD	127	OGND	175	A6	223	TC1
32	$\overline{ARTRY}$	80	DH21	128	OVDD	176	A4	224	TC0
33	OGND	81	DH20	129	DL9	177	VDD	225	CSE0
34	VDD	82	DH19	130	DL8	178	A2	226	AP3
35	OVDD	83	DH18	131	DL7	179	A0	227	AP2
36	$\overline{ABB}$	84	DH17	132	GND	180	TT4	228	OGND
37	A31	85	DH16	133	DL6	181	OGND	229	OVDD
38	DP0	86	OGND	134	DL5	182	GND	230	AP1
39	GND	87	DH15	135	DL4	183	OVDD	231	AP0
40	DP1	88	OVDD	136	OGND	184	TT3	232	$\overline{RSRV}$
41	DP2	89	DH14	137	VDD	185	TT2	233	$\overline{TLBISYNC}$
42	DP3	90	DH13	138	OVDD	186	$\overline{MCP}$	234	TBEN
43	OGND	91	DH12	139	DL3	187	$\overline{SMI}$	235	$\overline{QACK}$
44	VDD	92	DH11	140	DL2	188	$\overline{INT}$	236	$\overline{WT}$
45	OVDD	93	DH10	141	DL1	189	$\overline{SRESET}$	237	$\overline{CI}$
46	DP4	94	DH9	142	GND	190	TT1	238	OGND
47	DP5	95	OGND	143	DL0	191	TT0	239	GND
48	DP6	96	OVDD	144	A30	192	$\overline{TBST}$	240	OVDD

OVDD: output drivers VDD VDD: internal logic VDD AVDD:PLL VDD
OGND: output driver GND GND: internal logic GND

ORDERING INFORMATION



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