16. ELECTRICAL SPECIFICATIONS

Applied masks

The electrical characteristics shown below are applied to devices other than the old models conforming to E and P masks.

For the electrical characteristics of the E and P masks, consult NEC.

"Others" in the table below means products conforming to the masks other than E, P, M and N.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V ±10%	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K		−0.5 to V_{DD}+1.0	V
Output voltage	V_O		−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A	M, N masks	−10 to +70	°C
		Others	−40 to +85	
Storage temperature	T_{stg}		−65 to +150	°C

OPERATING RANGE

Product Name	Mask	T_A	V_{DD}
μPD70208, 70216-8	M, N	−10 to + 70 °C	5 V ± 10%
	Others	−40 to + 85 °C	
μPD70208, 70216-10	M, N	−10 to + 70 °C	5 V ± 5%
	Others	−40 to + 85 °C	5 V ± 10%
μPD70208, 70216 (A) -8	−	−40 to + 85 °C	5 V ± 10%
μPD70208, 70216 (A) -10	−	−40 to + 85 °C	5 V ± 10%

Cautions 1. Do not directly connect the output pins of two or more IC products and do not directly connect the output pins to V_{DD} or Vcc and GND. However, open-drain pins or open-collector pins may be connected directly. Moreover, an external circuit whose timing is designed to avoid output collision can be connected to pins that go into a high-impedance state.

2. If even one of the above parameters exceeds the absolute maximum rating even momentarily, the quality of the program may be degraded. Absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Use the program keeping all the parameters within these rated values.

The masks and conditions shown in DC and AC Characteristics below specify the range within which the normal operation of the product is guaranteed.

DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}			2.2		V_{DD}+0.3	V
Input voltage low	V_{IL}			−0.5		+0.8	V
Clock input voltage high	V_{KH}			3.9		V_{DD}+1.0	V
Clock input voltage low	V_{KL}			−0.5		0.6	V
Output voltage high	V_{OH}	I_{OH} = −400 μA		0.7V_{DD}			V
Output voltage low	V_{OL}	I_{OL} = 2.5 mA				0.4	V
Input leak current high	I_{LIH}	V_I = V_{DD}				10	μA
Input leak current low	I_{LIL}	Except INTP : V_I = 0 V				−10	μA
INTP input current low	I_{LIPL}	INTP input : V_I = 0 V				−300	μA
Output leak current high	I_{LOH}	V_O = V_{DD}				10	μA
Output leak current low	I_{LOL}	V_O = 0 V				−10	μA
Supply current	I_{DD}	During operation	70208, 70216-8		70	90	mA
			70208, 70216-10		90	120	mA
		On standby	70208, 70216-8		10	20	mA
			70208, 70216-10		15	25	mA

Remark The supply voltage during operation is almost propotional to the operating clock frequency.

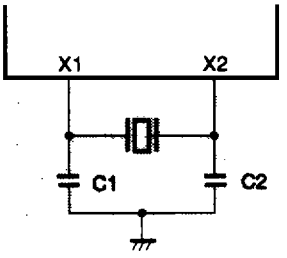
CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			15	pF
Input/output capacitance	C_{IO}	0 V other than test pin.			15	pF

★ **RECOMMENDED OSCILLATION CIRCUIT**

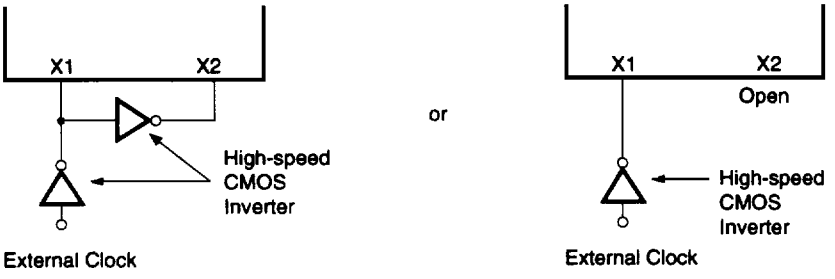
The clock input circuits (1) and (2) shown below are recommended.

(1) Oscillator connection



Cautions
1. **The oscillation circuit should be as close as possible to the X1 and X2 pins.**
2. **No other signal lines should pass through the shaded area.**
3. **V40, V50 and resonator matching requires careful evaluation.**
4. **The values of oscillation circuit constants C1 and C2 vary depending on the characteristics of the oscillator used. Evaluate these constants with the oscillator actually used.**

(2) External clock input



Caution The high-speed CMOS inverter should be as close as possible to the X1 and X2 pins.

AC CHARACTERISTICS

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208-8 μPD70216-8		μPD70208-10 μPD70216-10		Unit
			MIN.	MAX.	MIN.	MAX.	
External clock input cycle	①	t_{CYX}	62	250	50	250	ns
External clock input high-level width (V_{KH}=3.0 V)	②	t_{XXH}	20		19		ns
External clock input low-level width (V_{KL}=1.5 V)	③	t_{XXL}	20		19		ns
External clock input rise time (1.5→3.0 V)	④	t_{XR}		10		5	ns
External clock input fall time (3.0→1.5 V)	⑤	t_{XF}		10		5	ns
Clock output cycle	⑥	t_{CYK}	124	500	100	500	ns
Clock output high-level width (V_{OH}=3.0 V)	⑦	t_{KKH}	0.5t_{CYK}–7		0.5t_{CYK}–5		ns
Clock output low-level width (V_{OL}=1.5 V)	⑧	t_{KKL}	0.5t_{CYK}–7		0.5t_{CYK}–5		ns
Clock output rise time (1.5→3.0 V)	⑨	t_{KR}		7		5	ns
Clock output fall time (3.0→1.5 V)	⑩	t_{KF}		7		5	ns
CLKOUT delay time (vs. external clock)	⑪	t_{DXK}		55		40	ns
Input rise time (except external clock) (0.8→2.2 V)	⑫	t_{IR}		20		15	ns
Input fall time (except external clock) (2.2→0.8 V)	⑬	t_{IF}		12		10	ns
Output rise time(except CLKOUT) (0.8→2.2 V)	⑭	t_{OR}		20		15	ns
Output fall time (except CLKOUT) (2.2→0.8 V)	⑮	t_{OF}		12		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)[Note 1]	⑯	t_{SRESK}	25		20		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)[Note 1]	⑰	t_{HKRES}	35		25		ns
RESOUT output delay time (vs. CLKOUT↓)	⑱	t_{DKRES}	5	60	5	50	ns
READY inactive setup time (vs. CLKOUT↑)	⑲	t_{SRYLK}	15		15		ns
READY inactive hold time (vs. CLKOUT↑)	⑳	t_{HKRYL}	25		20		ns
READY active setup time (vs. CLKOUT↑)	㉑	t_{SRYHK}	15		15		ns
READY active hold time (vs. CLKOUT↑)	㉒	t_{HKRYH}	25		20		ns
NMI setup time (vs. CLKOUT↑)	㉓	t_{SNMIK}	15		15		ns
POLL setup time (vs. CLKOUT↑)	㉔	t_{SPOLK}	20		20		ns
Data setup time (vs. CLKOUT↓)	㉕	t_{SDK}	15		15		ns
Data hold time (vs. CLKOUT↓)	㉖	t_{HKD}	10		10		ns
CLKOUT → address delay time[Note 2]	㉗	t_{DKA}	10	55	10	50	ns
CLKOUT → address hold time	㉘	t_{HKA}	10		10		ns
CLKOUT↓ → PS delay time	㉙	t_{DKP}	10	60	10	50	ns
CLKOUT↓ → PS float delay time	㉚	t_{FKP}	10	60	10	50	ns
Address setup time (vs. ASTB↓)	㉛	t_{SAST}	t_{KKL}–30		t_{KKL}–20		ns
CLKOUT↓ → address float delay time[Note 3]	㉜	t_{FKA}	t_{HKA}	60	t_{HKA}	50	ns
CLKOUT↓ → ASTB↑ delay time	㉝	t_{DKSTH}		45		40	ns

Notes 1. When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

2. Specification to also support QS0, QS1, and BUSLOCK signals; and A16/PS0 through A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, and BS0 through BS2 signals in HLDRQ/HLDAK timing.

3. Specification to also support A16/PS0 through A19/PS3, $\overline{\text{UBE}}$, $\overline{\text{BUFEN}}$, BUF$\overline{\text{R}}$/W, $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$, BS0 through BS2 signals in HLDRQ/HLDAK timing.

AC CHARACTERISTICS (cont'd)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208-8 μPD70216-8		μPD70208-10 μPD70216-10		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT↑ → ASTB↓ delay time		㉞	t_{DKSTL}		50		45	ns
ASTB high-level width		㉟	t_{STST}	t_{KKL}–10		t_{KKL}–10		ns
ASTB↓ → address hold time		㊱	t_{HSTA}	t_{KKH}–20		t_{KKH}–20		ns
CLKOUT → control 1[Note 1] delay time		㊲	t_{DKCT1}	10	70	10	60	ns
CLKOUT → control 2[Note 2] delay time		㊳	t_{DKCT2}	10	60	10	55	ns
Address float → $\overline{RD}$↓ delay time		㊴	t_{DAFRL}	0		0		ns
CLKOUT↓ → $\overline{RD}$↓ delay time		㊵	t_{DKRL}	10	75	10	65	ns
CLKOUT↓ → $\overline{RD}$↑ delay time		㊶	t_{DKRH}	10	70	10	60	ns
$\overline{RD}$↑ → address delay time		㊷	t_{DRHA}	t_{CYK}–50		t_{CYK}–40		ns
$\overline{RD}$ low-level width		㊸	t_{RR}	2t_{CYK}–50		2t_{CYK}–40		ns
$\overline{BUFEN}$↑ → BUF$\overline{R}$/W delay time (read cycle)		㊹	t_{DBECT}	t_{KKL}–20		t_{KKL}–20		ns
CLKOUT↓ → data output delay time		㊺	t_{DKD}	10	60	10	55	ns
CLKOUT↓ → data float delay time		㊻	t_{FKD}	10	60	10	55	ns
$\overline{WR}$ low-level width		㊼	t_{WW}	2t_{CYK}–40		2t_{CYK}–40		ns
$\overline{WR}$↑ → $\overline{BUFEN}$↑ or BUF$\overline{R}$/W↓ (write cycle)		㊽	t_{DWCT}	t_{KKL}–20		t_{KKL}–20		ns
CLKOUT↑ → BS↓ delay time		㊾	t_{DKBL}	10	60	10	55	ns
CLKOUT↓ → BS↑ delay time		㊿	t_{DKBH}	10	60	10	55	ns
HLDRQ setup time (vs. CLKOUT↓)		(51)	t_{SHQK}	20		15		ns
CLKOUT↓ → HLDAK delay time		(52)	t_{DKHA}	10	70	10	60	ns
CLKOUT↑ → $\overline{DMAAK}$ delay time		(53)	t_{DKHDA}	10	60	10	55	ns
CLKOUT↓ → $\overline{DMAAK}$ delay time (cascade mode)		(54)	t_{DKLDA}	10	90	10	80	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA expansion write	(55)	t_{WW1}	2t_{CYK}–40		2t_{CYK}–40		ns
	DMA normal write	(56)	t_{WW2}	t_{CYK}–40		t_{CYK}–40		ns
$\overline{RD}$↓, $\overline{WR}$↓ delay time (vs. $\overline{DMAAK}$↓)		(57)	t_{DDARW}	t_{KKH}–30		t_{KKH}–30		ns
$\overline{DMAAK}$↑ delay time (vs. $\overline{RD}$↑)		(58)	t_{DRHDAH}	t_{KKL}–30		t_{KKL}–30		ns
$\overline{RD}$↑ delay time (vs. $\overline{WR}$↑)		(59)	t_{DWHRH}	5		5		ns
$\overline{TC}$ output delay time (vs. CLKOUT↑)		(60)	t_{DKTCL}		60		55	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT↑)		(61)	t_{DKTCF}		60		55	ns
$\overline{TC}$ low-level width		(62)	t_{TCTCL}	t_{CYK}–15		t_{CYK}–15		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT↑)		(63)	t_{DKTCH}		**Note 3**		**Note 3**	ns
$\overline{END}$ setup time (vs. CLKOUT↑)		(64)	t_{SEDK}	35		30		ns
$\overline{END}$ low-level width		(65)	t_{EDEDL}	100		80		ns
DMARQ setup time (vs. CLKOUT↑)		(66)	t_{SDQK}	35		30		ns
INTPn low-level width		(67)	t_{IPIPL}	100		80		ns
RxD setup time (vs. SCU internal clock↓)		(68)	t_{SRX}	1000		500		ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$, $\overline{REFRQ}$ and CPU cycles.

3. $t_{KKH}+t_{CYK}$ – 10 (Reference value when a 1.1-kΩ pull-up resistor is connected.)

AC CHARACTERISTICS (cont'd)

Output Pin Load Capacitance: C_L = 100 pF

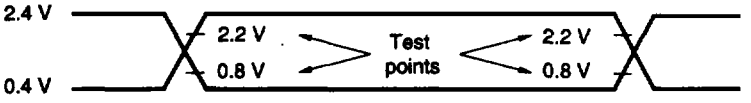
Parameter	Symbol		μPD70208-8 μPD70216-8		μPD70208-10 μPD70216-10		Unit
			MIN.	MAX.	MIN.	MAX.	
RxD hold time (vs. SCU internal clock↓)	⑲	t_{HRX}	1000		500		ns
CLKOUT↓ → $\overline{SRDY}$ delay time	⑳	t_{DKSR}		150		100	ns
TOUT1↓ → TxD delay time	㉑	t_{DTX}		500		200	ns
TCTL2 setup time (vs. CLKOUT↓)	㉒	t_{SGK}	50		40		ns
TCTL2 setup time (vs. TCLK↑)	㉓	t_{SGTK}	50		40		ns
TCTL2 hold time (vs. CLKOUT↓)	㉔	t_{HKG}	100		80		ns
TCTL2 hold time (vs. TCLK↑)	㉕	t_{HTKG}	50		40		ns
TCTL2 high-level width	㉖	t_{GGH}	50		40		ns
TCTL2 low-level width	㉗	t_{GGL}	50		40		ns
TOUT output delay time (vs. CLKOUT↓)	㉘	t_{DKTO}		200		150	ns
TOUT output delay time (vs. TCLK↓)	㉙	t_{DTKTO}		150		100	ns
TOUT output delay time (vs. TCTL2↓)	㉚	t_{DGTO}		120		90	ns
TCLK rise time	㉛	t_{TKR}		25		25	ns
TCLK fall time	㉜	t_{TKF}		25		25	ns
TCLK high-level width	㉝	t_{TKTKH}	50		45		ns
TCLK low-level width	㉞	t_{TKTKL}	50		45		ns
TCLK cycle	㉟	t_{CYTK}	124	DC	100	DC	ns
Access interval[Note 1]	㊱	t_{AI}	$2t_{CYK}$–50		$2t_{CYK}$–40		ns
$\overline{REFRQ}$↑ delay time (vs. $\overline{MRD}$↑)[Note 2]	㊲	t_{DRQHRH}	t_{KKL}–30		t_{KKL}–30		ns
$\overline{RESET}$ pulse width[Note 3]	㊳	t_{WRESL}	$4t_{CYK}$		$4t_{CYK}$		ns

Notes 1. Specification to guarantee read/write recovery time for I/O device.

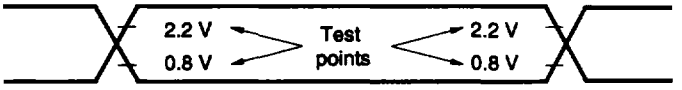
2. Specification to guarantee that $\overline{REFRQ}$↑ is always later than $\overline{MRD}$↑.

3. The oscillation stabilization time must be added on the power-ON reset when the oscillator is connected to the X1, X2 pins, and the internal clock generator is used. ★
Because the oscillation stabilization time varies depending on the characteristics of the oscillator and oscillation circuit used, evaluate the oscillation stabilization time with the oscillator and oscillation circuit actually used.

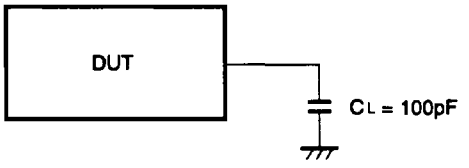
AC Test Input Waveform (Except X1 and X2)



AC Test Output Test Points

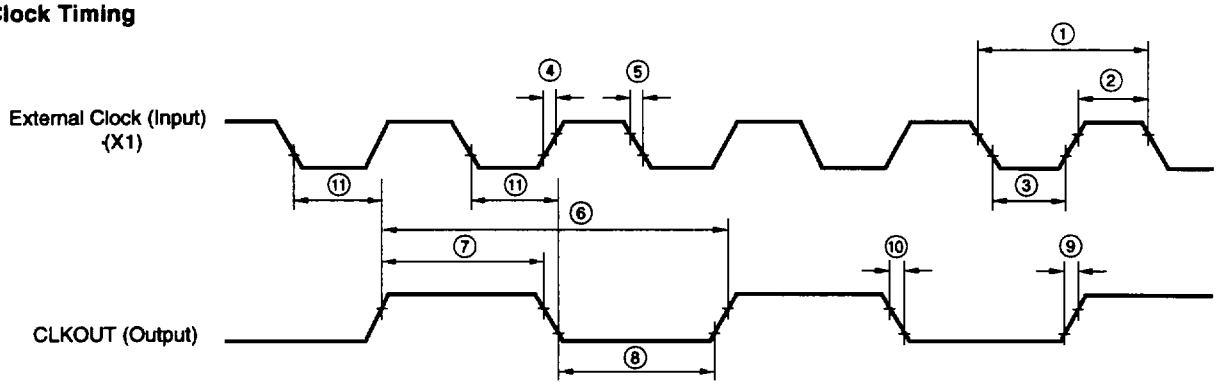


Load Conditions

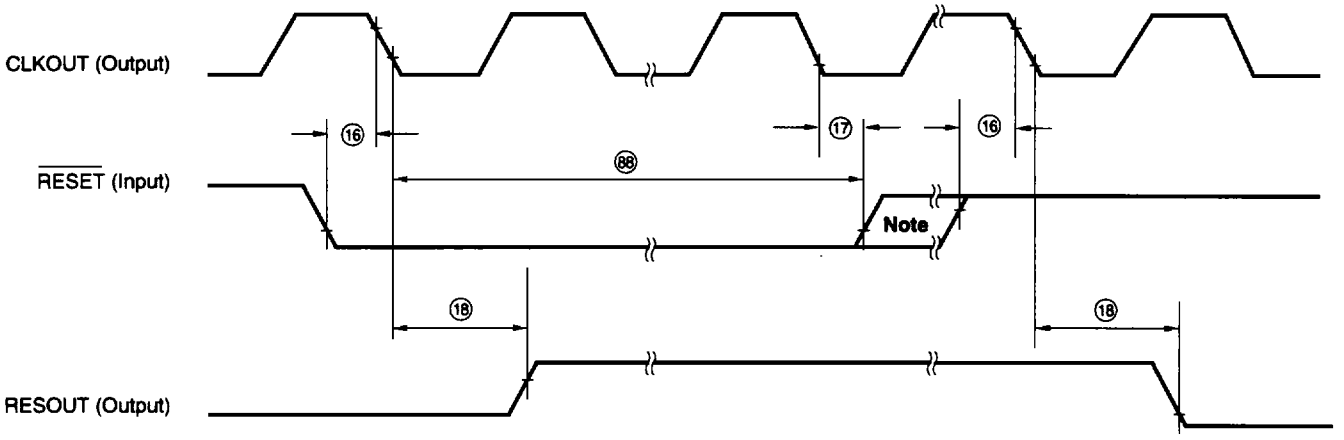


Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

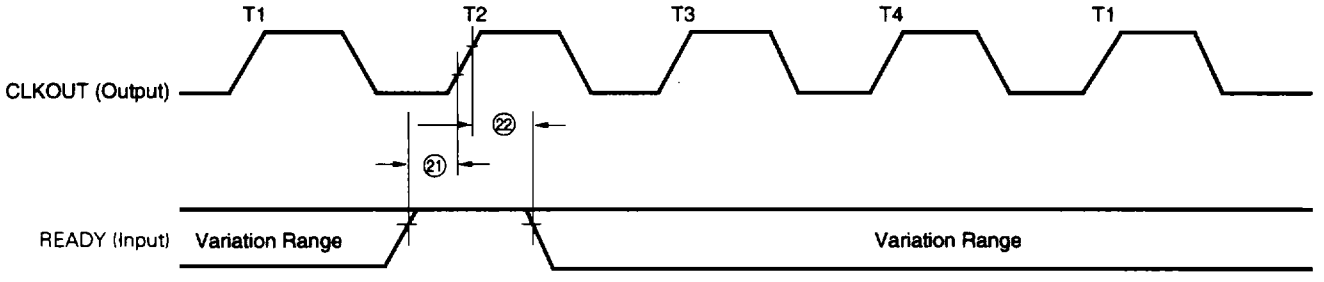
Clock Timing



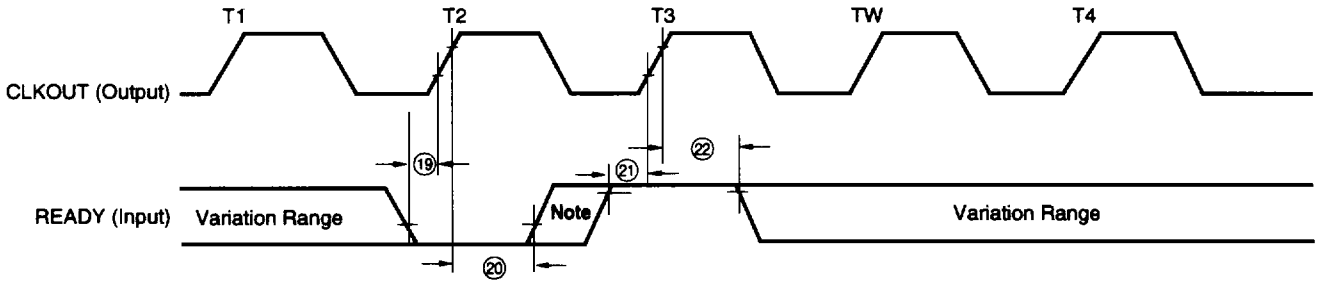
Reset Timing



Ready Timing (1)

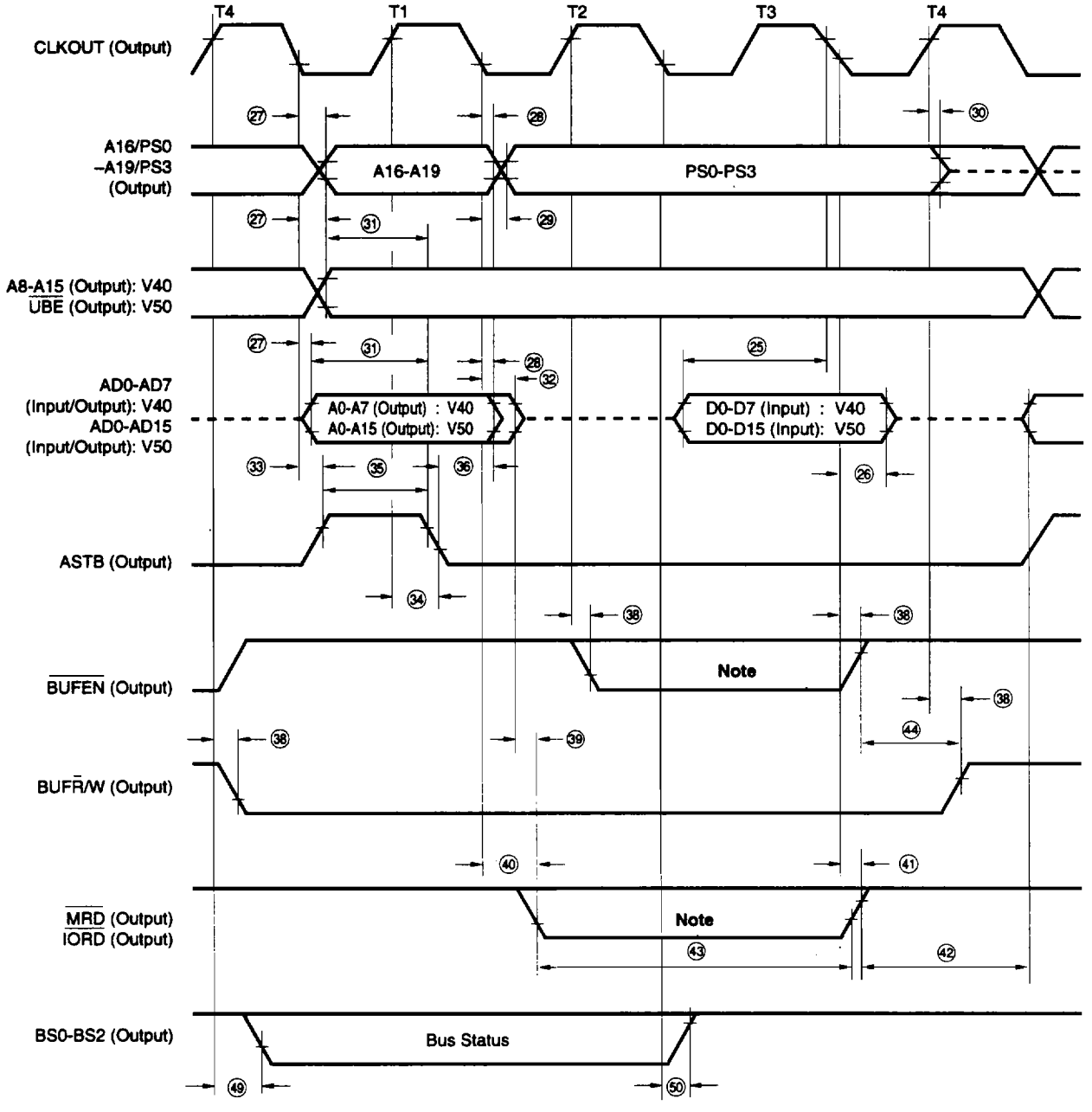


Ready Timing (2)



Note Variation range

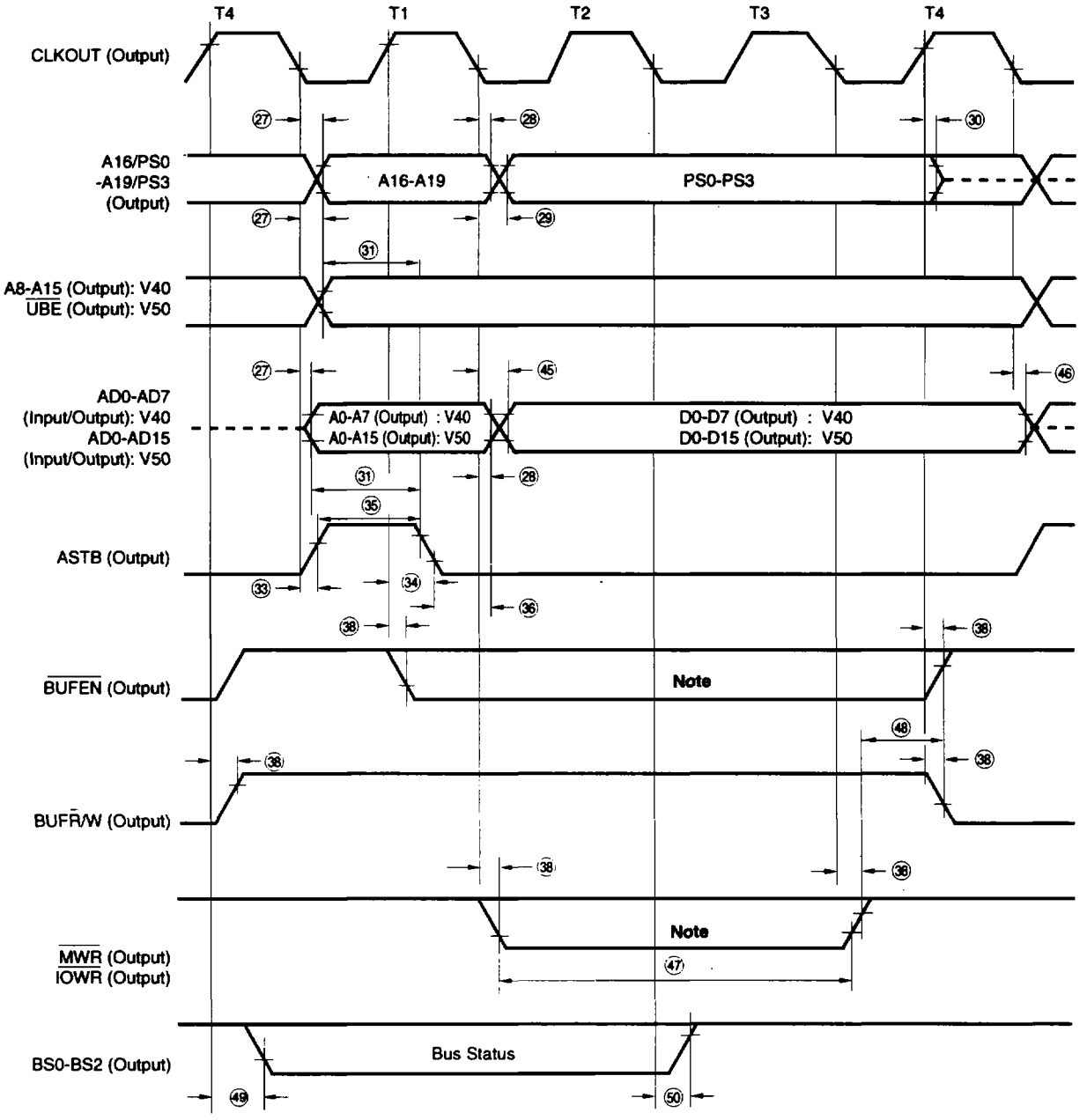
Read Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

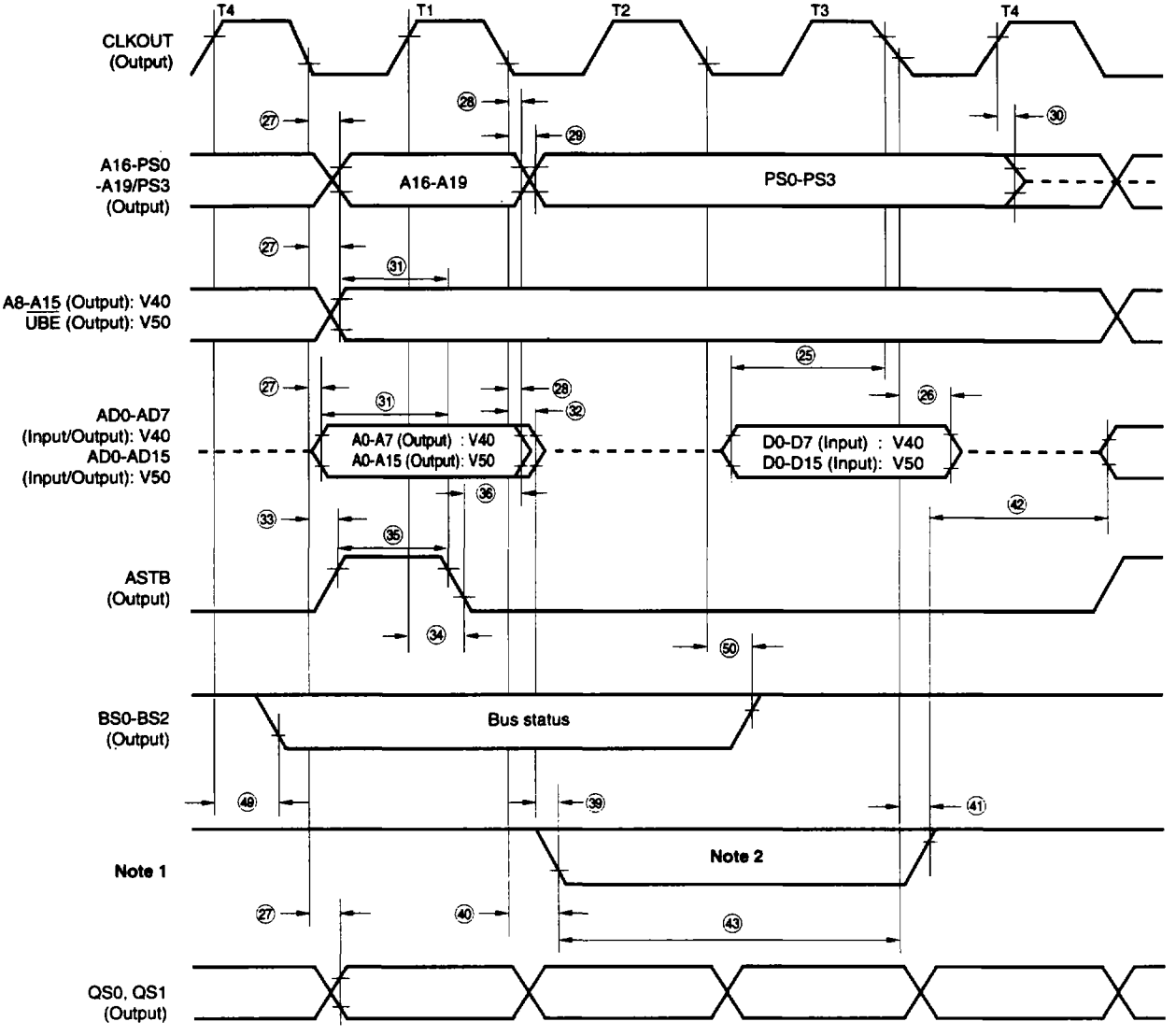
Write Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Status Timing

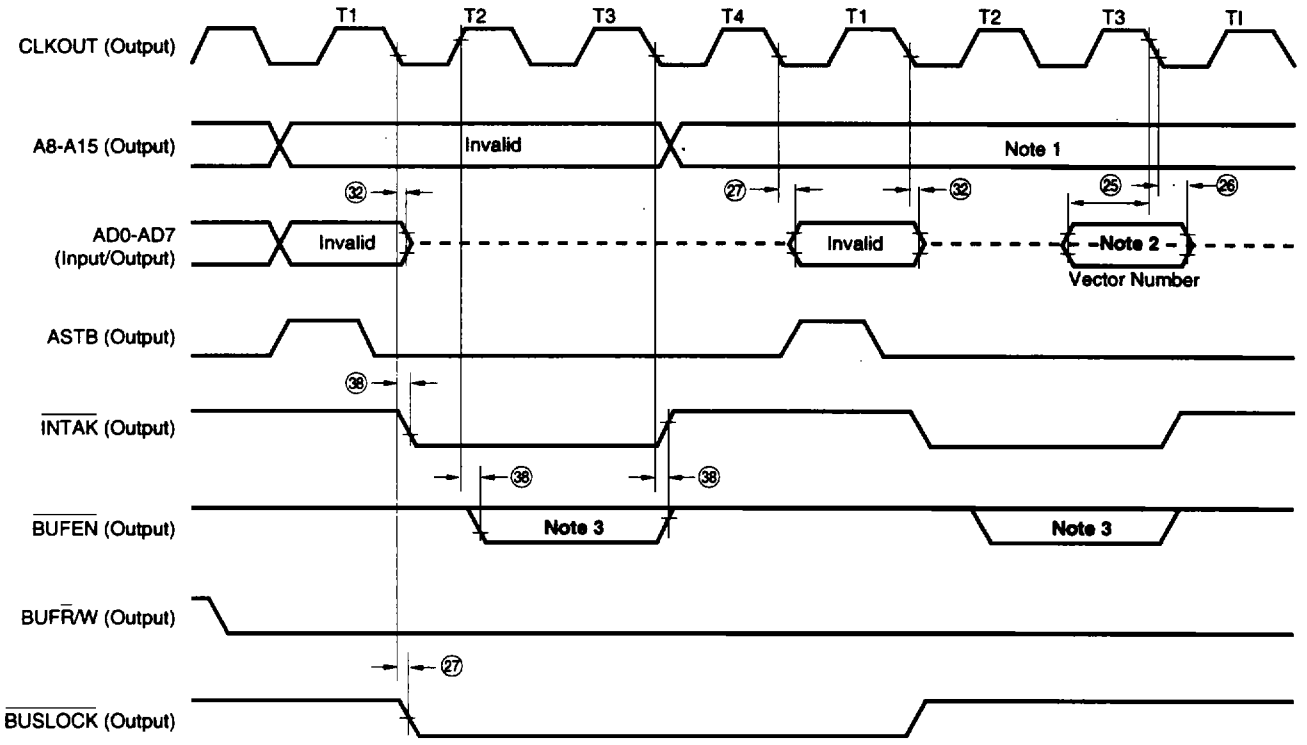


Notes 1. $\overline{\text{MRD}}$, $\overline{\text{IORD}}$, $\overline{\text{MWR}}$, $\overline{\text{IOWR}}$ (all output)

2. High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V40)



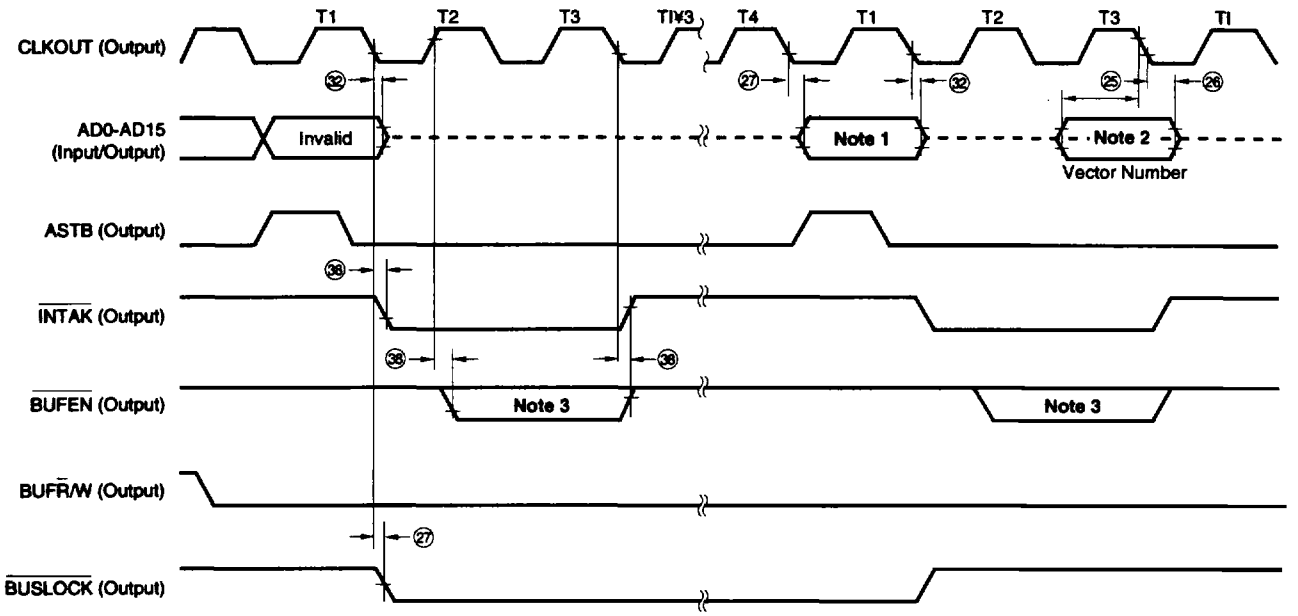
Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.

3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V50)



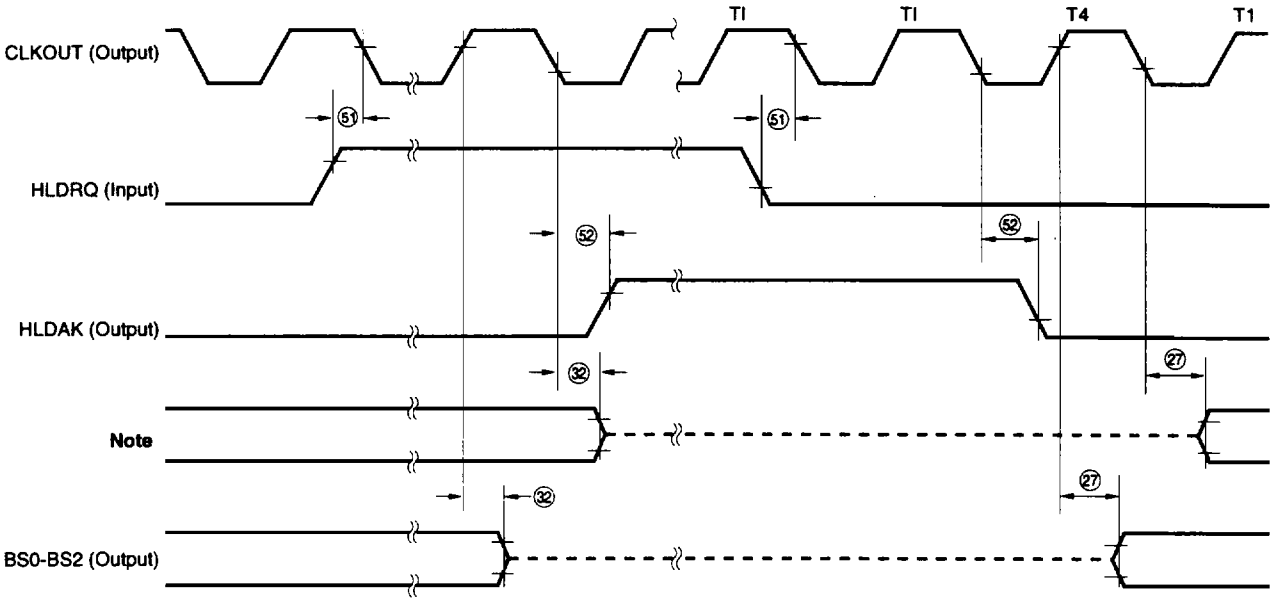
Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.

3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

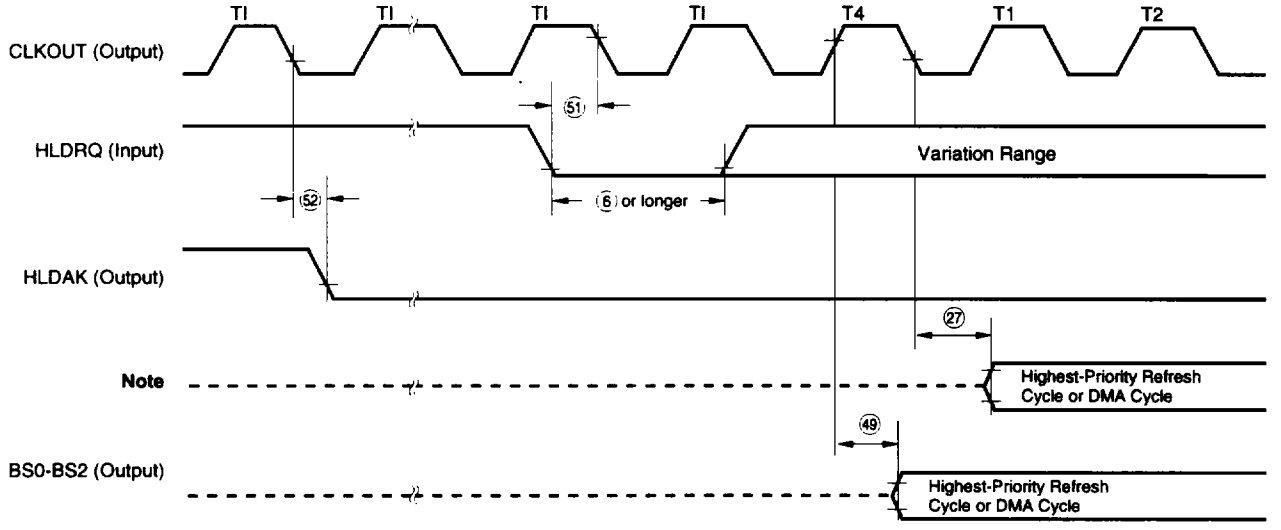
HLDRQ/HLDAK Timing (1)



Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUFR/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40, V50
A8-A15 (output), AD0-AD7 (input/output): V40 AD0-AD15 (input/output) V50

Remark A dashed line indicates high impedance.

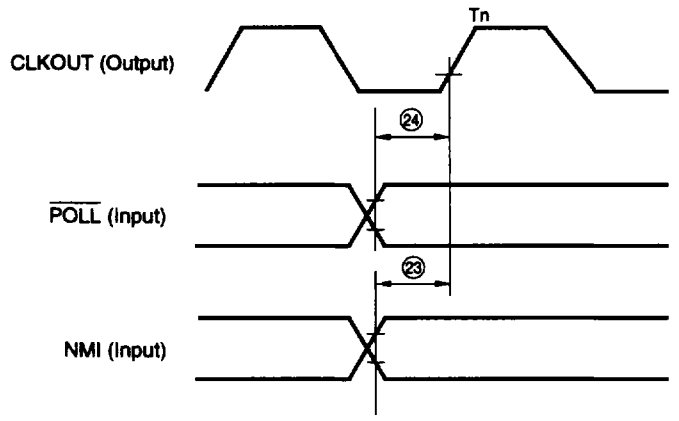
HLDRQ/HLDAK Timing (2)



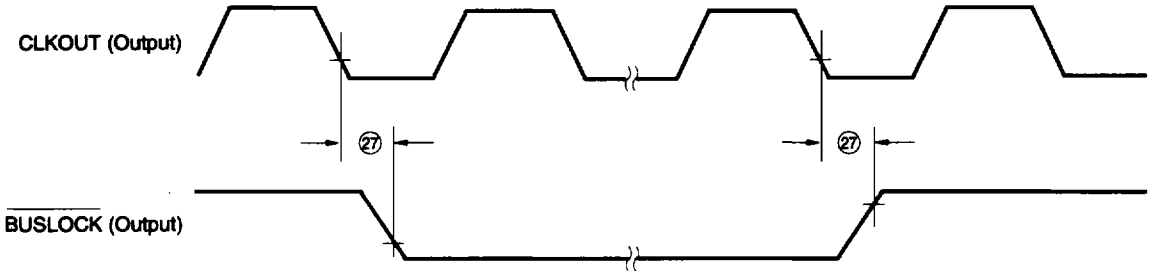
Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUFR/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40, V50
A8-A15 (output), V40 AD0-AD7 (input/output): V40 AD0-AD15 (input/output) V50

Remark A dashed line indicates high impedance.

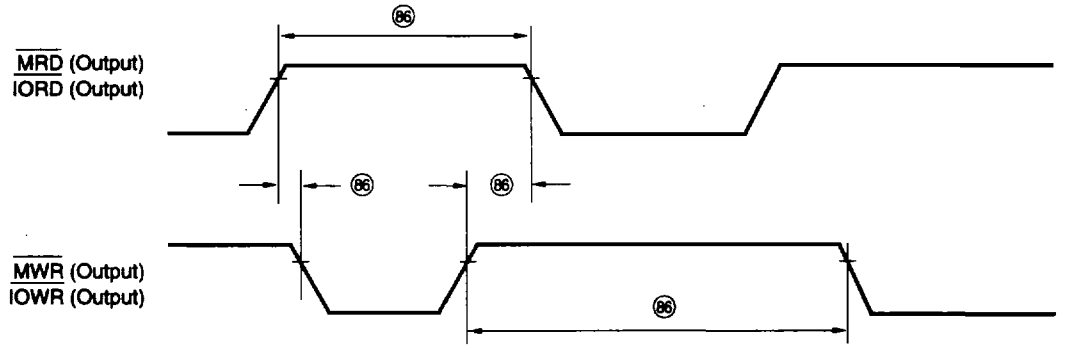
$\overline{\text{POLL}}$, NMI Input Timing



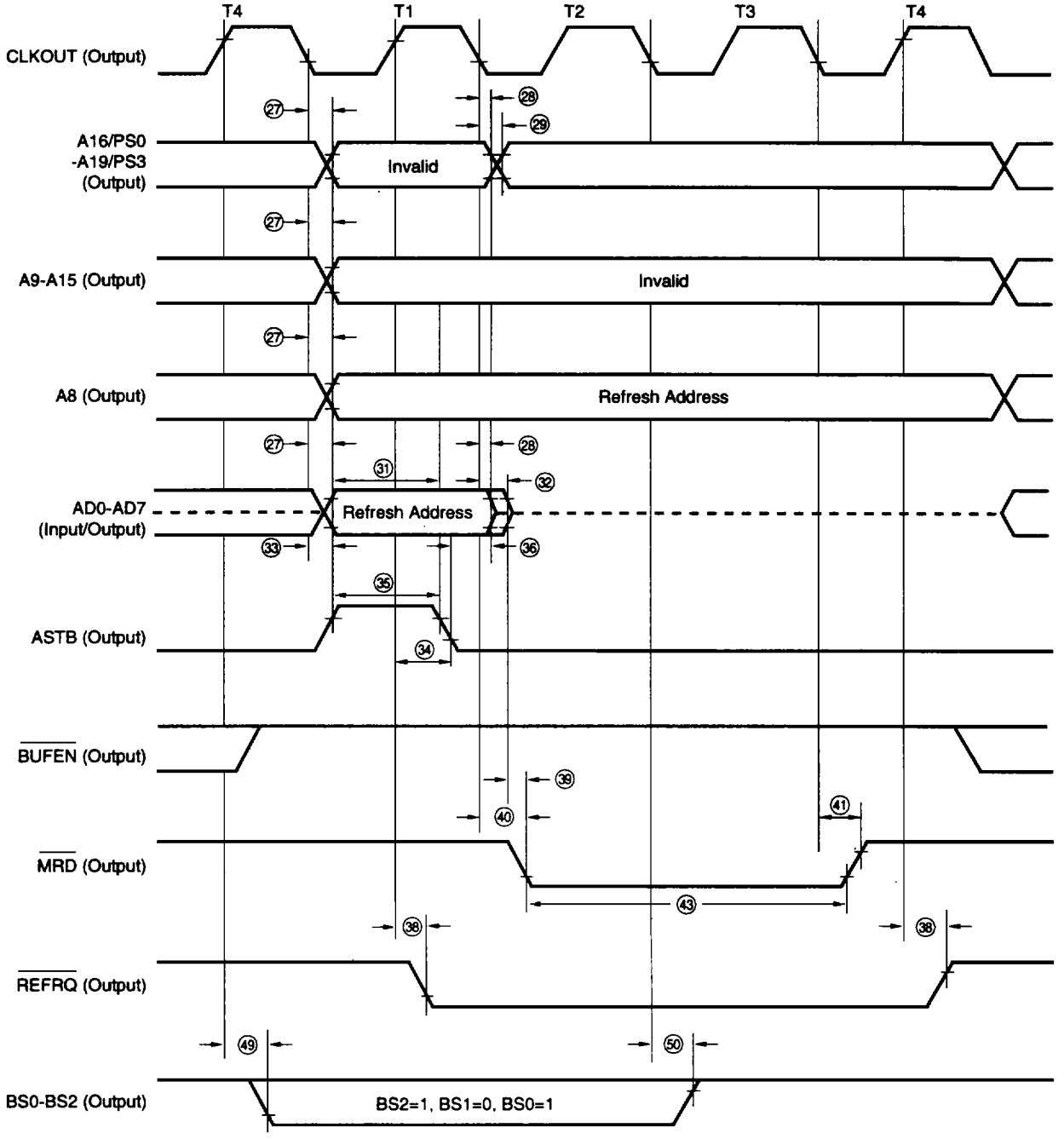
$\overline{\text{BUSLOCK}}$ Output Timing



Access Interval

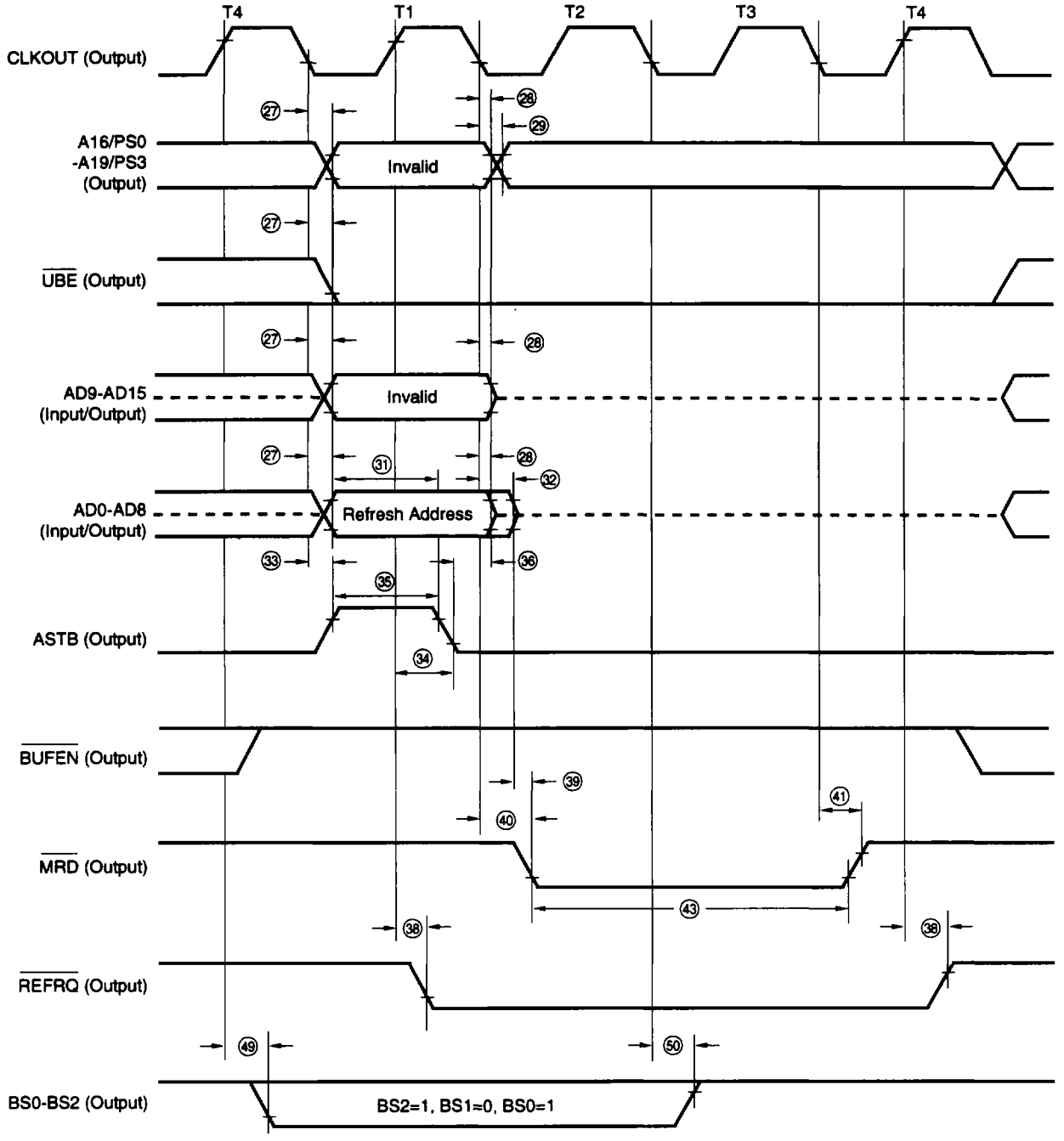


Refresh Timing (V40)



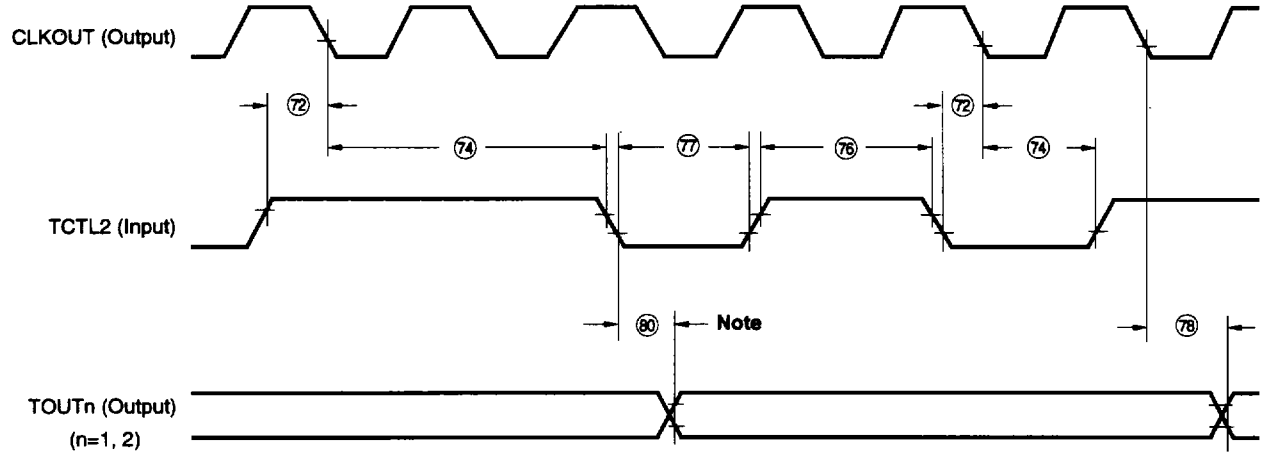
Remark A dashed line indicates high impedance.

Refresh Timing (V50)



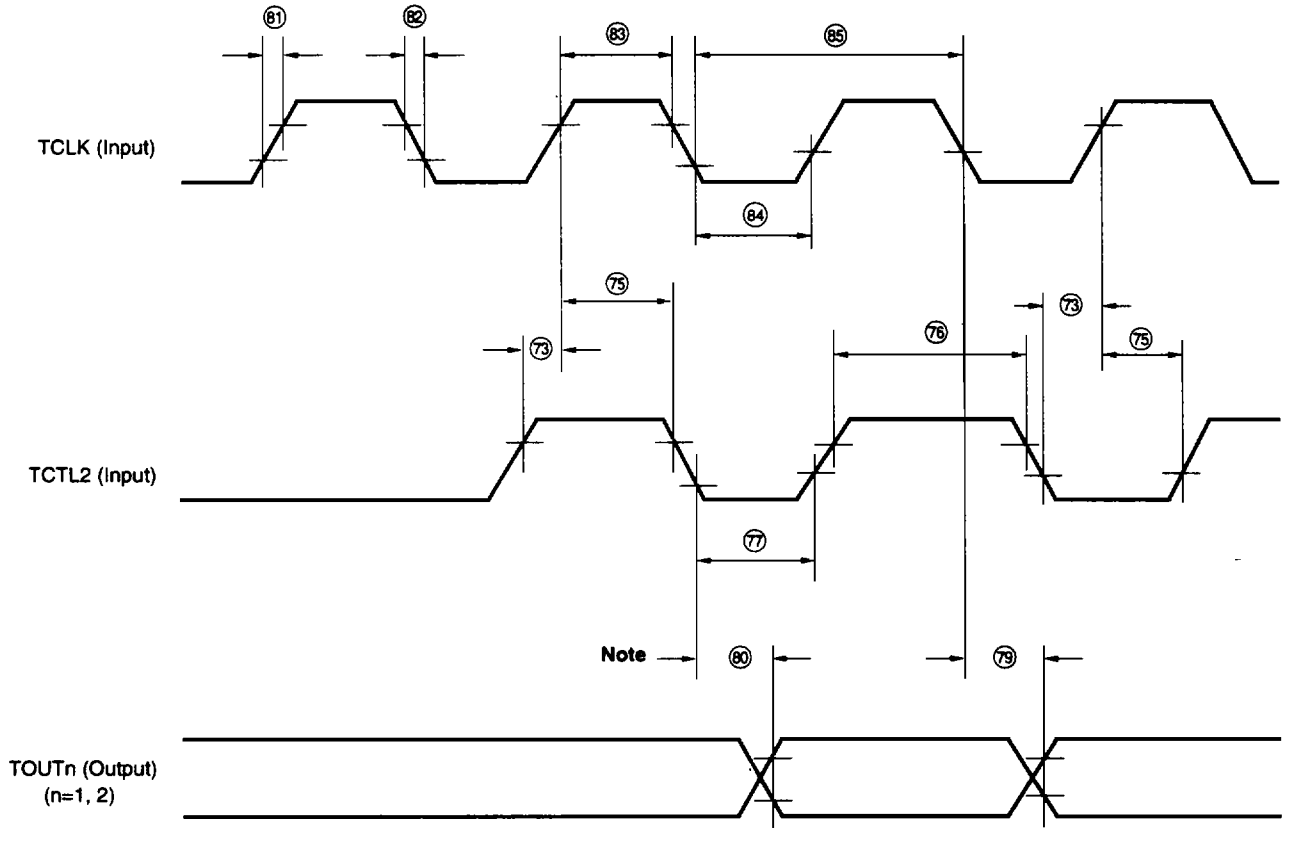
Remark A dashed line indicates high impedance.

TCU Timing (1)



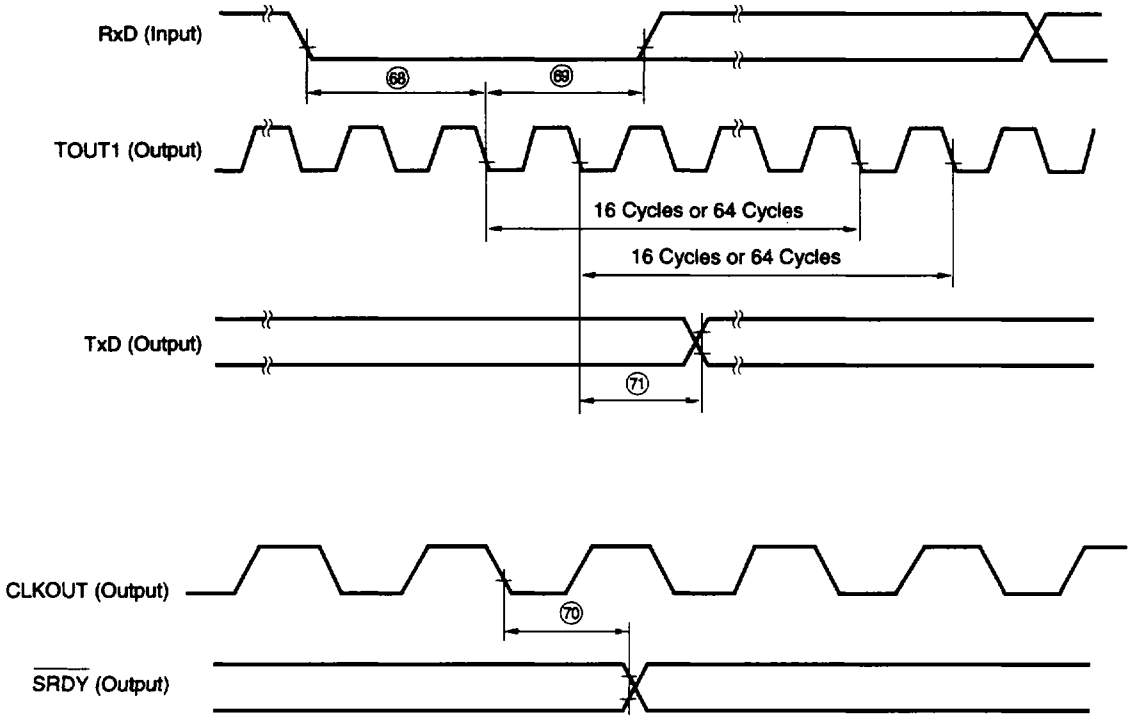
Note Applies to TOUT2 output.

TCU Timing (2)

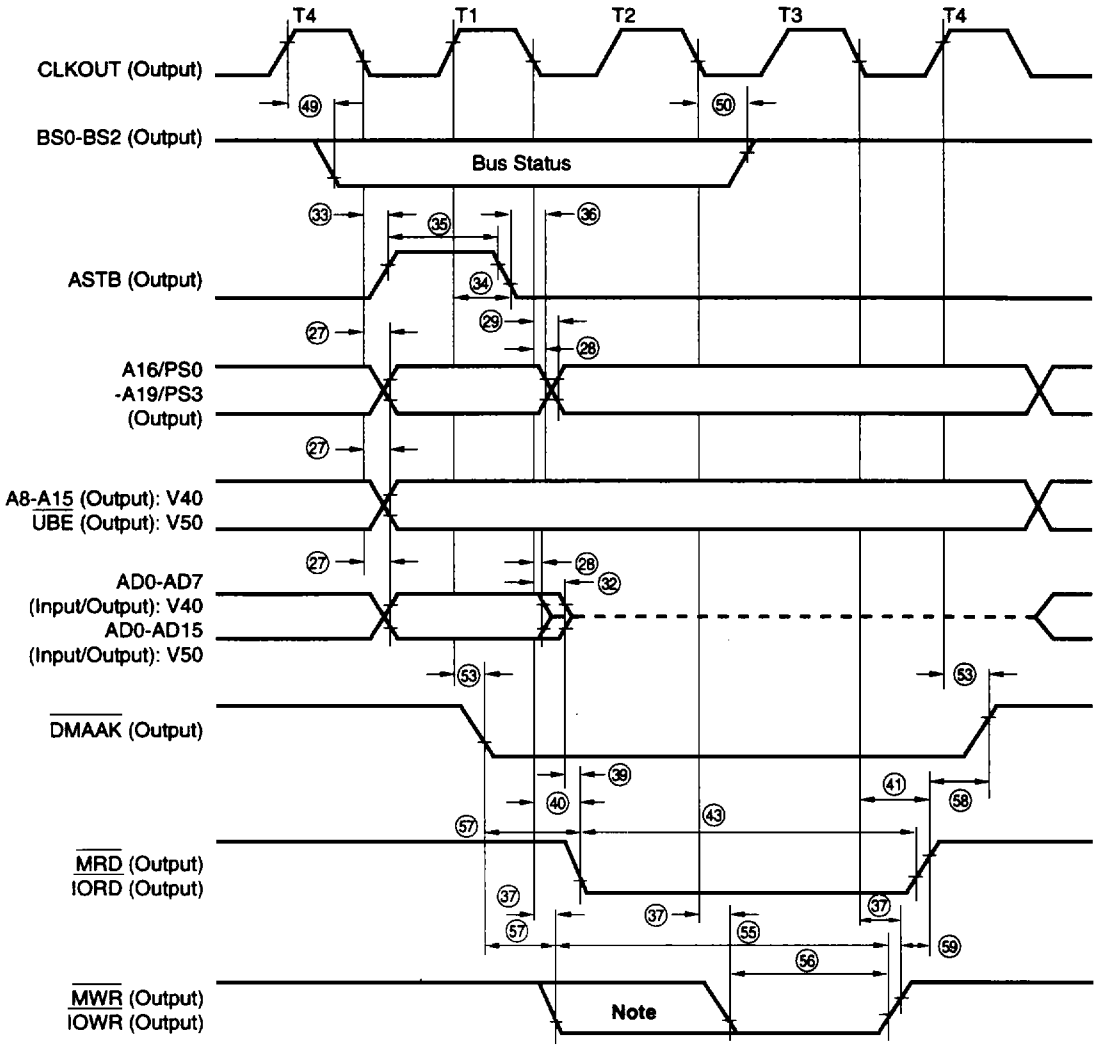


Note Applies to TOUT2 output.

SCU Timing


RxD (Input)
68
69
TOUT1 (Output)
16 Cycles or 64 Cycles
16 Cycles or 64 Cycles
TxD (Output)
71
CLKOUT (Output)
70
SRDY (Output)

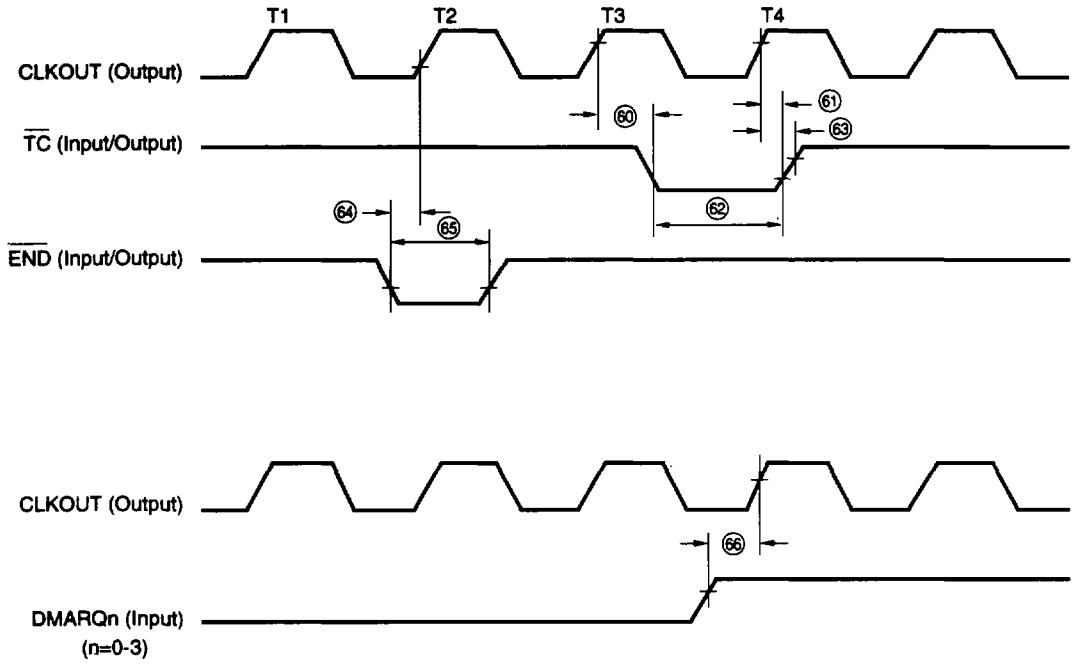
DMAU Timing (1)



Note Low-level signal is output in extended wrote mode.

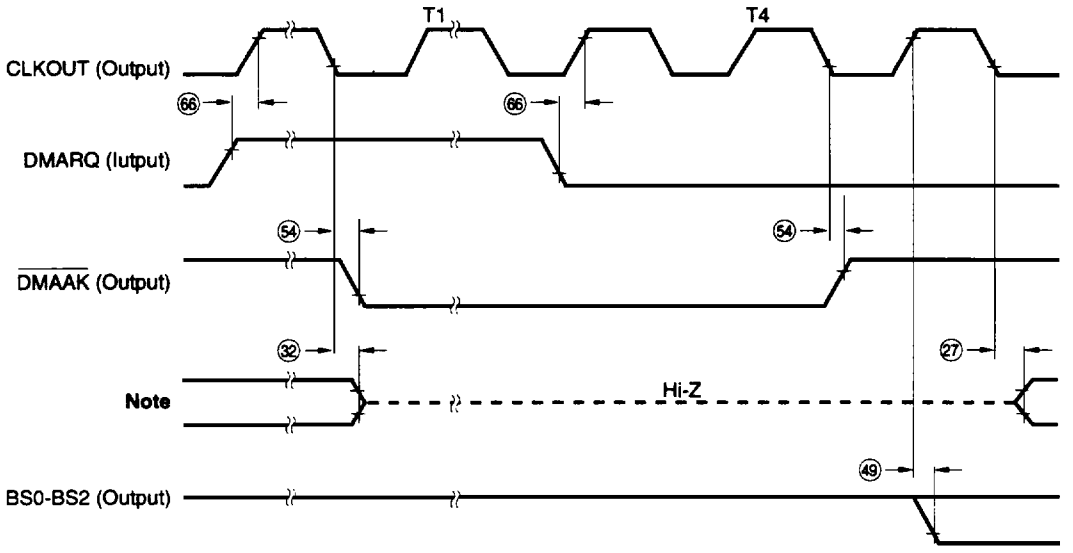
Remark A dashed line indicates high impedance.

DMAU Timing (2)



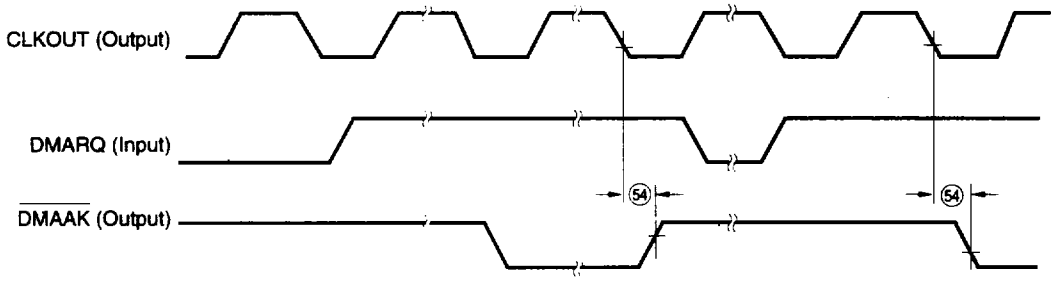
DMAU Timing (3) (Cascade Mode)

In Normal Operation:



Note A16/PS0-A19/PS3, BUFEN, BUFR/W, MRD, IORD, MWR, IOWR, BUSLOCK (All of these are outputs.)
:V40, V50
A8-A15 (Output), AD0-AD7 (Input/Output): V40 AD0-AD15 (Input/Output): V50

When Refresh Cycle is Inserted:



ICU Timing