Single-chip 8-bit microcontroller — 80C552/83C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C552/83C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552—8k bytes mask programmable ROM
- 80C552—ROMless version of the 83C552
- 87C552—8k bytes EPROM (described in a separate chapter)

The 8XC552 contains a non-volatile 8k × 8 read-only program memory (83C552), a volatile 256 × 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

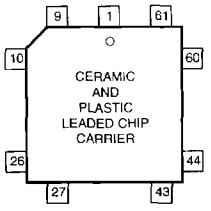
In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte, and 17 three-byte. With a 16MHz (24MHz) crystal, 58% of the instructions are executed in 0.75µs (0.5µs) and 40% in 1.5µs (1µs). Multiply and divide instructions require 3µs (2µs).

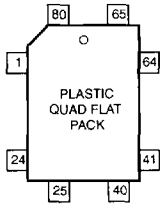
FEATURES

- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 × 8 RAM, expandable externally to 64k bytes
- Capable of producing eight synchronized, timed outputs
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three speed ranges:
  - 1.2 to 16MHz
  - 1.2 to 24MHz (ROM, ROMless only)
  - 1.2 to 30MHz (ROM, ROMless only)
- Three operating ambient temperature ranges:
  - PCB83C552–5: 0°C to +70°C
  - PCF83C552–5: –40°C to +85°C (XTAL frequency max. 24 MHz)
  - PCA83C552–5: –40°C to +125°C (XTAL frequency max. 16 MHz)

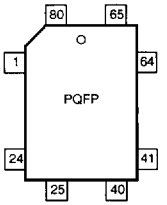
PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMSR1	42	P2.3/A11
9	P4.2/CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1/TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



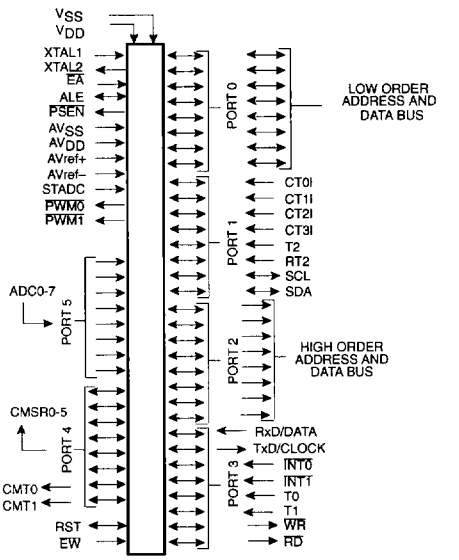
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function
1	P4.1/CMSR1	41	P2.3/A11
2	P4.2/CMSR2	42	P2.4/A12
3	NC	43	NC
4	P4.3/CMSR3	44	NC
5	P4.4/CMSR4	45	P2.5/A13
6	P4.5/CMSR5	46	P2.6/A14
7	P4.6/CMT0	47	P2.7/A15
8	P4.7/CMT1	48	$\overline{PSEN}$
9	RST	49	ALE
10	P1.0/CT0I	50	$\overline{EA}$
11	P1.1/CT1I	51	P0.7/AD7
12	P1.2/CT2I	52	P0.6/AD6
13	P1.3/CT3I	53	P0.5/AD5
14	P1.4/T2	54	P0.4/AD4
15	P1.5/RT2	55	P0.3/AD3
16	P1.6/SCL	56	P0.2/AD2
17	P1.7/SDA	57	P0.1/AD1
18	P3.0/RxD	58	P0.0/AD0
19	P3.1/TxD	59	AVref–
20	P3.2/$\overline{INT0}$	60	AVref+
21	NC	61	AV_{SS}
22	NC	62	NC
23	P3.3/$\overline{INT1}$	63	AV_{DD}
24	P3.4/T0	64	P5.7/ADC7
25	P3.5/T1	65	P5.6/ADC6
26	P3.6/$\overline{WR}$	66	P5.5/ADC5
27	P3.7/$\overline{RD}$	67	P5.4/ADC4
28	NC	68	P5.3/ADC3
29	NC	69	P5.2/ADC2
30	NC	70	P5.1/ADC1
31	XTAL2	71	P5.0/ADC0
32	XTAL1	72	V_{DD}
33	IC	73	IC
34	V_{SS}	74	STADC
35	V_{SS}	75	$\overline{PWM0}$
36	V_{SS}	76	$\overline{PWM1}$
37	NC	77	$\overline{EW}$
38	P2.0/A08	78	NC
39	P2.1/A09	79	NC
40	P2.2/A10	80	P4.0/CMSR0

NC = not connected
IC = internally connected (do not use)

LOGIC SYMBOL



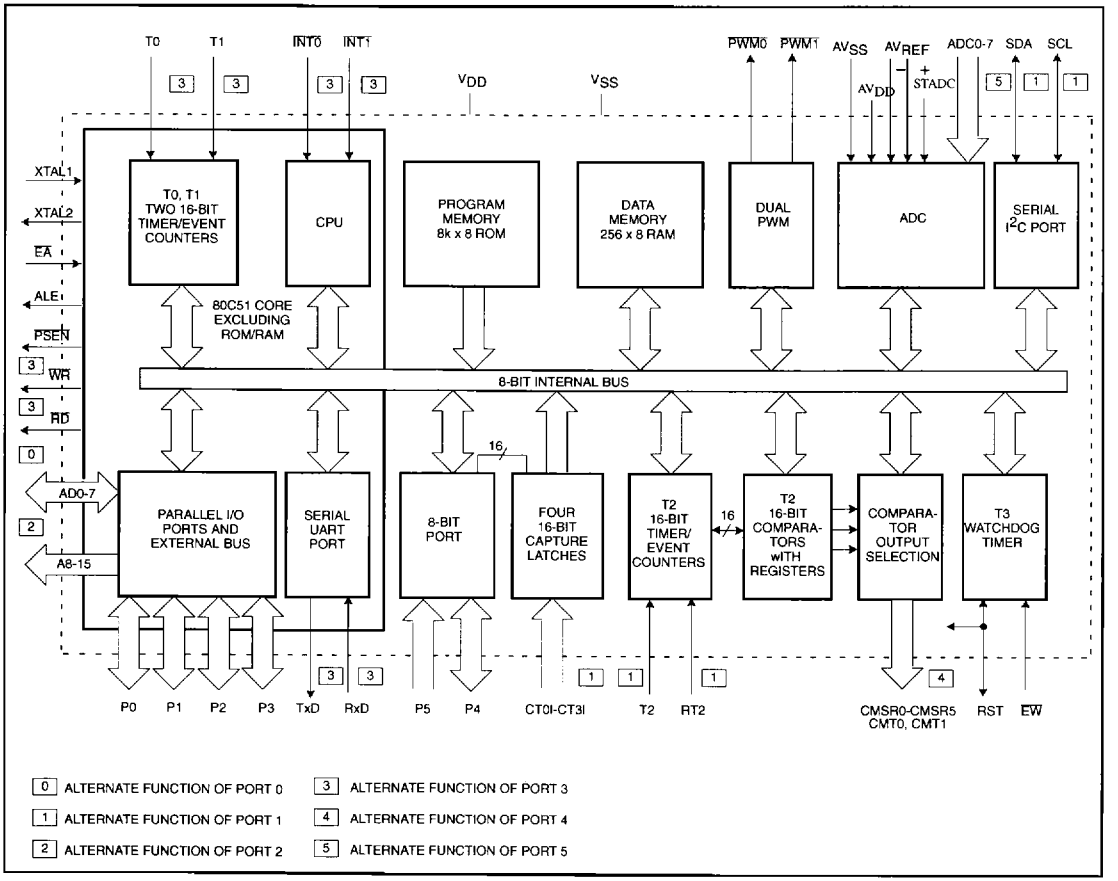
ORDERING INFORMATION

PHILIPS PART ORDER NUMBER PART MARKING		NORTH AMERICA PHILIPS PART ORDER NUMBER		DRAWING NUMBER	TEMPERATURE °C AND PACKAGE	FREQ MHz
ROMless	ROM	ROMless	ROM			
PCB80C552-5-16WP	PCB83C552-5WP/xxx	S80C552-4A68	S83C552-4A68	SOT188	0 to +70, Plastic Leaded Chip Carrier	16
PCB80C552-5-16H	PCB83C552-5H/xxx	S80C552-4B	S83C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
PCF80C552-5-16WP	PCF83C552-5WP/xxx	S80C552-5A68	S83C552-5A68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	16
PCF80C552-5-16H	PCF83C552-5H/xxx	S80C552-5B	S83C552-5B	SOT318	–40 to +85, Plastic Quad Flat Pack	16
PCA80C552-5-16WP	PCA83C552-5WP/xxx	S80C552-6A68	S83C552-6A68	SOT188	–40 to +125, Plastic Leaded Chip Carrier	16
PCA80C552-5-16H	PCA83C552-5H/xxx	S80C552-6B	S83C552-6B	SOT318	–40 to +125, Plastic Quad Flat Pack	16
PCB80C552-5-24WP	PCB83C552-5WP/xxx	S80C552-AA68	S83C552-AA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	24
PCB80C552-5-24H	PCB83C552-5H/xxx	S80C552-AB	S83C552-AB	SOT318	0 to +70, Plastic Quad Flat Pack	24
PCF80C552-5-24WP	PCF83C552-5WP/xxx	S80C552-BA68	S83C552-BA68	SOT188	–40 to +85, Plastic Leaded Chip Carrier	24
PCF80C552-5-24H	PCF83C552-5H/xxx	S80C552-BB	S83C552-BB	SOT318	–40 to +85, Plastic Quad Flat Pack	24
PCB80C552-5-30WP	PCB83C552-5WP/xxx	S80C552-CA68	S83C552-CA68	SOT188	0 to +70, Plastic Leaded Chip Carrier	30
PCB80C552-5-30H	PCB83C552-5H/xxx	S80C552-CB	S83C552-CB	SOT318	0 to +70, Plastic Quad Flat Pack	30

NOTE:
1. xxx denotes the ROM code number.

EPROM	DRAWING NUMBER	TEMPERATURE °C AND PACKAGE	FREQ MHz
S87C552-4A68	0398E	0 to +70, Plastic Leaded Chip Carrier	16
S87C552-4K68	1473A	0 to +70, Ceramic Leaded Chip Carrier w/Window	16
S87C552-4B	SOT318	0 to +70, Plastic Quad Flat Pack	16
S87C552-5A68	0398E	−40 to +85, Plastic Leaded Chip Carrier	16
S87C552-5K68	1473A	−40 to +85, Ceramic Leaded Chip Carrier w/Window	16
S87C552-5B	SOT318	−40 to +85, Plastic Quad Flat Pack	16

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO. PLCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{DD}	2	72	I	**Digital Power Supply:** +5V power supply pin during normal operation, idle and power-down mode.
STADC	3	74	I	**Start ADC Operation:** Input starting analog to digital conversion (ADC operation can also be started by software). This pin must not float.
$\overline{PWM0}$	4	75	O	**Pulse Width Modulation:** Output 0.
$\overline{PWM1}$	5	76	O	**Pulse Width Modulation:** Output 1.
$\overline{EW}$	6	77	I	**Enable Watchdog Timer:** Enable for T3 watchdog timer and disable power-down mode. This pin must not float.
P0.0-P0.7	57-50	58-51	I/O	**Port 0:** Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s.
P1.0-P1.7	16-23	10-17	I/O	**Port 1:** 8-bit I/O port. Alternate functions include:
	16-21	10-15	I/O	**(P1.0-P1.5):** Quasi-bidirectional port pins.
	22-23	16-17	I/O	**(P1.6, P1.7):** Open drain port pins.
	16-19	10-13	I	**CT0I-CT3I (P1.0-P1.3):** Capture timer input signals for timer T2.
	20	14	I	**T2 (P1.4):** T2 event input.
	21	15	I	**RT2 (P1.5):** T2 timer reset signal. Rising edge triggered.
	22	16	I/O	**SCL (P1.6):** Serial port clock line I^2C-bus.
	23	17	I/O	**SDA (P1.7):** Serial port data line I^2C-bus.
				Port 1 is also used to input the lower order address byte during EPROM programming and verification. A0 is on P1.0, etc.
P2.0-P2.7	39-46	38-42, 45-47	I/O	**Port 2:** 8-bit quasi-bidirectional I/O port. Alternate function: High-order address byte for external memory (A08-A15).
P3.0-P3.7	24-31	18-20, 23-27	I/O	**Port 3:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	24	18		**RxD(P3.0):** Serial input port.
	25	19		**TxD (P3.1):** Serial output port.
	26	20		**$\overline{INT0}$ (P3.2):** External interrupt.
	27	23		**$\overline{INT1}$ (P3.3):** External interrupt.
	28	24		**T0 (P3.4):** Timer 0 external input.
	29	25		**T1 (P3.5):** Timer 1 external input.
	30	26		**$\overline{WR}$ (P3.6):** External data memory write strobe.
	31	27		**$\overline{RD}$ (P3.7):** External data memory read strobe.
P4.0-P4.7	7-14	80, 1-2 4-8	I/O	**Port 4:** 8-bit quasi-bidirectional I/O port. Alternate functions include:
	7-12	80, 1-2 4-6	O	**CMSR0-CMSR5 (P4.0-P4.5):** Timer T2 compare and set/reset outputs on a match with timer T2.
	13, 14	7, 8	O	**CMT0, CMT1 (P4.6, P4.7):** Timer T2 compare and toggle outputs on a match with timer T2.
P5.0-P5.7	68-62, 1	71-64,	I	**Port 5:** 8-bit input port. **ADC0-ADC7 (P5.0-P5.7):** Alternate function: Eight input channels to ADC.
RST	15	9	I/O	**Reset:** Input to reset the 8XC552. It also provides a reset pulse as output when timer T3 overflows.
XTAL1	35	32	I	**Crystal Input 1:** Input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external clock signal when an external oscillator is used.
XTAL2	34	31	O	**Crystal Input 2:** Output of the inverting amplifier that forms the oscillator. Left open-circuit when an external clock is used.

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO. PLCC	PIN NO. QFP	TYPE	NAME AND FUNCTION
V_{SS}	36, 37	34-36	I	**Two Digital ground pins.**
$\overline{PSEN}$	47	48	O	**Program Store Enable:** Active-low read strobe to external program memory.
ALE	48	49	O	**Address Latch Enable:** Latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access, one ALE pulse is skipped. ALE can drive up to eight LS TTL inputs and handles CMOS inputs without an external pull-up.
$\overline{EA}$	49	50	I	**External Access:** When $\overline{EA}$ is held at TTL level high, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL low level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
AV_{REF-}	58	59	I	**Analog to Digital Conversion Reference Resistor:** Low-end.
AV_{REF+}	59	60	I	**Analog to Digital Conversion Reference Resistor:** High-end.
AV_{SS}	60	61	I	**Analog Ground**
AV_{DD}	61	63	I	**Analog Power Supply**

NOTE:
1. To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0.5V or V_{SS} – 0.5V, respectively.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 799.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{DD} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PWM0/ PWM1
Idle	Internal	1	1	Data	Data	Data	Data	Data	1
Idle	External	1	1	Float	Data	Address	Data	Data	1
Power-down	Internal	0	0	Data	Data	Data	Data	Data	1
Power-down	External	0	0	Float	Data	Data	Data	Data	1

Serial Control Register (S1CON) – See Table 2

S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC} 6MHz	12MHz	16MHz	24MHz[2]	30MHz[2]	f_{OSC} DIVIDED BY
0	0	0	23	47	62.5	94	117 [1]	256
0	0	1	27	54	71	107 [1]	134 [1]	224
0	1	0	31	63	83.3	125 [1]	156 [1]	192
0	1	1	37	75	100	150 [1]	188 [1]	160
1	0	0	6.25	12.5	17	25	31	960
1	0	1	50	100	133 [1]	200 [1]	250 [1]	120
1	1	0	100	200	267 [1]	400 [1]	500 [1]	60
1	1	1	0.24 < 62.5	0.49 < 62.5	0.65 < 55.6	0.98 < 50.0	1.22 < 52.1	96 × (256 – (reload value Timer 1))
			0 < 255	0 < 254	0 < 253	0 <251	0 < 250	reload value Timer 1 in Mode 2.

NOTES:
1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.
2. At f_{OSC} = 24MHz/ 30MHz the maximum I²C bus rate of 100kHz cannot be realized due to the fixed divider rates.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Input, output DC current on any single I/O pin	5.0	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid appiying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DEVICE SPECIFICATIONS

TYPE	SUPPLY VOLTAGE (V) MIN	MAX	FREQUENCY (MHz) MIN	MAX	TEMPERATURE RANGE (°C)
PCB83(0)C552-5-16	4.0	6.0	1.2	16	0 to +70
PCF83(0)C552-5-16	4.0	6.0	1.2	16	–40 to +85
PCA83(0)C552-5-16	4.5	5.5	1.2	16	–40 to +125
PCB83(0)C552-5-24	4.5	5.5	1.2	24	0 to +70
PCF83(0)C552-5-24	4.5	5.5	1.2	24	–40 to +85
PCB83(0)C552-5-30	4.5	5.5	1.2	30	0 to +70

DC ELECTRICAL CHARACTERISTICS

V_{SS}, AV_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
I_{DD}	Supply current operating:	See notes 1 and 2			
	PCB8XC552-5-16	f_{OSC} = 16MHz		45	mA
	PCF8XC552-5-16	f_{OSC} = 16MHz		45	mA
	PCA8XC552-5-16	f_{OSC} = 16MHz		40	mA
	PCB8XC552-5-24	f_{OSC} = 24MHz		55	mA
	PCF8XC552-5-24	f_{OSC} = 24MHz		55	mA
	PCB8XC552-5-30	f_{OSC} = 30MHz		68	mA
I_{ID}	Idle mode:	See notes 1 and 3			
	PCB8XC552-5-16	f_{OSC} = 16MHz		10	mA
	PCF8XC552-5-16	f_{OSC} = 16MHz		10	mA
	PCA8XC552-5-16	f_{OSC} = 16MHz		9	mA
	PCB8XC552-5-24	f_{OSC} = 24MHz		12.5	mA
	PCF8XC552-5-24	f_{OSC} = 24MHz		12.5	mA
	PCB8XC552-5-30	f_{OSC} = 30MHz		15	mA
I_{PD}	Power-down current:	See notes 1 and 4; 2V < V_{PD} < V_{DD} max			
	PCB8XC552			50	µA
	PCF8XC552			50	µA
	PCA8XC552			150	µA
Inputs					
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6, P1.7		–0.5	$0.2V_{DD}$–0.1	V
V_{IL1}	Input low voltage to $\overline{EA}$		–0.5	$0.2V_{DD}$–0.3	V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[5]		–0.5	$0.3V_{DD}$	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA		$0.2V_{DD}$+0.9	V_{DD}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{DD}$	V_{DD}+0.5	V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[5]		$0.7V_{DD}$	6.0	V
I_{IL}	Logical 0 input current, ports 1, 2, 3, 4, except P1.6, P1.7	V_{IN} = 0.45V		–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, 4, except P1.6, P1.7	See note 6		–650	µA
$\pm I_{IL1}$	Input leakage current, port 0, $\overline{EA}$, STADC, $\overline{EW}$	0.45V < V_I < V_{DD}		10	µA
$\pm I_{IL2}$	Input leakage current, P1.6/SCL, P1.7/SDA	0V < V_I < 6V 0V < V_{DD} < 5.5V		10	µA
$\pm I_{IL3}$	Input leakage current, port 5	0.45V < V_I < V_{DD}		1	µA
Outputs					
V_{OL}	Output low voltage, ports 1, 2, 3, 4, except P1.6, P1.7	I_{OL} = 1.6mA[7]		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$	I_{OL} = 3.2mA[7]		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA	I_{OL} = 3.0mA[7]		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA	V_{DD} = 5V +10% $-I_{OH}$ = 60µA $-I_{OH}$ = 25µA $-I_{OH}$ = 10µA	 2.4 $0.75V_{DD}$ $0.9V_{DD}$		 V V V

DC ELECTRICAL CHARACTERISTICS (Continued)

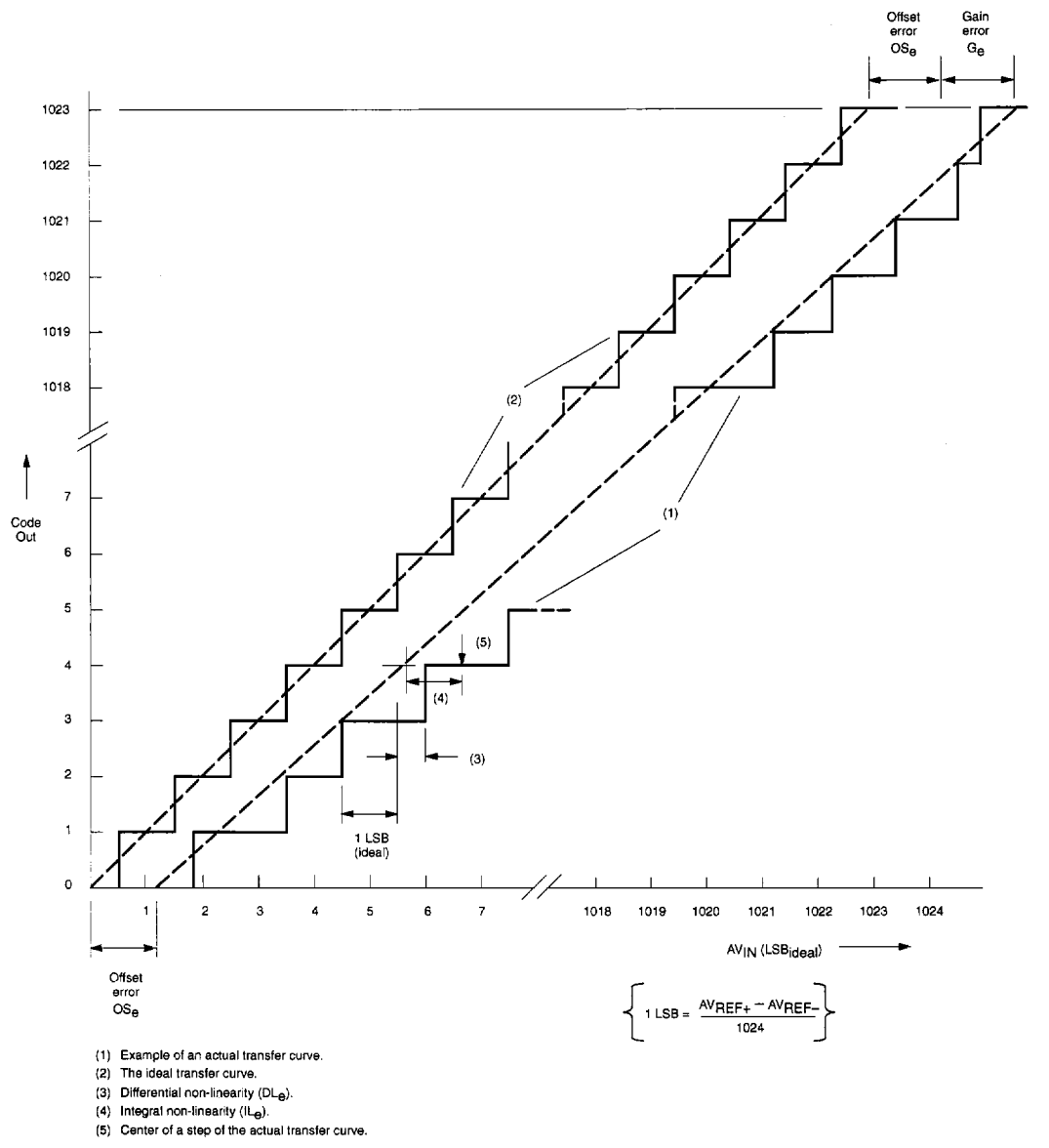
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
Outputs (Continued)					
V_{OH1}	Output high voltage (port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)[8]	V_{DD} = 5V +10% $-I_{OH}$ = 400µA $-I_{OH}$ = 150µA $-I_{OH}$ = 40µA	 2.4 0.75V_{DD} 0.9V_{DD}		 V V V
V_{OH2}	Output high voltage (RST)	$-I_{OH}$ = 400µA $-I_{OH}$ = 120µA	2.4 0.8V_{DD}		V V
R_{RST}	Internal reset pull-down resistor		50	150	kΩ
C_{IO}	Pin capacitance	Test freq = 1MHz, T_{amb} = 25°C		10	pF
Analog Inputs					
AV_{DD}	Analog supply voltage: PCB8XC552-5-16 PCF8XC552-5-16 PCA8XC552-5-16 PCB8XC552-5-24 PCF8XC552-5-24 PCB8XC552-5-30	 $AV_{DD} = V_{DD} \pm 0.2V$ $AV_{DD} = V_{DD} \pm 0.2V$ $AV_{DD} = V_{DD} \pm 0.2V$ $AV_{DD} = V_{DD} \pm 0.2V$ $AV_{DD} = V_{DD} \pm 0.2V$ $AV_{DD} = V_{DD} \pm 0.2V$	 4.0 4.0 4.5 4.5 4.5 4.5	 6.0 6.0 5.5 5.5 5.5 5.5	 V V V V V V
AI_{DD}	Analog supply current: operating: (16MHz) Analog supply current: operating: (24MHz, 30MHz)	Port 5 = 0 to AV_{DD} Port 5 = 0 to AV_{DD}		1.2 1.0	mA mA
AI_{ID}	Idle mode: PCB8XC552-5-16 PCF8XC552-5-16 PCA8XC552-5-16 PCB8XC552-5-24 PCF8XC552-5-24 PCB8XC552-5-30			 50 50 100 50 50 50	 µA µA µA µA µA µA
AI_{PD}	Power-down mode: PCB8XC552 PCF8XC552 PCA8XC552	2V < AV_{PD} < AV_{DD} max		 50 50 100	 µA µA µA
AV_{IN}	Analog input voltage		AV_{SS}–0.2	AV_{DD}+0.2	V
AV_{REF}	Reference voltage: AV_{REF-} AV_{REF+}		 AV_{SS}–0.2	 AV_{DD}+0.2	 V V
R_{REF}	Resistance between AV_{REF+} and AV_{REF-}		10	50	kΩ
C_{IA}	Analog input capacitance			15	pF
t_{ADS}	Sampling time			$8t_{CY}$	µs
t_{ADC}	Conversion time (including sampling time)			$50t_{CY}$	µs
DL_e	Differential non-linearity[10, 11, 12]			±1	LSB
IL_e	Integral non-linearity[10, 13]			±2	LSB
OS_e	Offset error[10, 14]			±2	LSB

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNIT
Analog Inputs (continued)					
G_e	Gain error[10, 15]			±0.4	%
A_e	Absolute voltage error[10, 16]			±3	LSB
M_{CTC}	Channel to channel matching			±1	LSB
C_t	Crosstalk between inputs of port 5[17]	0–100kHz		–60	dB

NOTES FOR DC ELECTRICAL CHARACTERISTICS:

1. See Figures 10 through 15 for I_{DD} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5V$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = $\overline{EW} = V_{DD}$; STADC = V_{SS}.
3. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{DD} - 0.5V$; XTAL2 not connected; Port 0 = $\overline{EW} = V_{DD}$; $\overline{EA}$ = RST = STADC = V_{SS}.
4. The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = $\overline{EW} = V_{DD}$; $\overline{EA}$ = RST = STADC = XTAL1 = V_{SS}.
5. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
6. Pins of ports 1 (except P1.6, P1.7), 2, 3, and 4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
7. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
8. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{DD}$ specification when the address bits are stabilizing.
9. The following condition must not be exceeded: $V_{DD} - 0.2V < AV_{DD} < V_{DD} + 0.2V$.
10. Conditions: $AV_{REF-} = 0V$; $AV_{DD} = 5.0V$, AV_{REF+} (80C552, 83C552) = 5.12V. ADC is monotonic with no missing codes. Measurement by continuous conversion of AV_{IN} = –20mV to 5.12V in steps of 0.5mV.
11. The differential non-linearity (DL_e) is the difference between the actual step width and the ideal step width. (See Figure 1.)
12. The ADC is monotonic; there are no missing codes.
13. The integral non-linearity (IL_e) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset error. (See Figure 1.)
14. The offset error (OS_e) is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. (See Figure 1.)
15. The gain error (G_e) is the relative difference in percent between the straight line fitting the actual transfer curve (after removing offset error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve. (See Figure 1.)
16. The absolute voltage error (A_e) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve.
17. This should be considered when both analog and digital signals are simultaneously input to port 5.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential non-linearity (DL_e).
(4) Integral non-linearity (IL_e).
(5) Center of a step of the actual transfer curve.

Figure 1. ADC Conversion Characteristic

AC ELECTRICAL CHARACTERISTICS[1, 2]

16 MHz version

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	2	Oscillator frequency			1.2	16	MHz
t_{LHLL}	2	ALE pulse width	85		$2t_{CLCL}-40$		ns
t_{AVLL}	2	Address valid to ALE low	8		$t_{CLCL}-55$		ns
t_{LLAX}	2	Address hold after ALE low	28		$t_{CLCL}-35$		ns
t_{LLIV}	2	ALE low to valid instruction in		150		$4t_{CLCL}-100$	ns
t_{LLPL}	2	ALE low to $\overline{PSEN}$ low	23		$t_{CLCL}-40$		ns
t_{PLPH}	2	$\overline{PSEN}$ pulse width	143		$3t_{CLCL}-45$		ns
t_{PLIV}	2	$\overline{PSEN}$ low to valid instruction in		83		$3t_{CLCL}-105$	ns
t_{PXIX}	2	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	2	Input instruction float after $\overline{PSEN}$		38		$t_{CLCL}-25$	ns
t_{AVIV}	2	Address to valid instruction in		208		$5t_{CLCL}-105$	ns
t_{PLAZ}	2	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	3	$\overline{RD}$ pulse width	275		$6t_{CLCL}-100$		ns
t_{WLWH}	4	$\overline{WR}$ pulse width	275		$6t_{CLCL}-100$		ns
t_{RLDV}	3	$\overline{RD}$ low to valid data in		148		$5t_{CLCL}-165$	ns
t_{RHDX}	3	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	3	Data float after $\overline{RD}$		55		$2t_{CLCL}-70$	ns
t_{LLDV}	3	ALE low to valid data in		350		$8t_{CLCL}-150$	ns
t_{AVDV}	3	Address to valid data in		398		$9t_{CLCL}-165$	ns
t_{LLWL}	3, 4	ALE low to $\overline{RD}$ or $\overline{WR}$ low	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	3, 4	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	120		$4t_{CLCL}-130$		ns
t_{QVWX}	4	Data valid to $\overline{WR}$ transition	3		$t_{CLCL}-60$		ns
t_{DW}	4	Data before $\overline{WR}$	288		$7t_{CLCL}-150$		ns
t_{WHQX}	4	Data hold after $\overline{WR}$	13		$t_{CLCL}-50$		ns
t_{RLAZ}	3	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	3, 4	$\overline{RD}$ or $\overline{WR}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
External Clock							
t_{CHCX}	5	High time[4]	20		20		ns
t_{CLCX}	5	Low time[4]	20		20		ns
t_{CLCH}	5	Rise time[4]		20		20	ns
t_{CHCL}	5	Fall time[4]		20		20	ns
Serial Timing – Shift Register Mode[4] (Test Conditions: T_{amb} = 0°C to +70°C; V_{SS} = 0V; Load Capacitance = 80pF)							
t_{XLXL}	6	Serial port clock cycle time	0.75		$12t_{CLCL}$		µs
t_{QVXH}	6	Output data setup to clock rising edge	492		$10t_{CLCL}-133$		ns
t_{XHQX}	6	Output data hold after clock rising edge	8		$2t_{CLCL}-117$		ns
t_{XHDX}	6	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	6	Clock rising edge to input data valid		492		$10t_{CLCL}-133$	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period.
   t_{CLCL} = 83.3ns at f_{OSC} = 12MHz.
   t_{CLCL} = 62.5ns at f_{OSC} = 16MHz.
4. These values are characterized but not 100% production tested.

AC ELECTRICAL CHARACTERISTICS (Continued)[1, 2]

24/30 MHz version

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		30MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	2	Oscillator frequency					1.2	24	MHz
t_{LHLL}	2	ALE pulse width	43		27		$2t_{CLCL}-40$		ns
t_{AVLL}	2	Address valid to ALE low	17		8		$t_{CLCL}-25$		ns
t_{LLAX}	2	Address hold after ALE low	17		8		$t_{CLCL}-25$		ns
t_{LLIV}	2	ALE low to valid instruction in		102		68		$4t_{CLCL}-65$	ns
t_{LLPL}	2	ALE low to $\overline{PSEN}$ low	17		8		$t_{CLCL}-25$		ns
t_{PLPH}	2	$\overline{PSEN}$ pulse width	80		55		$3t_{CLCL}-45$		ns
t_{PLIV}	2	$\overline{PSEN}$ low to valid instruction in		65		40		$3t_{CLCL}-60$	ns
t_{PXIX}	2	Input instruction hold after $\overline{PSEN}$	0		0		0		ns
t_{PXIZ}	2	Input instruction float after $\overline{PSEN}$		17		8		$t_{CLCL}-25$	ns
t_{AVIV}	2	Address to valid instruction in		128		87		$5t_{CLCL}-80$	ns
t_{PLAZ}	2	$\overline{PSEN}$ low to address float		10		10		10	ns
Data Memory									
t_{RLRH}	3	$\overline{RD}$ pulse width	150		100		$6t_{CLCL}-100$		ns
t_{WLWH}	4	$\overline{WR}$ pulse width	150		100		$6t_{CLCL}-100$		ns
t_{RLDV}	3	$\overline{RD}$ low to valid data in		118		77		$5t_{CLCL}-90$	ns
t_{RHDX}	3	Data hold after $\overline{RD}$	0		0		0		ns
t_{RHDZ}	3	Data float after $\overline{RD}$		55		39		$2t_{CLCL}-28$	ns
t_{LLDV}	3	ALE low to valid data in		183		117		$8t_{CLCL}-150$	ns
t_{AVDV}	3	Address to valid data in		210		135		$9t_{CLCL}-165$	ns
t_{LLWL}	3, 4	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	50	150	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	3, 4	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	92		58		$4t_{CLCL}-75$		ns
t_{QVWX}	4	Data valid to $\overline{WR}$ transition	12		3		$t_{CLCL}-30$		ns
t_{DW}	4	Data before $\overline{WR}$	162		103		$7t_{CLCL}-130$		ns
t_{WHQX}	4	Data hold after $\overline{WR}$	17		8		$t_{CLCL}-25$		ns
t_{RLAZ}	3	$\overline{RD}$ low to address float		0		0		0	ns
t_{WHLH}	3, 4	$\overline{RD}$ or $\overline{WR}$ high to ALE high	17	67	8	58	$t_{CLCL}-25$	$t_{CLCL}+25$	ns
External Clock									
t_{CHCX}	5	High time[3]	17		15		17		ns
t_{CLCX}	5	Low time[3]	17		15		17		ns
t_{CLCH}	5	Rise time[3]		5		3		20	ns
t_{CHCL}	5	Fall time[3]		5		3		20	ns
Serial Timing – Shift Register Mode[3] (Test Conditions: T_{amb} = 0°C to +70°C; V_{SS} = 0V; Load Capacitance = 80pF)									
t_{XLXL}	6	Serial port clock cycle time	0.5		0.4		$12t_{CLCL}$		µs
t_{QVXH}	6	Output data setup to clock rising edge	283		200		$10t_{CLCL}-133$		ns
t_{XHQX}	6	Output data hold after clock rising edge	23		6.6		$2t_{CLCL}-60$		ns
t_{XHDX}	6	Input data hold after clock rising edge	0		0		0		ns
t_{XHDV}	6	Clock rising edge to input data valid		283		200		$10t_{CLCL}-133$	ns

NOTES:

1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. These values are characterized but not 100% production tested.
4. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period.
   t_{CLCL} = 41.7ns at f_{OSC} = 24MHz.

AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	INPUT	OUTPUT
I²C Interface (Refer to Figure 9)			
t_{HD}; STA	START condition hold time	≥ 14 t_{CLCL}	> 4.0µs [1]
t_{LOW}	SCL low time	≥ 16 t_{CLCL}	> 4.7µs [1]
t_{HIGH}	SCL high time	≥ 14 t_{CLCL}	> 4.0µs [1]
t_{RC}	SCL rise time	≤ 1µs	– [2]
t_{FC}	SCL fall time	≤ 0.3µs	< 0.3µs [3]
t_{SU}; DAT1	Data set-up time	≥ 250ns	> 20 t_{CLCL} – t_{RD}
t_{SU}; DAT2	SDA set-up time (before rep. START cond.)	≥ 250ns	> 1µs [1]
t_{SU}; DAT3	SDA set-up time (before STOP cond.)	≥ 250ns	> 8 t_{CLCL}
t_{HD}; DAT	Data hold time	≥ 0ns	> 8 t_{CLCL} – t_{FC}
t_{SU}; STA	Repeated START set-up time	≥ 14 t_{CLCL}	> 4.7µs [1]
t_{SU}; STO	STOP condition set-up time	≥ 14 t_{CLCL}	> 4.0µs [1]
t_{BUF}	Bus free time	≥ 14 t_{CLCL}	> 4.7µs [1]
t_{RD}	SDA rise time	≤ 1µs	– [2]
t_{FD}	SDA fall time	≤ 0.3µs	< 0.3µs [3]

NOTES:
1. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
4. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period at pin XTAL1. For 62ns, 42ns, 33.3ns < t_{CLCL} < 285ns (16MHz, 24MHz, 30MHz > f_{OSC} > 1.2MHz) the SI01 interface meets the I²C-bus specification for bit-rates up to 100 kbit/s.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} = Time for ALE low to $\overline{PSEN}$ low.

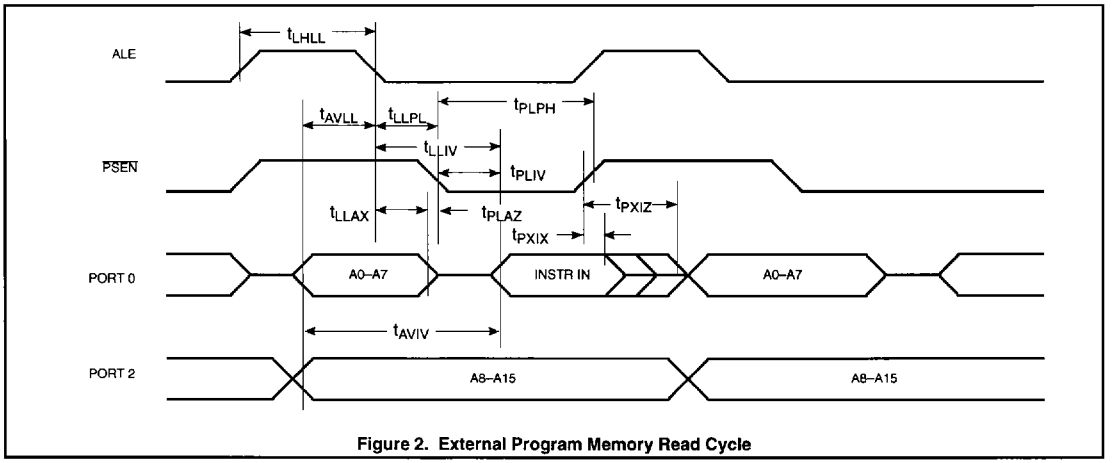


Figure 2. External Program Memory Read Cycle

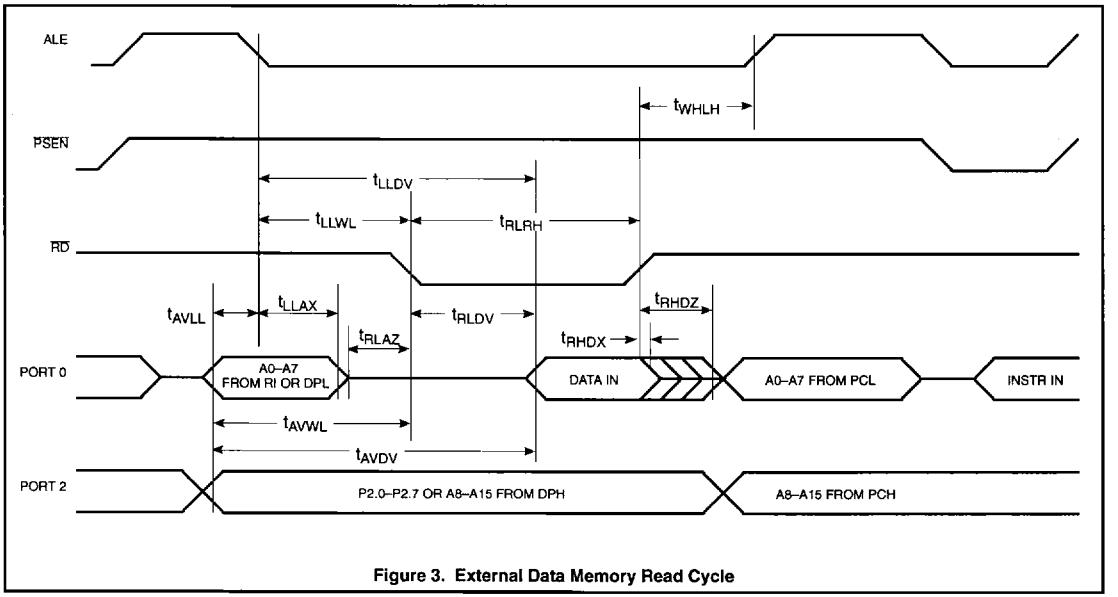


Figure 3. External Data Memory Read Cycle

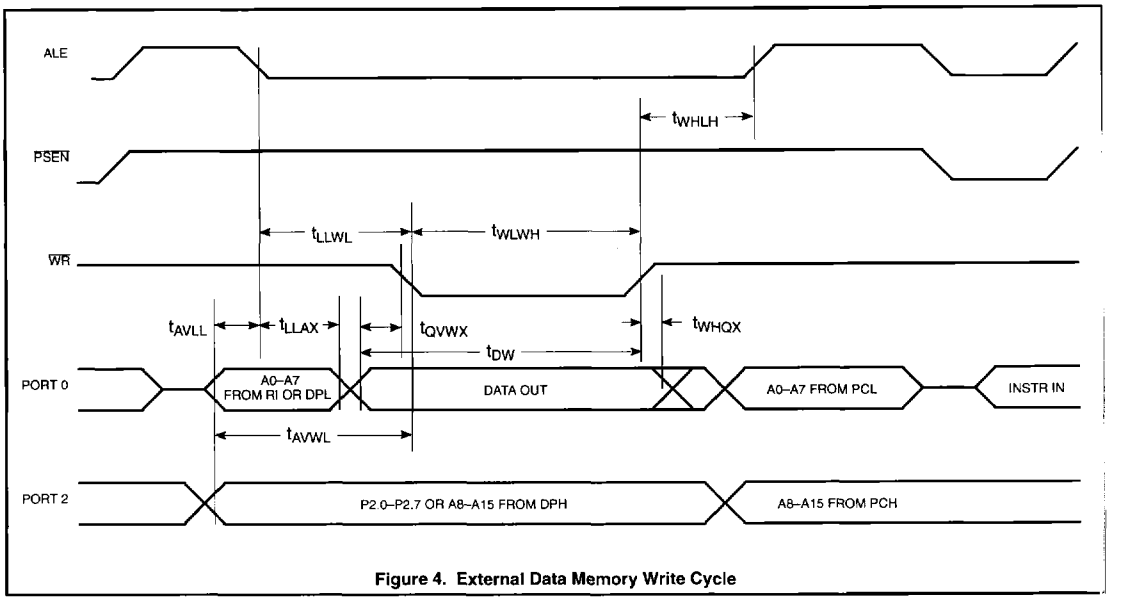


Figure 4. External Data Memory Write Cycle

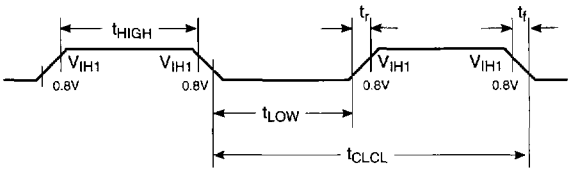


Figure 5. External Clock Drive XTAL1

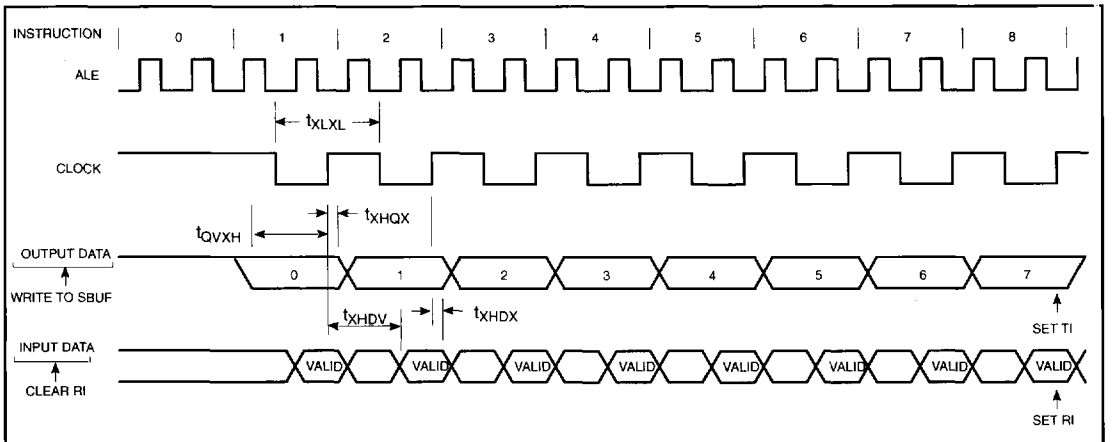
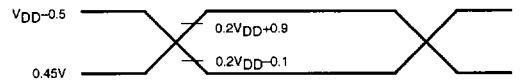
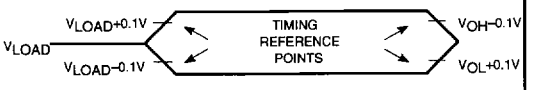


Figure 6. Shift Register Mode Timing



NOTE:
AC INPUTS DURING TESTING ARE DRIVEN AT V_{DD}–0.5 FOR A LOGIC '1' AND 0.45V FOR A LOGIC '0'. TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN FOR A LOGIC '1' AND V_{IL} MAX FOR A LOGIC '0'.

Figure 7. AC Testing Input/Output



NOTE:
FOR TIMING PURPOSES, A PORT IS NO LONGER FLOATING WHEN A 100MV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OH}/I_{OL} \geq \pm$ 20mA.

Figure 8. Float Waveform

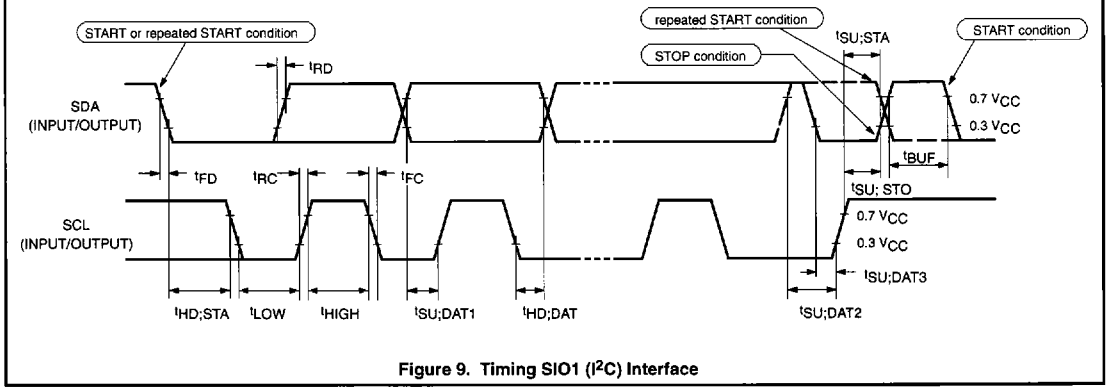
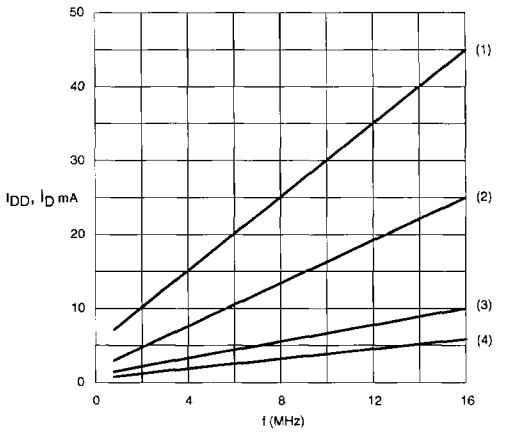


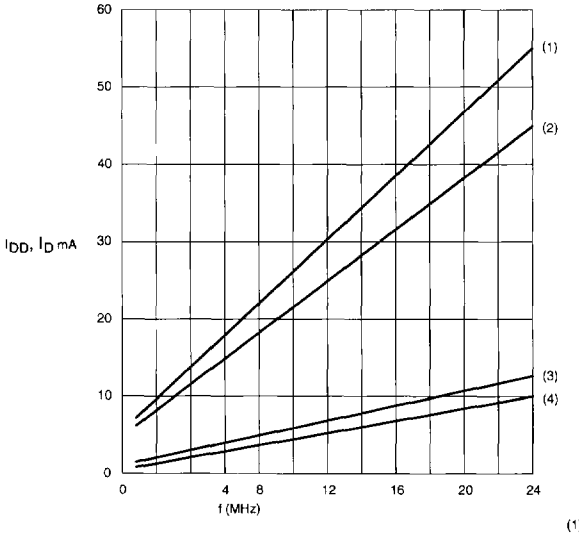
Figure 9. Timing SIO1 (I^2C) Interface



(1) Maximum operating mode; V_{DD} = 6V
(2) Maximum operating mode; V_{DD} = 4V
(3) Maximum idle mode; V_{DD} = 6V
(4) Maximum idle mode; V_{DD} = 4V

NOTE:
These values are valid only within the frequency specifications of the device under test.

Figure 10. 16MHz Version Supply Current (I_{DD}) as a Function of Frequency at XTAL1 (f_{OSC})



(1) Maximum operating mode; V_{DD} = 5.5V
(2) Maximum operating mode; V_{DD} = 4.5V
(3) Maximum idle mode; V_{DD} = 5.5V
(4) Maximum idle mode; V_{DD} = 4.5V

NOTE:
These values are valid only within the frequency specifications of the device under test.

Figure 11. 24MHz Version Supply Current (I_{DD}) as a Function of Frequency at XTAL1 (f_{OSC})

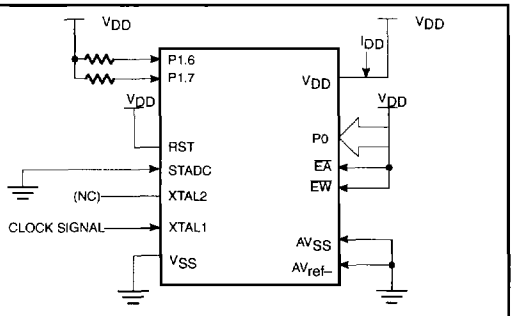


Figure 12. I_{DD} Test Condition, Active Mode
All other pins are disconnected[1]

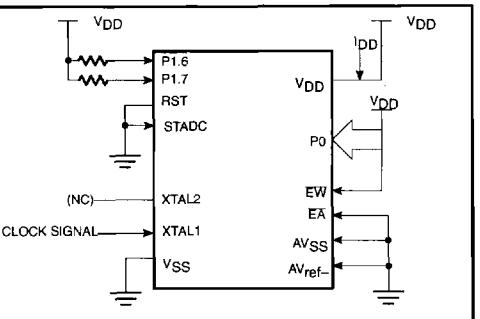


Figure 13. I_{DD} Test Condition, Idle Mode
All other pins are disconnected[2]

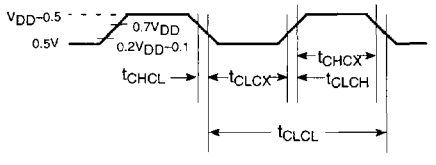


Figure 14. Clock Signal Waveform for I_{DD} Tests in Active and Idle Modes $t_{CLCH} = t_{CHCL} = 5ns$

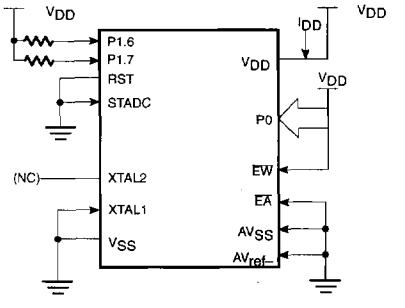


Figure 15. I_{DD} Test Condition, Power Down Mode
All other pins are disconnected. V_{DD} = 2V to 5.5V[3]

NOTES:

1. Active Mode:
   a. The following pins must be forced to V_{DD}: $\overline{EA}$, RST, Port 0, and $\overline{EW}$.
   b. The following pins must be forced to V_{SS}: STADC, AV_{ss}, and AV_{ref-}.
   c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins.
   d. The following pins must be disconnected: XTAL2 and all pins not specified above.
2. Idle Mode:
   a. The following pins must be forced to V_{DD}: Port 0 and $\overline{EW}$.
   b. The following pins must be forced to V_{SS}: RST, STADC, AV_{ss},, AV_{ref-}, and $\overline{EA}$.
   c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
   d. The following pins must be disconnected: XTAL2 and all pins not specified above.
3. Power Down Mode:
   a. The following pins must be forced to V_{DD}: Port 0 and $\overline{EW}$.
   b. The following pins must be forced to V_{SS}: RST, STADC, XTAL1, AV_{ss},, AV_{ref-}, and $\overline{EA}$.
   c. Ports 1.6 and 1.7 should be connected to V_{DD} through resistors of sufficiently high value such that the sink current into these pins cannot exceed the I_{OL1} spec of these pins. These pins must not have logic 0 written to them prior to this measurement.
   d. The following pins must be disconnected: XTAL2 and all pins not specified above.