IS61LPS25632T/D
IS61LPS25636T/D
IS61LPS51218T/D

ISSI®

256K x 32, 256K x 36, 512K x 18 SYNCHRONOUS PIPELINED, SINGLE-CYCLE DESELECT STATIC RAM

DECEMBER 2003

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Linear burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin TQFP package
- Power Supply

  +3.3V V_{DD}

  +3.3V or 2.5 V_{DDQ} (I/O)
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- T Version (three chips selects)
- D Version (two chips selects)

DESCRIPTION

The *ISSI* IS61LPS25632T/D, IS61LPS25636T/D, and IS61LPS51218T/D are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61LPS25632T/D is organized as 262,144 words by 32 bits and the IS61LPS25636T/D is organized as 262,144 words by 36 bits. The IS61LPS51218T/D is organized as 524,288 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. Byte write operation is performed by using byte write enable ($\overline{BWE}$). Input combined with one or more individual byte write signals ($\overline{BWx}$). In addition, Global Write ($\overline{GW}$) is available for writing all bytes at one time, regardless of the byte write controls.

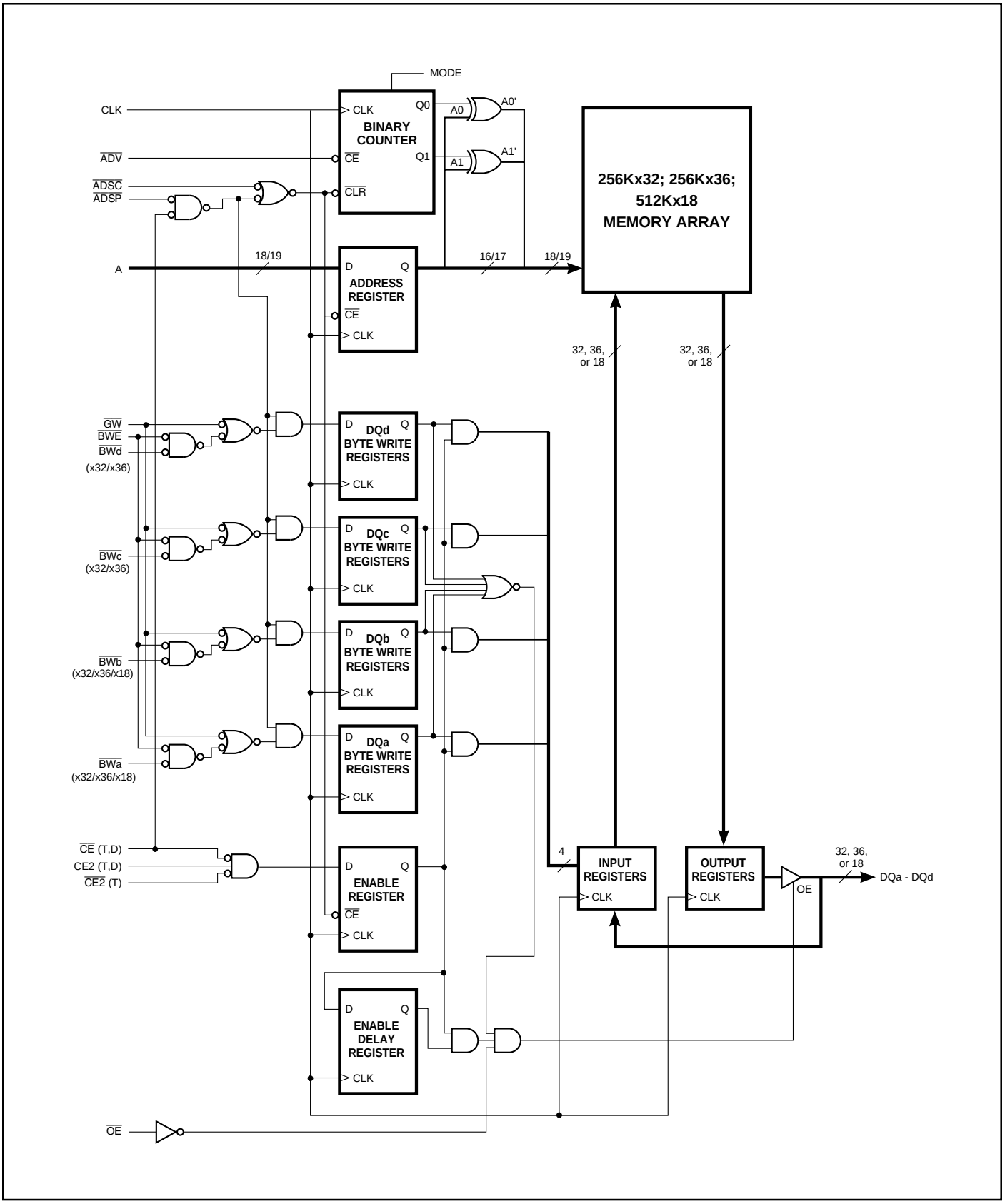
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

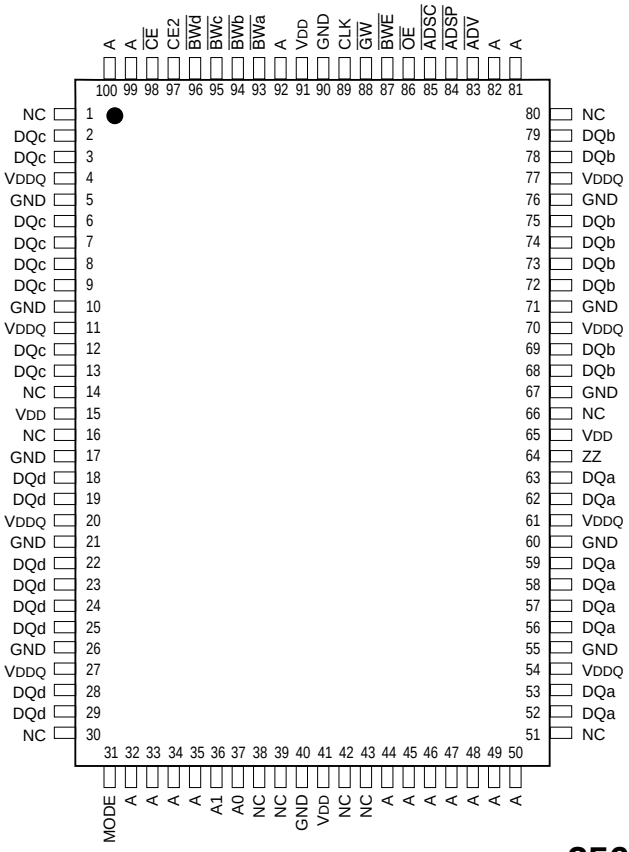
Symbol	Parameter	-200	-166	Units
t_{KQ}	Clock Access Time	3.1	3.5	ns
t_{KC}	Cycle Time	5	6	ns
	Frequency	200	166	MHz

BLOCK DIAGRAM

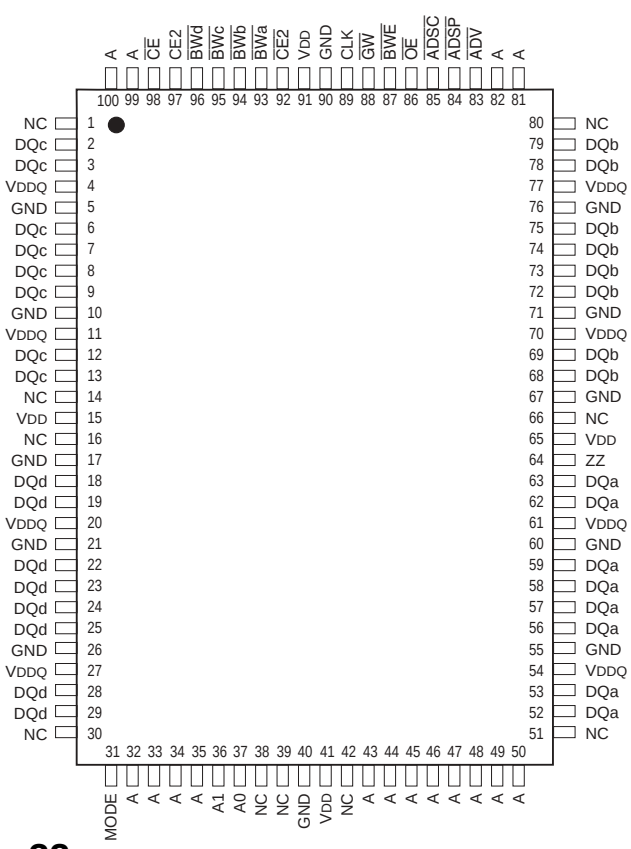


PIN CONFIGURATION

100-Pin TQFP (D Version)



100-Pin TQFP (T Version)



256K x 32

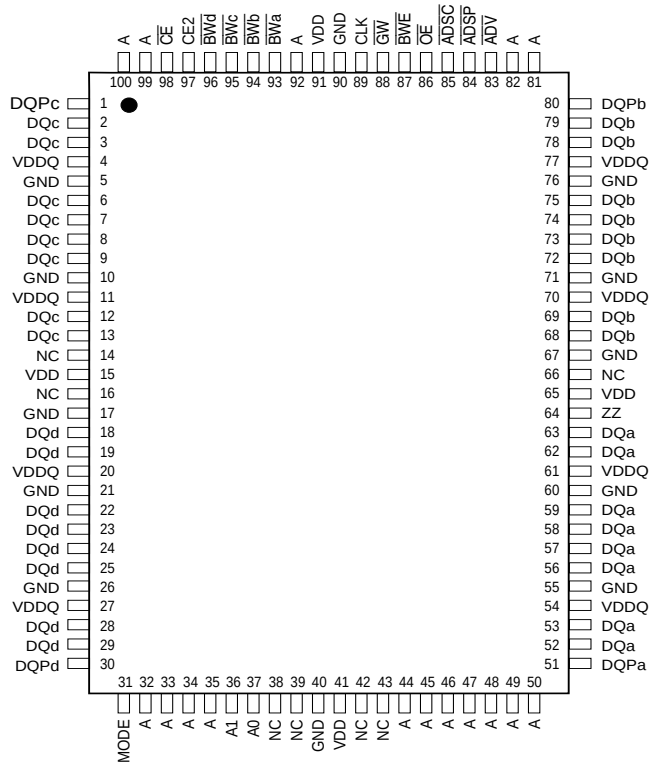
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

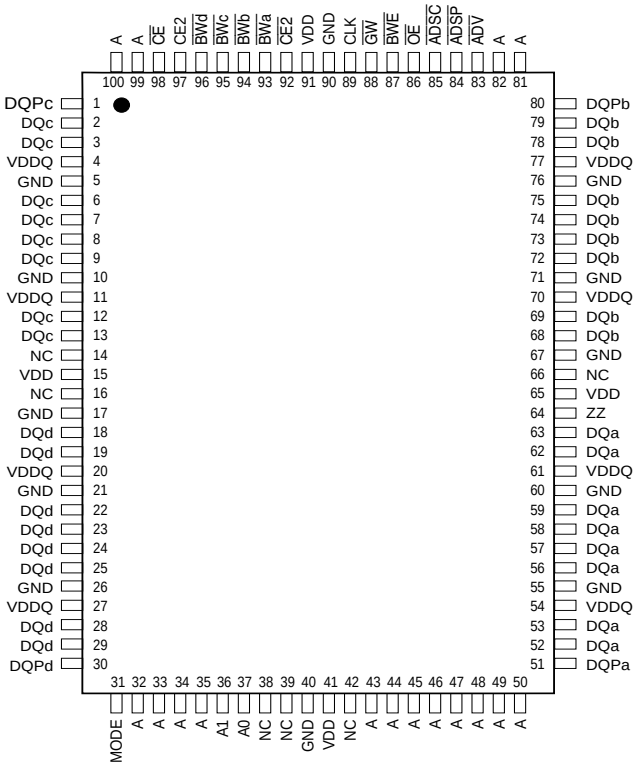
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

100-Pin TQFP (D Version)



100-Pin TQFP (T Version)



256K x 36

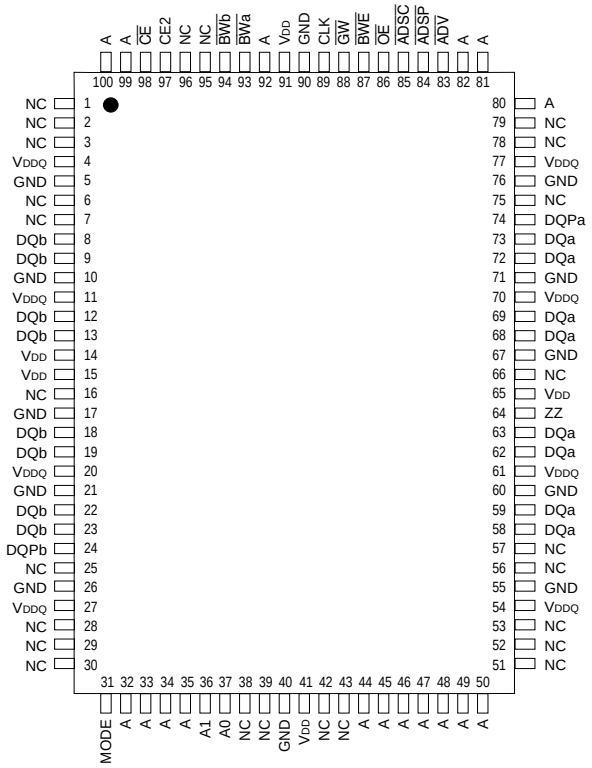
PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

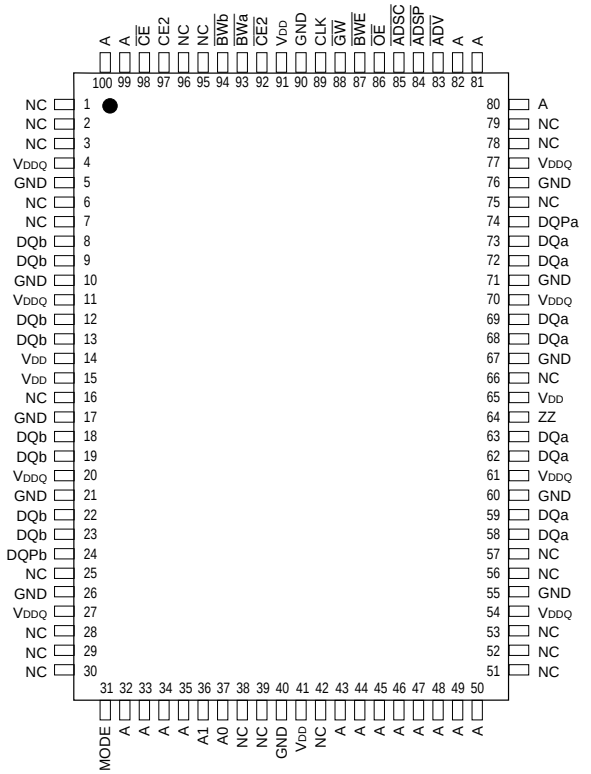
$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

PIN CONFIGURATION

100-Pin TQFP (D Version)



100-Pin TQFP (T Version)



512K x 18

PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BWa}$-$\overline{BWd}$	Individual Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{DD}	+3.3V Power Supply
GND	Ground
V_{DDQ}	Isolated Output Buffer Supply: +3.3V or 2.5V
ZZ	Snooze Enable
DQPa-DQPd	Parity Data I/O

TRUTH TABLE[1-8]

OPERATION	ADDRESS	$\overline{CE}$	$\overline{CE2}$	CE2	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselect Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselect Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
Snooze Mode, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
Write Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
Read Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For $\overline{WRITE}$, L means one or more byte write enable signals ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$ or $\overline{BWd}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BWx}$, $\overline{BWE}$, $\overline{GW}$ HIGH.
3. $\overline{BWa}$ enables WRITEs to DQa's and DQPa. $\overline{BWb}$ enables WRITEs to DQb's and DQPb. $\overline{BWc}$ enables WRITEs to DQc's and DQPc. $\overline{BWd}$ enables WRITEs to DQd's and DQPd. DQPa and DQPb are only available on the x18 and x36 versions. DQPc and DQPd are only available on the x36 version.
4. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

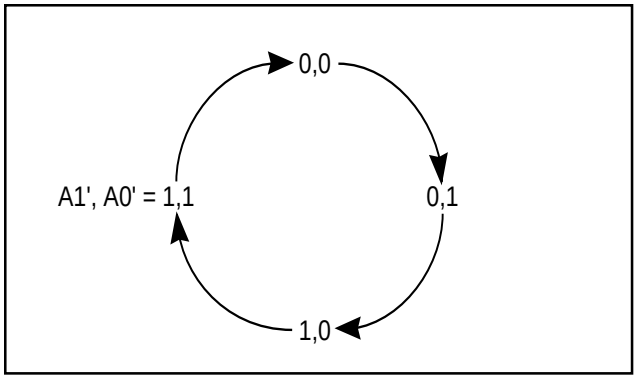
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V ± 5%
			2.5V ± 5%
Industrial	-40°C to +85°C	3.3V ± 5%	3.3V ± 5%
			2.5V ± 5%

LINEAR BURST ADDRESS TABLE (MODE = GND)



INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{DDQ} + 0.5	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{DD} + 0.5	V
V_{DD}	Voltage on V_{DD} Supply Relative to GND	–0.5 to 4.6	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			2.5V (I/O)		3.3V (I/O)		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA (3.3V) I_{OH} = 1.0 mA (2.5V)	2.0	—	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA (3.3V) I_{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	2.0	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	–0.3	0.8	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{DD}[1]	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{DDQ}, $\overline{OE}$ = V_I	–5	5	–5	5	µA

POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	Test Conditions		-200 Max x18	-200 Max x36	-166 Max x18	-166 Max x36/x32	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ V_{IL} or ≥ V_{IH}, Cycle Time ≥ t_{KC} min.	Com.	125	130	120	125	mA
			Ind.	135	140	130	135	
I_{SB}	Standby Current TTL Input	Device Deselected, V_{DD} = Max., All Inputs ≤ V_{IL} or ≥ V_{IH}, ZZ ≤ V_{IL}, f = Max.	Com.	55	55	50	50	mA
			Ind.	60	60	55	55	
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{DD} = Max., V_{IN} ≤ GND + 0.2V or ≥ V_{DD} – 0.2V f = 0	Com.	30	30	30	30	mA
			Ind.	40	40	40	40	

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ V_{DD} – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

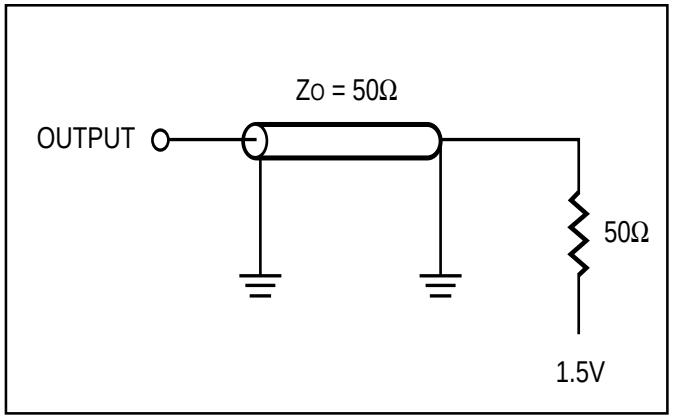


Figure 1

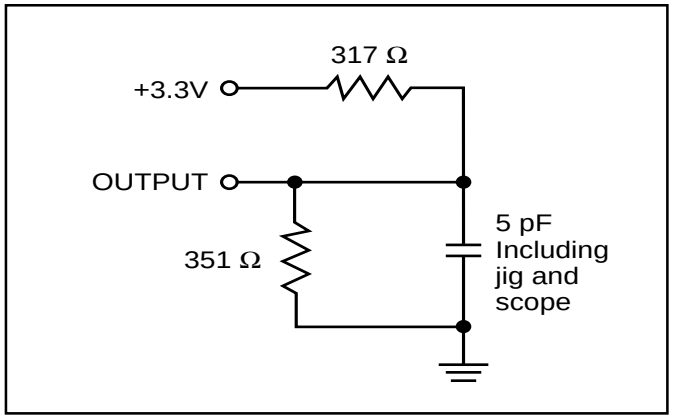


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

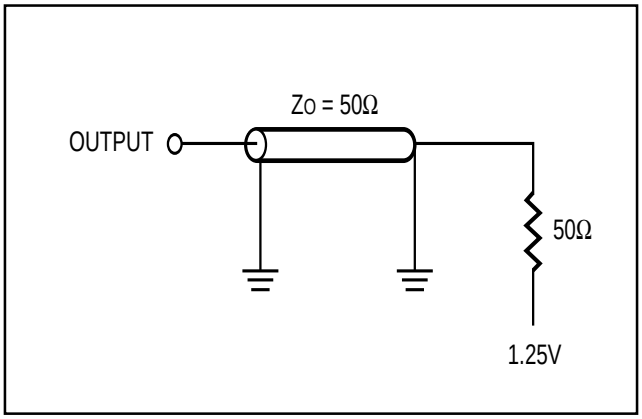


Figure 3

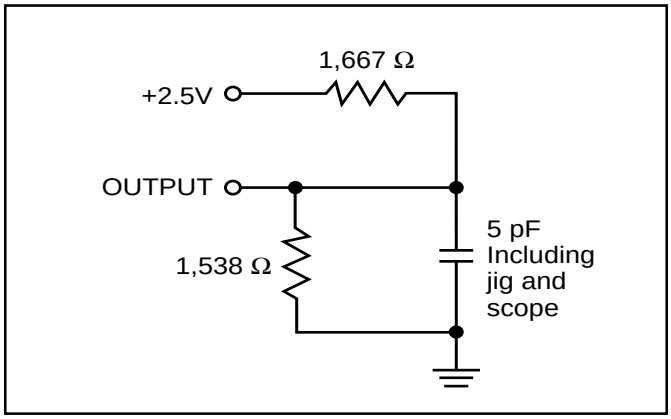


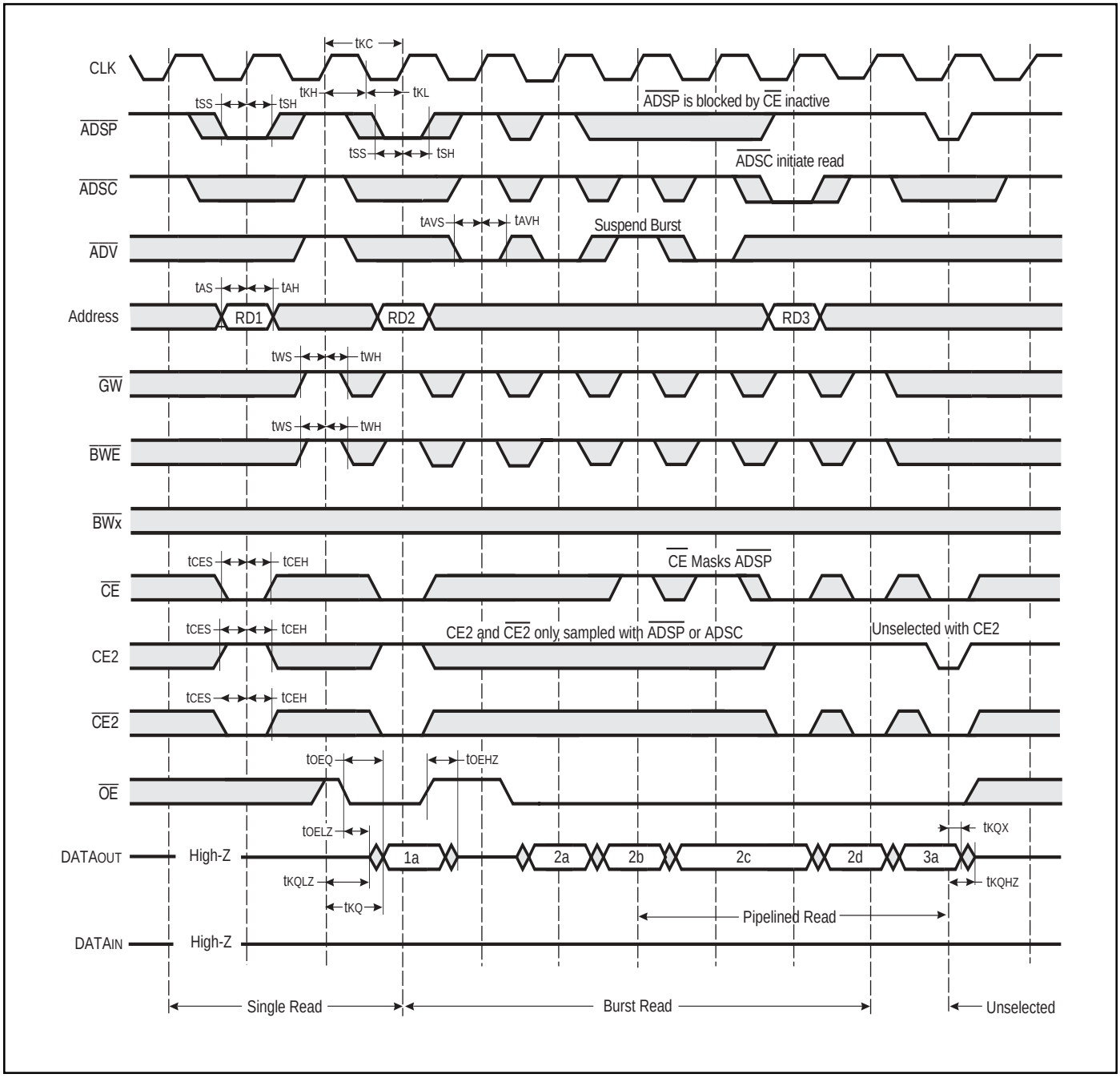
Figure 4

Read/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166 Min.	-166 Max.	-200 Min.	-200 Max.	Unit
f_{MAX}	Clock Frequency	—	166	—	200	ns
t_{KC}	Cycle Time	6	—	5	—	ns
t_{KH}	Clock High Pulse Width	2.3	—	2	—	ns
t_{KL}	Clock Low Pulse Width	2.3	—	2	—	ns
t_{KQ}	Clock Access Time	—	3.5	—	3.1	ns
t_{KQX}(1)	Clock High to Output Invalid	1.5	—	1.0	—	ns
t_{KQLZ}(1,2)	Clock High to Output Low-Z	0	—	0	—	ns
t_{KQHZ}(1,2)	Clock High to Output High-Z	—	3.5	—	3.0	ns
t_{OEQ}	Output Enable to Output Valid	—	3.5	—	3.1	ns
t_{OELZ}(1,2)	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}(1,2)	Output Enable to Output High-Z	—	3.5	—	3.0	ns
t_{AS}	Address Setup Time	1.5	—	1.4	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.4	—	ns
t_{WS}	Write Setup Time	1.5	—	1.4	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.4	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.4	—	ns
t_{AH}	Address Hold Time	0.5	—	0.4	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.4	—	ns
t_{WH}	Write Hold Time	0.5	—	0.4	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.4	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.4	—	ns

Note:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 1,2,3,4.

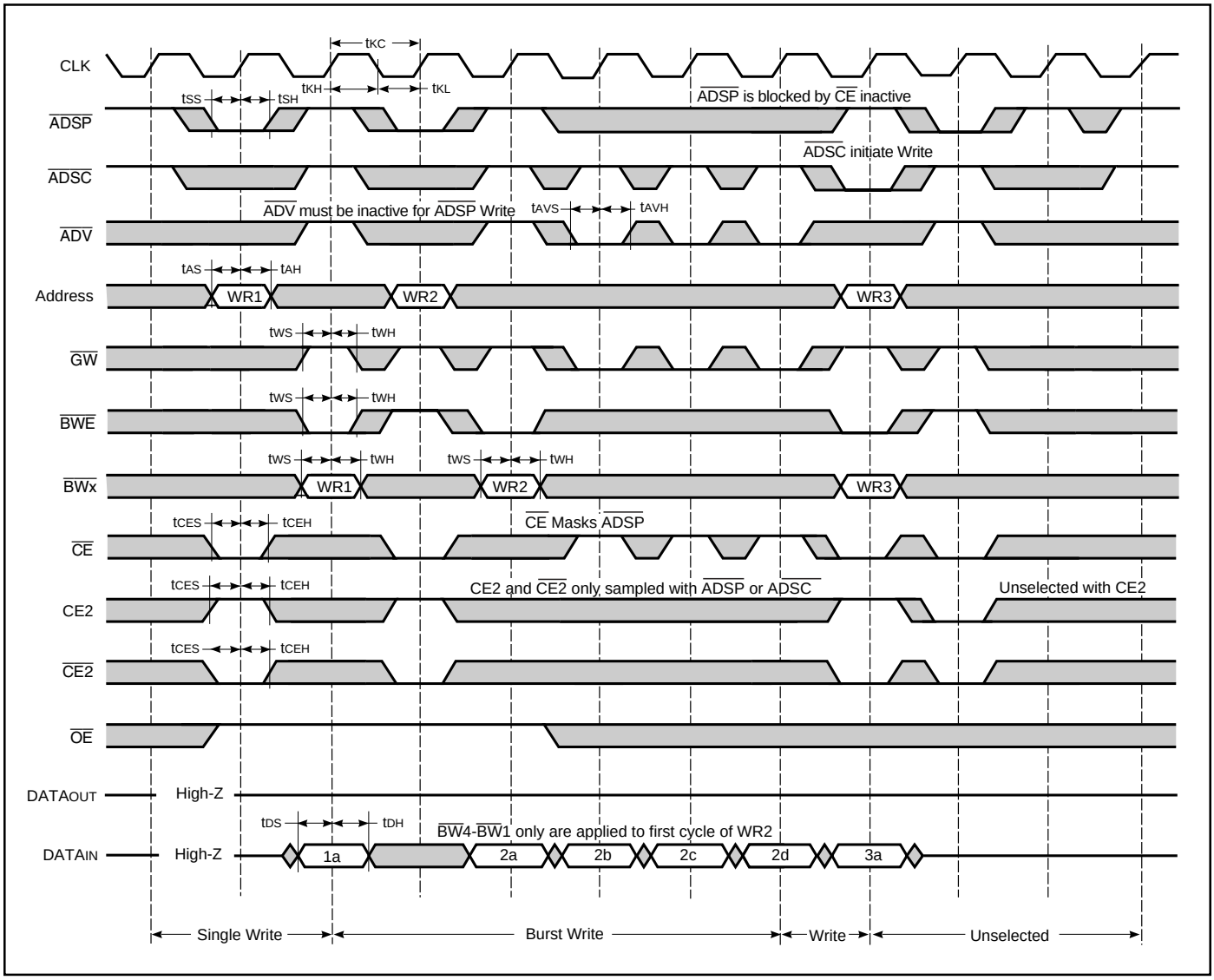
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166 Min.	-166 Max.	-200 Min.	-200 Max.	Unit
t_{KC}	Cycle Time	6	—	5	—	ns
t_{KH}	Clock High Pulse Width	2.3	—	2	—	ns
t_{KL}	Clock Low Pulse Width	2.3	—	2	—	ns
t_{AS}	Address Setup Time	1.5	—	1.4	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.4	—	ns
t_{WS}	Write Setup Time	1.5	—	1.4	—	ns
t_{DS}	Data In Setup Time	1.5	—	1.4	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.4	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.4	—	ns
t_{AH}	Address Hold Time	0.5	—	0.4	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.4	—	ns
t_{DH}	Data In Hold Time	0.5	—	0.4	—	ns
t_{WH}	Write Hold Time	0.5	—	0.4	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.4	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.4	—	ns

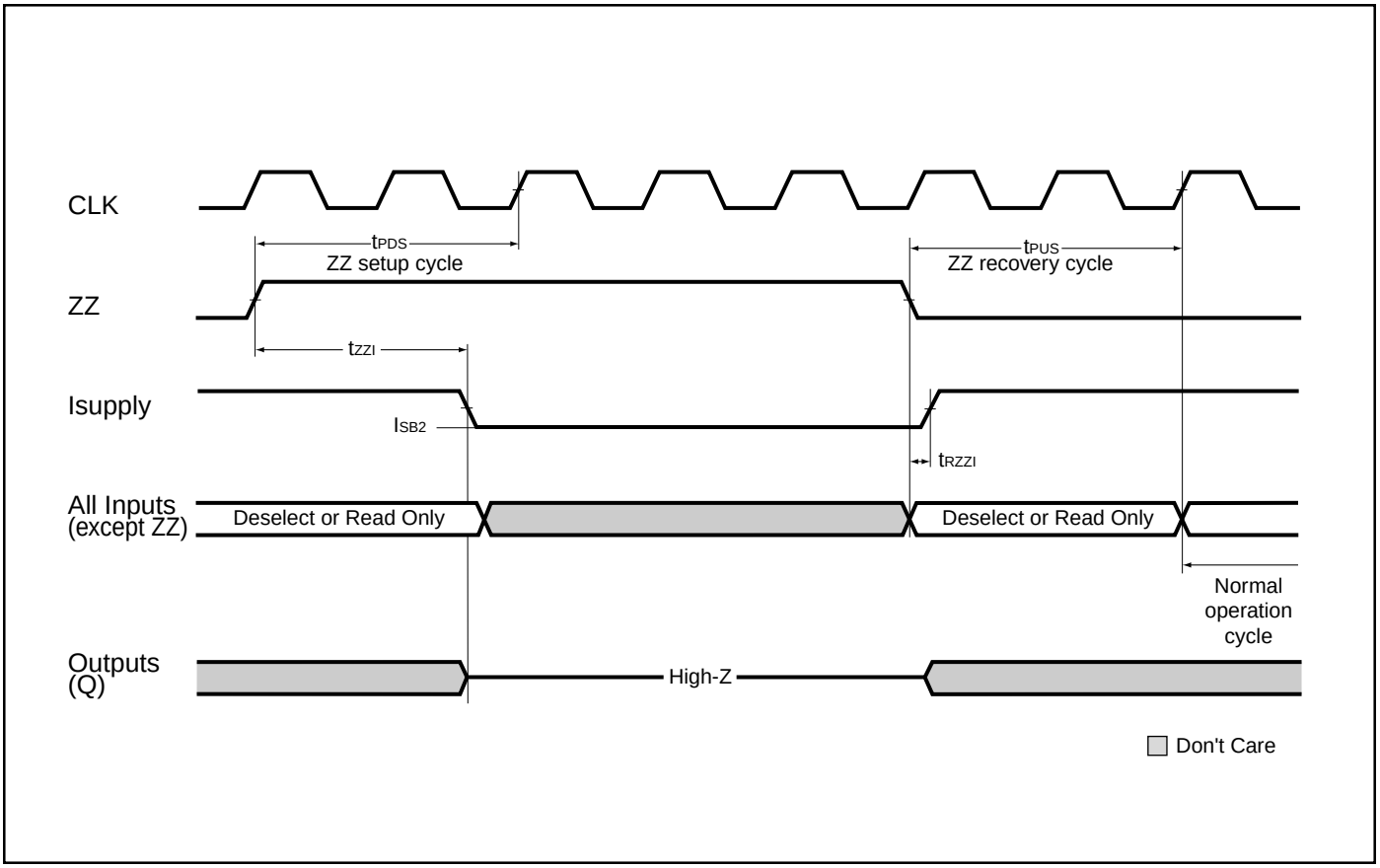
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SNOOZE MODE	ZZ ≥ Vih, Com.	—	30	mA
		ZZ ≥ Vih, Ind.	—	40	
t_{PUS}	ZZ inactive to input sampled		2	—	cycle
t_{ZZI}	ZZ active to SNOOZE current		—	2	cycle
t_{RZZI}	ZZ inactive to exit SNOOZE current		0	—	ns

SNOOZE MODE TIMING



ORDERING INFORMATION: IS61LPS25632

(T Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25632T-166TQ	TQFP

(T Version)
Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25632T-166TQI	TQFP

(D Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25632D-166TQ	TQFP

ORDERING INFORMATION: IS61LPS25636

(T Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25636T-166TQ	TQFP

(T Version)
Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25636T-166TQI	TQFP
200Mhz	IS61LPS25636T-200TQI	TQFP

(D Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25636D-166TQ	TQFP

(D Version)
Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
166Mhz	IS61LPS25636D-166TQI	TQFP

ORDERING INFORMATION: IS61LPS51218

(T Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS51218T-166TQ	TQFP

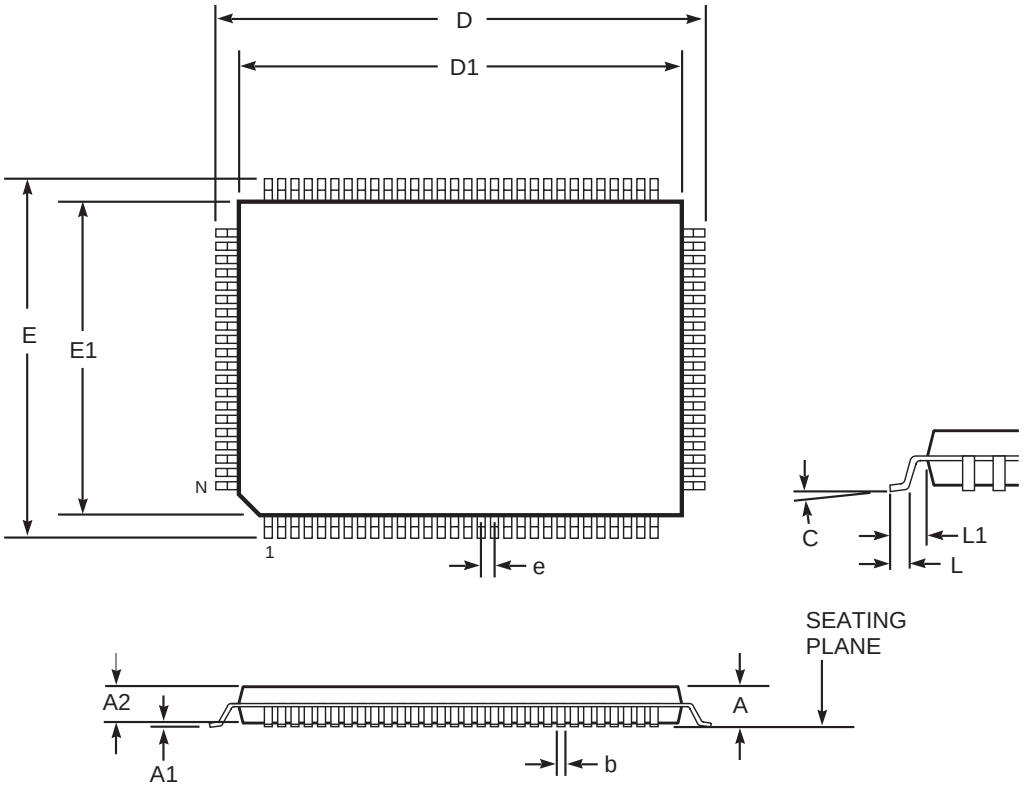
(T Version)
Industrial Range: -40°C to +85°C

Speed	Order Part Number	Package
166Mhz	IS61LPS51218T-166TQI	TQFP

(D Version)
Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166Mhz	IS61LPS51218D-166TQ	TQFP

TQFP (Thin Quad Flat Pack Package)
Package Code: TQ



Thin Quad Flat Pack (TQ)								
	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.								
No. Leads (N)	100				128			
A	—	1.60	—	0.063	—	1.60	—	0.063
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057	1.35	1.45	0.053	0.057
b	0.22	0.38	0.009	0.015	0.17	0.27	0.007	0.011
D	21.90	22.10	0.862	0.870	21.80	22.20	0.858	0.874
D1	19.90	20.10	0.783	0.791	19.90	20.10	0.783	0.791
E	15.90	16.10	0.626	0.634	15.80	16.20	0.622	0.638
E1	13.90	14.10	0.547	0.555	13.90	14.10	0.547	0.555
e	0.65 BSC		0.026 BSC		0.50 BSC		0.020 BSC	
L	0.45	0.75	0.018	0.030	0.45	0.75	0.018	0.030
L1	1.00 REF.		0.039 REF.		1.00 REF.		0.039 REF.	
C	0°	7°	0°	7°	0°	7°	0°	7°

Notes:
1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.