

TSOP  
Commercial Temp  
Industrial Temp

# 128K x 8

## 1Mb Asynchronous SRAM

8 ns  
3.3 V  $V_{DD}$   
Center  $V_{DD}$  and  $V_{SS}$

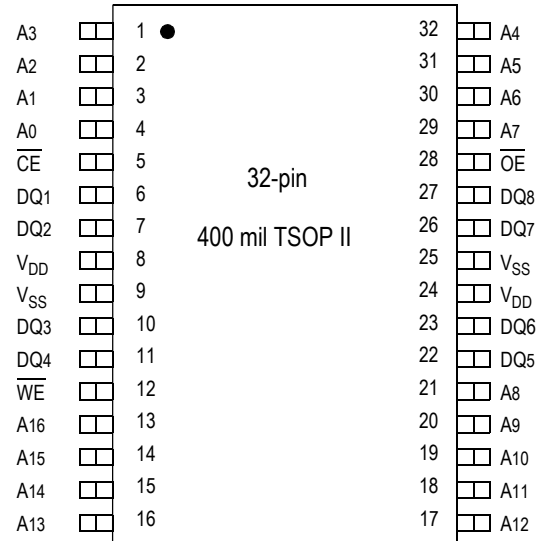
### Features

- Fast access time: 8 ns
- CMOS low power operation: 150 mA at minimum cycle time
- Single 3.3 V  $\pm$  0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}$ C
- Package line up
  - TP: 400 mil, 32-pin TSOP Type II package

### Description

The GS71208 is a high speed CMOS Static RAM organized as 131,072 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS71208 is available in a 400 mil TSOP Type-II package.

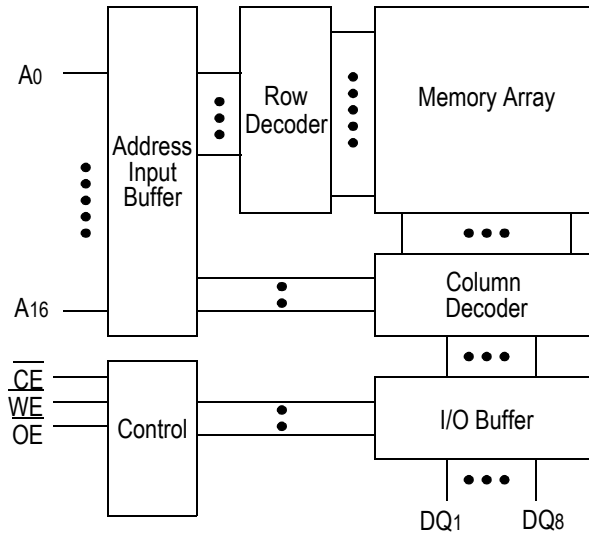
### TSOP-II 128K x 8-Pin Configuration



### Pin Descriptions

Symbol	Description
A <sub>0</sub> –A <sub>16</sub>	Address input
DQ <sub>1</sub> –DQ <sub>8</sub>	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
$V_{DD}$	+3.3 V power supply
$V_{SS}$	Ground
NC	No connect

### Block Diagram



### Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ1 to DQ8	$V_{DD}$ Current
H	X	X	Not Selected	ISB1, ISB2
L	L	H	Read	IDD
L	X	L	Write	
L	H	H	High Z	

Note: X: "H" or "L"

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V <sub>DD</sub>	-0.5 to +4.6	V
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>DD</sub> +0.5 (≤ 4.6 V max.)	V
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5 (≤ 4.6 V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	T <sub>STG</sub>	-55 to 150	°C

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

## Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8	V <sub>DD</sub>	3.135	3.3	3.6	V
Input High Voltage	V <sub>IH</sub>	2.0	—	V <sub>DD</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T <sub>Ac</sub>	0	—	70	°C
Ambient Temperature, Industrial Range	T <sub>AI</sub>	-40	—	85	°C

Note:

1. Input overshoot voltage should be less than V<sub>DD</sub> +2 V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

## Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	5	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0 V	7	pF

Notes:

1. Tested at T<sub>A</sub> = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

**DC I/O Pin Characteristics**

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	$I_{IL}$	$V_{IN} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output Leakage Current	$I_{LO}$	Output High Z $V_{OUT} = 0$ to $V_{DD}$	-1 $\mu$ A	1 $\mu$ A
Output High Voltage	$V_{OH}$	$I_{OH} = -4$ mA	2.4	—
Output Low Voltage	$V_{OL}$	$I_{LO} = +4$ mA	—	0.4 V

**Power Supply Currents**

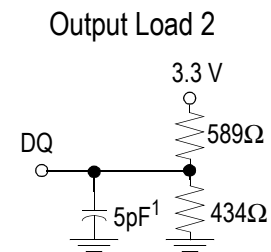
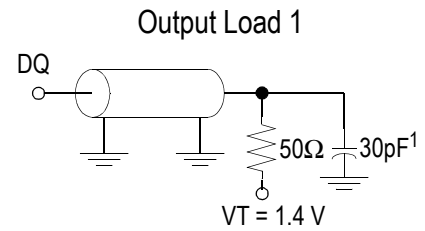
Parameter	Symbol	Test Conditions	0 to 70°C	-40 to 85°C
			8 ns	8 ns
Operating Supply Current	$I_{DD}(\max)$	$\overline{CE} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0$ mA	150 mA	160 mA
Standby Current	$I_{SB1}(\max)$	$\overline{CE} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	55 mA	65 mA
Standby Current	$I_{SB2}(\max)$	$CE \geq V_{DD} - 0.2$ V All other inputs $\geq V_{DD} - 0.2$ V or $\leq 0.2$ V	15 mA	25 mA

## AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4\text{ V}$
Input low level	$V_{IL} = 0.4\text{ V}$
Input rise time	$t_r = 1\text{ V/ns}$
Input fall time	$t_f = 1\text{ V/ns}$
Input reference level	1.4 V
Output reference level	1.4 V
Output load	<b>Fig. 1&amp; 2</b>

Note:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$



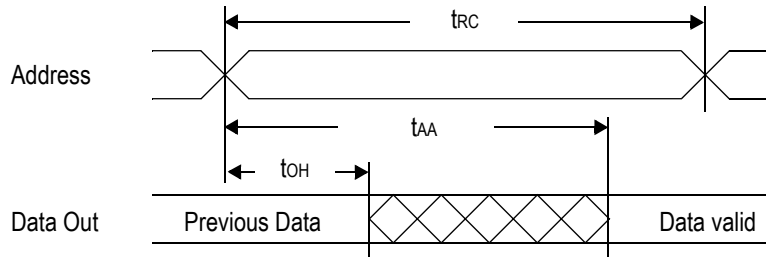
## AC Characteristics

### Read Cycle

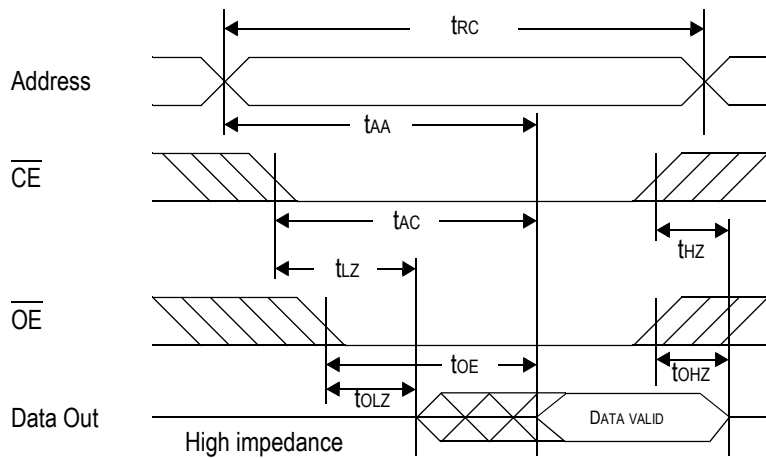
Parameter	Symbol	-8		Unit
		Min	Max	
Read cycle time	$t_{RC}$	8	—	ns
Address access time	$t_{AA}$	—	8	ns
Chip enable access time ( $\overline{CE}$ )	$t_{AC}$	—	8	ns
Output enable to output valid ( $\overline{OE}$ )	$t_{OE}$	—	3.5	ns
Output hold from address change	$t_{OH}$	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	$t_{LZ}^*$	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	$t_{OLZ}^*$	0	—	ns
Chip disable to output in High Z ( $\overline{CE}$ )	$t_{HZ}^*$	—	4	ns
Output disable to output in High Z ( $\overline{OE}$ )	$t_{OHZ}^*$	—	3.5	ns

\* These parameters are sampled and are not 100% tested

Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$



Read Cycle 2:  $\overline{WE} = V_{IH}$

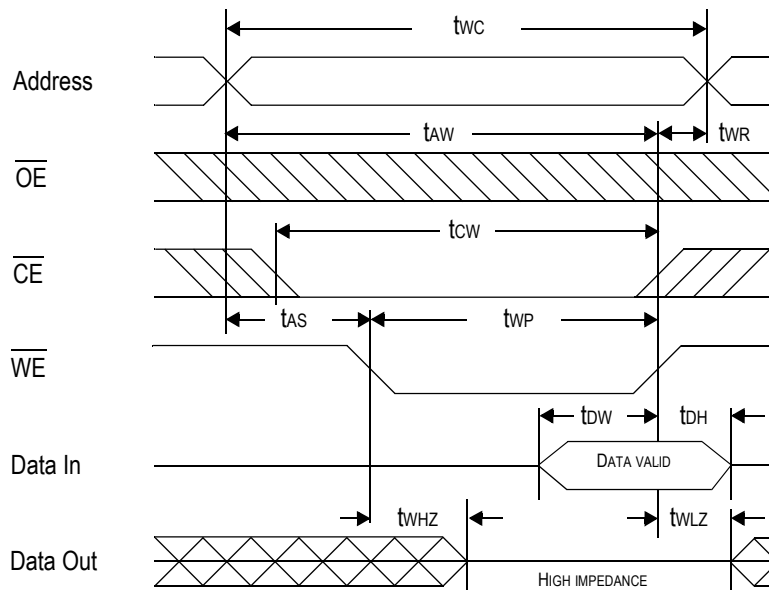


**Write Cycle**

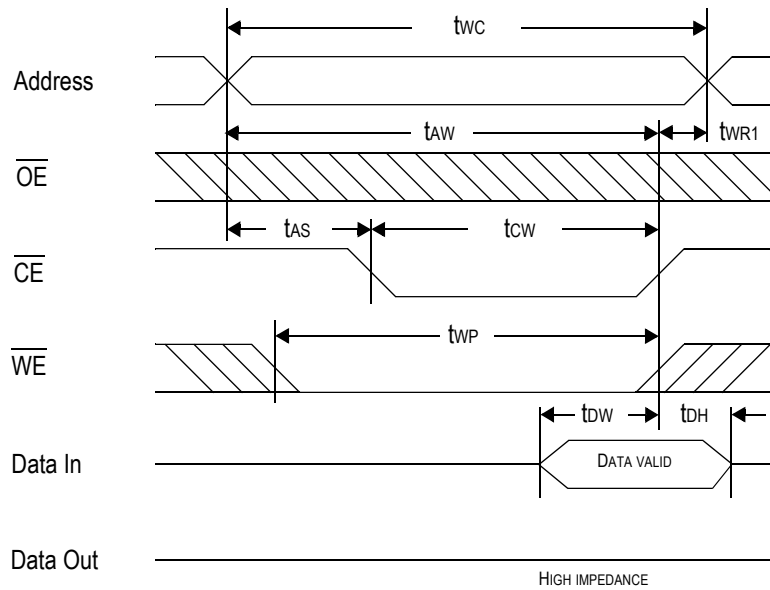
Parameter	Symbol	-8		Unit
		Min	Max	
Write cycle time	tWC	8	—	ns
Address valid to end of write	tAW	5.5	—	ns
Chip enable to end of write	tCW	5.5	—	ns
Data set up time	tDW	4	—	ns
Data hold time	tDH	0	—	ns
Write pulse width	tWP	5.5	—	ns
Address set up time	tAS	0	—	ns
Write recovery time ( $\overline{WE}$ )	tWR	0	—	ns
Write recovery time ( $\overline{CE}$ )	tWR1	0	—	ns
Output Low Z from end of write	tWLZ*	3	—	ns
Write to output in High Z	tWHZ*	—	3.5	ns

\* These parameters are sampled and are not 100% tested

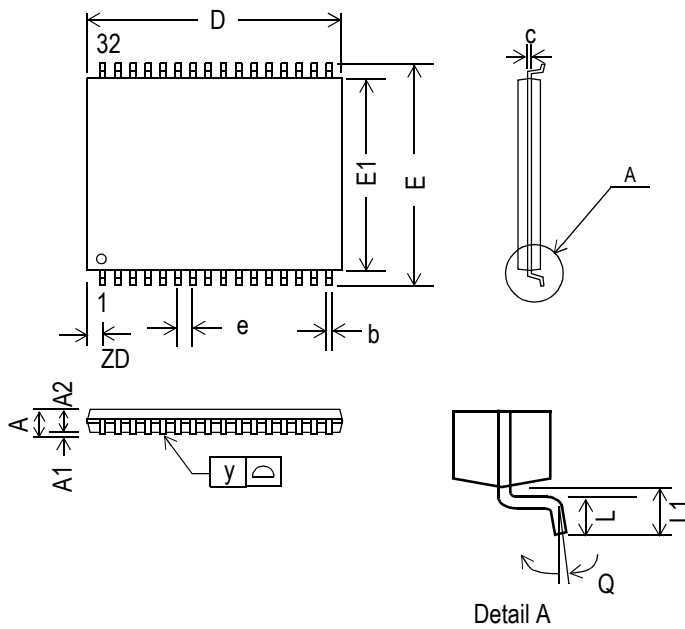
**Write Cycle 1:  $\overline{WE}$  control**



**Write Cycle 2:  $\overline{CE}$  control**





**32-Pin TSOP-II, 400mil**


Symbol	Dimension in inch			Dimension in mm		
	min	nom	max	min	nom	max
A	0.039	—	0.05	—	—	1.27
A1	0.002	—	0.006	0.01	—	0.15
A2	0.037	0.040	0.045	0.90	1.02	1.14
b	0.012	0.016	0.018	0.30	0.40	0.45
c	0.0047	0.0051	0.0062	0.12	0.13	0.16
D	0.820	0.825	0.830	20.82	20.95	21.08
ZD	—	0.037	—	—	0.95	—
E	0.455	0.463	0.471	11.56	11.76	11.96
E1	0.395	0.400	0.405	10.03	10.16	10.29
e	—	0.05	—	—	1.27	—
L	0.017	0.020	0.023	0.40	0.50	0.60
L1	0.024	0.031	0.039	0.60	0.80	1.00
y	0.00	—	0.003	0.00	—	0.76
Q	0°	—	5°	0°	—	5°

**Note:**

1. Dimension D includes mold flash, protrusions or gate burrs.
2. Dimension E does not include interlead flash.
3. Controlling dimension: mm

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**Ordering Information**

<b>Part Number</b> *	<b>Package</b>	<b>Access Time</b>	<b>Temp. Range</b>	<b>Status</b>
GS71208TP-8	400 mil TSOP-II	8 ns	Commercial	

\* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example:  
GS71208TP-8T

**Revision History**

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
1.00 12/1999/1.01 12/1999	Content	1. Added TP package to 71208
GS71208Rev1.01 12/1999KRev 1.01 2/2000L	Format/Content	<ul style="list-style-type: none"> <li>• GSI LogoAdded Dimension D to 32 pin 400 ml TSOP II Package.</li> </ul>
71208_r1_01; 71208_r1_02	Format/Content	<ul style="list-style-type: none"> <li>• Updated format to comply with Technical Publications standard</li> <li>• Specifically noted that numbers in Power Supply Currents table are worst case scenario</li> </ul>
71208_r1_02; 71208_r1_03	Content	<ul style="list-style-type: none"> <li>• Removed all references to other parts except 71208TP-8</li> </ul>