

**DESCRIPTION:**

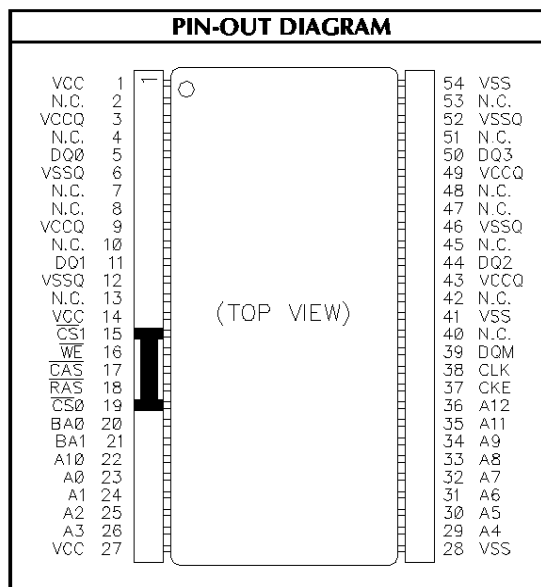
The *M-Densus* series is a family of interchangeable memory modules. The 512 Megabit SDRAM is a member of this family which utilizes the new and innovative space saving TSO P stacking technology. The modules are constructed with 64 Meg x 4 SDRAMs.

This 256 Megabit based *M-Densus* module, the DPSD128MX4WY5 has been designed to fit in the same footprint as the 64 Meg x 4 SDRAM TSOP monolithic and 64 Megabit SDRAM based family of *M-Densus* modules. This allows the memory board designer to upgrade the memory in their products without redesigning the memory board, thus saving time and money.

**FEATURES:**

- Configuration Available:  
128 Meg x 4 (2 Banks of 16M x 4 x 4 bits)
- Clock Frequency:  
66<sup>[1]</sup>, 83<sup>[1]</sup>, 100, 125<sup>[2]</sup>, 133<sup>[2]</sup> MHz (max.)
- PC100 and PC133 Compatible
- 3.3V Supply
- LVTTTL Compatible I/O
- Four Bank Operation
- Programmable Burst Type, Burst Length, and CAS Latency
- 8192 Cycles / 64 ms
- Auto and Self Refresh
- Package: TSOP Leadless Stack

NOTES: [1] Available in Industrial Temperature Ranges Only.  
[2] Available in Commercial Temperature Range Only.



PIN NAMES	
A0 - A12	Row Address: A0 - A12 Column Address: A0 - A9, A11
BA0, BA1	Bank Select Address
DQ0 - DQ3	Data In / Data Out
CAS	Column Address Strobes
RAS	Row Address Enables
WE	Data Write Enable
DQM	Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
CS0-CS1	Chip Selects
Vcc/Vss	Power Supply/Ground
Vccq/Vssq	Data Output Power/Ground
N.C.	No Connect

