

FEATURES

- 5 kV rms signal isolated CAN transceiver**
- 5 V or 3.3 V operation on V_{DD1}**
- 5 V operation on V_{DD2}**
- $V_{DD2SENSE}$ to detect loss of power on V_{DD2}**
- Complies with ISO 11898 standard**
- High speed data rates of up to 1 Mbps**
- Short-circuit protection on CANH and CANL against shorts to power/ground in 24 V systems**
- Unpowered nodes do not disturb the bus**
- Connect 110 or more nodes on the bus**
- Thermal shutdown protection**
- High common-mode transient immunity: >25 kV/ μ s**
- Safety and regulatory approvals**
 - UL recognition (pending)
 - 5000 V rms for 1 minute per UL 1577
 - VDE Certificates of Conformity (pending)
 - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
 - $V_{IORM} = 846$ V peak
- Industrial operating temperature range: -40°C to $+125^{\circ}\text{C}$**
- Wide-body, 16-lead SOIC package**

APPLICATIONS

- CAN data buses
- Industrial field networks

GENERAL DESCRIPTION

The ADM3054 is a 5 kV rms signal isolated controller area network (CAN) physical layer transceiver. The ADM3054 complies with the ISO 11898 standard.

The device employs Analog Devices, Inc., iCoupler® technology to combine a 3-channel isolator and a CAN transceiver into a single package. The logic side of the device is powered with a single 3.3 V or 5 V supply on V_{DD1} and the bus side uses a single 5 V supply on V_{DD2} only. Loss of power on the bus side (V_{DD2}) can be detected by an integrated $V_{DD2SENSE}$ signal.

The ADM3054 creates an isolated interface between the CAN protocol controller and the physical layer bus. It is capable of running at data rates of up to 1 Mbps.

The device has integrated protection on the bus pins, CANH and CANL against shorts to power/ground in 24 V systems.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where the bus might be shorted to ground or power terminals. The part is fully specified over the industrial temperature range and is available in a 16-lead, wide-body SOIC package.

FUNCTIONAL BLOCK DIAGRAM

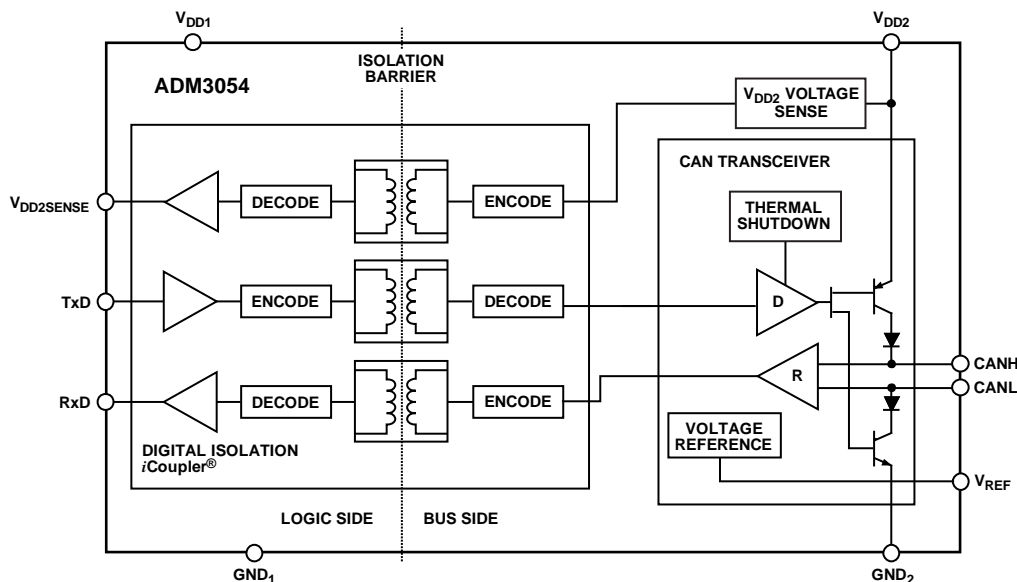


Figure 1

10274-001

Rev. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Typical Performance Characteristics	9
Applications.....	1	Test Circuits and Switching Characteristics.....	13
General Description	1	Theory of Operation	15
Functional Block Diagram	1	CAN Transceiver Operation	15
Revision History	2	Thermal Shutdown	15
Specifications.....	3	Truth Tables.....	15
Timing Specifications	4	Electrical Isolation.....	16
Regulatory Information.....	5	Magnetic Field Immunity	17
Insulation and Safety-Related Specifications	5	Applications Information	18
VDE 0884 Insulation Characteristics (Pending).....	6	Typical Applications.....	18
Absolute Maximum Ratings	7	Packaging and Ordering Information	20
ESD Caution.....	7	Outline Dimensions	20
Pin Configuration and Function Descriptions.....	8	Ordering Guide	20

REVISION HISTORY

10/11—Revision 0: Initial Version

SPECIFICATIONS

Each voltage is relative to its respective ground, $3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
Power Supply Current Logic Side						
TxD/RxD Data Rate 1 Mbps	I_{DD1}		2.5	3.0	mA	
Power Supply Current Bus Side						
Recessive State	I_{DD2}			10	mA	$R_L = 60\ \Omega$, see Figure 28
Dominant State				75	mA	$R_L = 60\ \Omega$, see Figure 28
TxD/RxD Data Rate 1 Mbps				55	mA	$R_L = 60\ \Omega$, see Figure 28
DRIVER						
Logic Inputs						
Input Voltage High	V_{IH}	$0.7 V_{DD1}$			V	TxD
Input Voltage Low	V_{IL}			$0.25 V_{DD1}$	V	TxD
CMOS Logic Input Currents	I_{IH}, I_{IL}			500	μA	TxD
Differential Outputs						
Recessive Bus Voltage	V_{CANL}, V_{CANH}	2.0		3.0	V	$V_{TxD} = \text{high}$, $R_L = \infty$, see Figure 22
CANH Output Voltage	V_{CANH}	2.75		4.5	V	$V_{TxD} = \text{low}$, see Figure 22
CANL Output Voltage	V_{CANL}	0.5		2.0	V	$V_{TxD} = \text{low}$, see Figure 22
Differential Output Voltage	V_{OD}	1.5		3.0	V	$V_{TxD} = \text{low}$, $R_L = 45\ \Omega$, see Figure 22
Short-Circuit Current, CANH	I_{SCCANH}	-500		+50	mV	$V_{TxD} = \text{high}$, $R_L = \infty$, see Figure 22
Short-Circuit Current, CANL	I_{SCCANL}		-100	-200	mA	$V_{CANH} = -5\text{ V}$
					mA	$V_{CANH} = -36\text{ V}$
					mA	$V_{CANL} = 36\text{ V}$
RECEIVER						
Differential Inputs						
Differential Input Voltage Recessive	V_{IDR}	-1.0		+0.5	V	$-2\text{ V} < V_{CANL}, V_{CANH} < 7\text{ V}$, see Figure 24, $C_L = 15\text{ pF}$
		-1.0		+0.4	V	$-7\text{ V} < V_{CANL}, V_{CANH} < 12\text{ V}$, see Figure 24, $C_L = 15\text{ pF}$
Differential Input Voltage Dominant	V_{IDD}	0.9		5.0	V	$-2\text{ V} < V_{CANL}, V_{CANH} < 7\text{ V}$, see Figure 24, $C_L = 15\text{ pF}$
		1.0		5.0	V	$-7\text{ V} < V_{CANL}, V_{CANH} < 12\text{ V}$, see Figure 24, $C_L = 15\text{ pF}$
Input Voltage Hysteresis	V_{HYS}		150		mV	See Figure 25
CANH, CANL Input Resistance	R_{IN}	5		25	k Ω	
Differential Input Resistance	R_{DIFF}	20		100	k Ω	
Logic Outputs						
Output Voltage Low	V_{OL}		0.2	0.4	V	$I_{OUT} = 1.5\text{ mA}$
Output Voltage High	V_{OH}	$V_{DD1} - 0.3$	$V_{DD1} - 0.2$		V	$I_{OUT} = -1.5\text{ mA}$
Short-Circuit Current	I_{OS}	7		85	mA	$V_{OUT} = \text{GND}_1$ or V_{DD1}
VOLTAGE REFERENCE						
Reference Output Voltage	V_{REF}	2.025		3.025	V	$ I_{REF} = 50\ \mu\text{A}$
V_{DD2} VOLTAGE SENSE						
$V_{DD2SENSE}$ Output Voltage Low	V_{OL}		0.2	0.4	V	$I_{OSENSE} = 1.5\text{ mA}$
$V_{DD2SENSE}$ Output Voltage High	V_{OH}	$V_{DD1} - 0.3$	$V_{DD1} - 0.2$		V	$I_{OSENSE} = -1.5\text{ mA}$
Bus Voltage Sense Threshold Voltage	$V_{TH(SENSE)}$	2.0		2.5	V	V_{DD2}
COMMON-MODE TRANSIENT IMMUNITY¹						
		25			kV/ μs	$V_{CM} = 1\text{ kV}$, transient, magnitude = 800 V

¹ CM is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

Each voltage is relative to its respective ground, $3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$. $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER						
Maximum Data Rate		1			Mbps	
Propagation Delay TxD On to Bus Active	t_{onTxD}			90	ns	$R_L = 60\ \Omega$, $C_L = 100\ \text{pF}$, see Figure 23 and Figure 27
Propagation Delay TxD Off to Bus Inactive	t_{offTxD}			120	ns	$R_L = 60\ \Omega$, $C_L = 100\ \text{pF}$, see Figure 23 and Figure 27
RECEIVER						
Propagation Delay TxD On to Receiver Active	t_{onRxD}			200	ns	$R_L = 60\ \Omega$, $C_L = 100\ \text{pF}$, see Figure 23 and Figure 27
Propagation Delay TxD Off to Receiver Inactive	t_{offRxD}			250	ns	$R_L = 60\ \Omega$, $C_L = 100\ \text{pF}$, see Figure 23 and Figure 27
POWER-UP						
Enable Time, V_{DD2} High to $V_{DD2\text{SENSE}}$ Low	t_{SE}			300	μs	See Figure 26
Disable Time, V_{DD2} Low to $V_{DD2\text{SENSE}}$ High	t_{SD}			10	ms	See Figure 26

REGULATORY INFORMATION (PENDING)

Table 3. ADM3054 Approvals (Pending)

Organization	Approval Type	Notes
UL	To be recognized under the component recognition program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM3054 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second
VDE	To be certified according to DIN V VDEV 0884-10 (VDEV 0884-10): 2006-12	In accordance with DIN V VDE V 0884-10, each ADM3054 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC)

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (External Clearance)	L(I01)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303-1
Isolation Group		IIIa		Material group (DIN VDE 0110)

VDE 0884 INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

Table 5.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
CLASSIFICATIONS Installation Classification per DIN VDE 0110 for Rated Mains Voltage ≤150 V rms ≤300 V rms ≤400 V rms Climatic Classification Pollution Degree	DIN VDE 0110		I to IV I to III I to II 40/125/21 2	
VOLTAGE Maximum Working Insulation Voltage Input-to-Output Test Voltage, Method B1 Input-to-Output Test Voltage, Method A After Environmental Tests, Subgroup 1 After Input and/or Safety Test, Subgroup 2/Subgroup 3): Highest Allowable Overvoltage	$V_{IORM} \times 1.875 = V_{PRV}$, 100% production tested, $t_m = 1$ sec, partial discharge < 5 pC $V_{IORM} \times 1.6 = V_{PRV}$, $t_m = 60$ sec, partial discharge < 5 pC $V_{IORM} \times 1.2 = V_{PRV}$, $t_m = 60$ sec, partial discharge < 5 pC	V_{IORM} V_{PR} V_{PR} V_{PR} V_{TR}	846 1590 1357 1018 6000	V peak V peak V peak V peak V peak
SAFETY LIMITING VALUES Case Temperature Input Current Output Current Insulation Resistance at T_s		T_s $I_{S, INPUT}$ $I_{S, OUTPUT}$ R_s	150 265 335 $>10^9$	°C mA mA Ω

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted. Each voltage is relative to its respective ground.

Table 6.

Parameter	Rating
V_{DD1}, V_{DD2} Digital Input Voltage	-0.5 V to +6 V
TxD Digital Output Voltage	-0.5 V to $V_{DD1} + 0.5$ V
RxD	-0.5 V to $V_{DD1} + 0.5$ V
$V_{DD2SENSE}$	-0.5 V to $V_{DD1} + 0.5$ V
CANH, CANL	-36 V to +36 V
V_{REF}	-0.5 V to +6 V
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-55°C to +150°C
ESD (Human Body Model)	± 3.5 kV
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
θ_{JA} Thermal Impedance	53°C/W
T_J Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

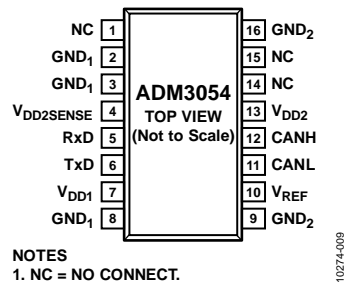


Figure 2. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. This pin remains unconnected.
2	GND ₁	Ground (Logic Side).
3	GND ₁	Ground (Logic Side).
4	V _{DD2SENSE}	V _{DD2} Voltage Sense. A low level on V _{DD2SENSE} indicates that power is connected on V _{DD2} . A high level on V _{DD2SENSE} indicates a loss of power on V _{DD2} .
5	RxD	Receiver Output Data.
6	TxD	Driver Input Data.
7	V _{DD1}	Power Supply (Logic Side); 3.3 V or 5 V. A decoupling capacitor to GND ₁ is required; a capacitor value between 0.01 μF and 0.1 μF is recommended.
8	GND ₁	Ground (Logic Side).
9	GND ₂	Ground (Bus Side).
10	V _{REF}	Reference Voltage Output.
11	CANL	Low Level CAN Voltage Input/Output.
12	CANH	High Level CAN Voltage Input/Output.
13	V _{DD2}	Power Supply (Bus Side); 5 V. A decoupling capacitor to GND ₂ is required; a capacitor value of 0.1 μF is recommended.
14	NC	No Connect. This pin remains unconnected.
15	NC	No Connect. This pin remains unconnected.
16	GND ₂	Ground (Bus Side).

TYPICAL PERFORMANCE CHARACTERISTICS

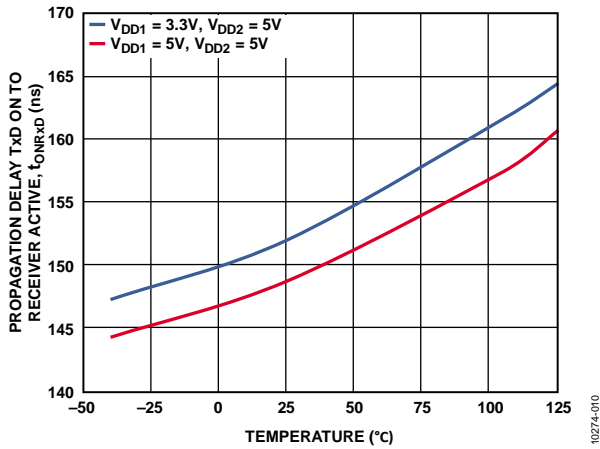


Figure 3. Propagation Delay from TxD On to Receiver Active vs. Temperature

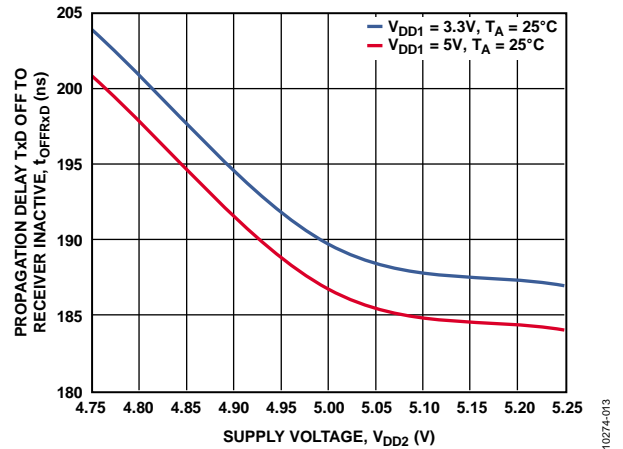


Figure 6. Propagation Delay from TxD Off to Receiver Inactive vs. Supply Voltage, V_{DD2}

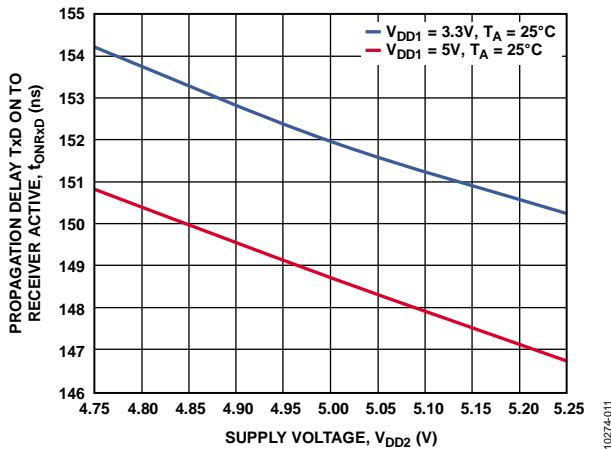


Figure 4. Propagation Delay from TxD On to Receiver Active vs. Supply Voltage, V_{DD2}

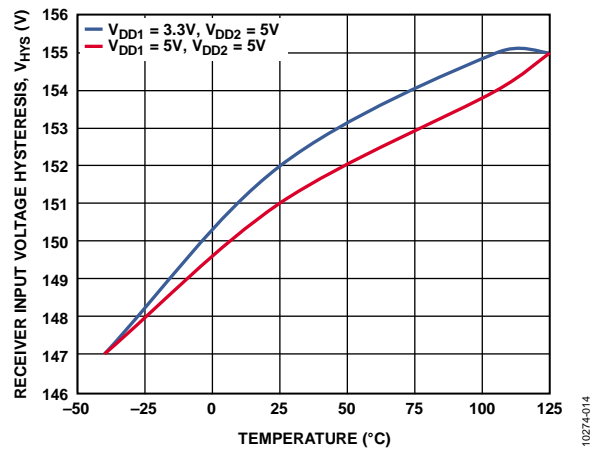


Figure 7. Receiver Input Hysteresis vs. Temperature

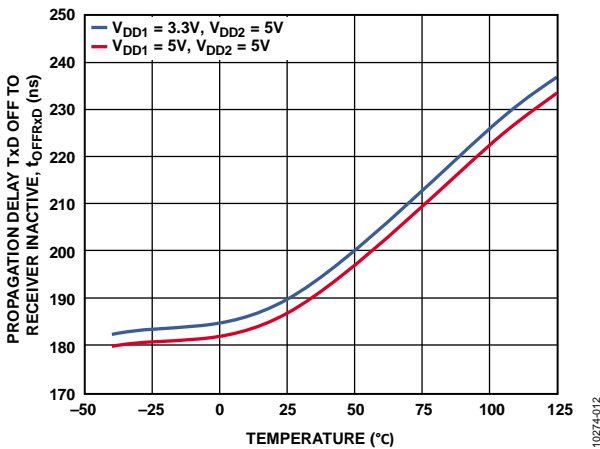


Figure 5. Propagation Delay from TxD Off to Receiver Inactive vs. Temperature

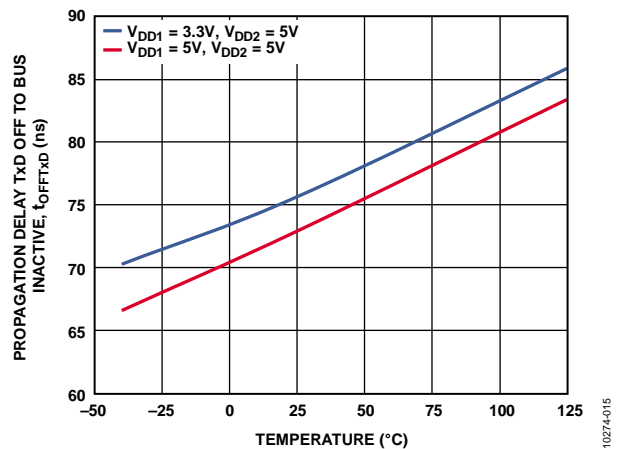
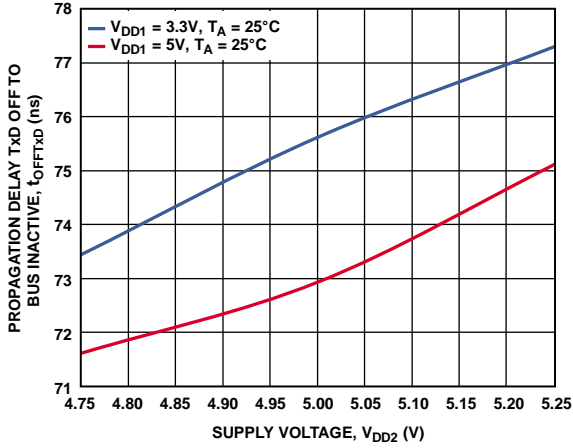
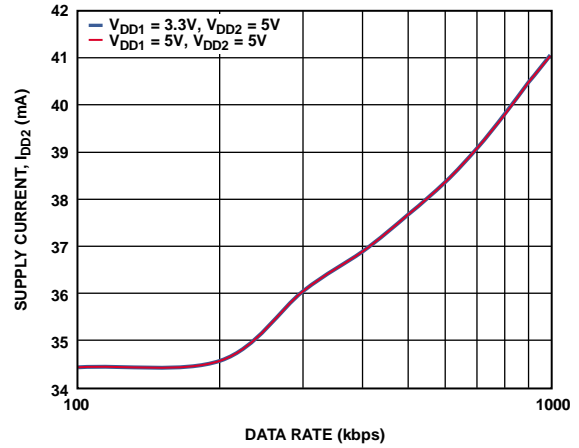


Figure 8. Propagation Delay from TxD Off to Bus Inactive vs. Temperature



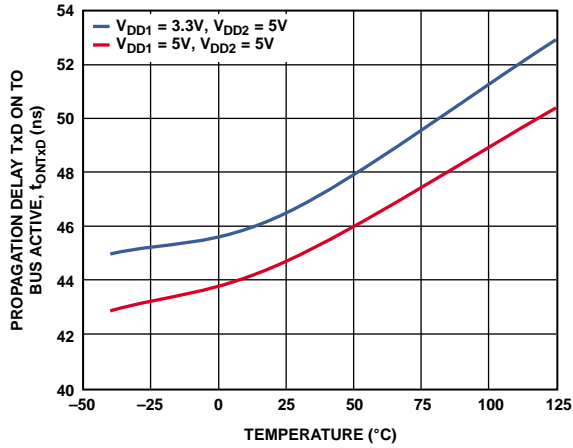
10274-016

Figure 9. Propagation Delay from TxD Off to Bus Inactive vs. Supply Voltage, V_{DD2}



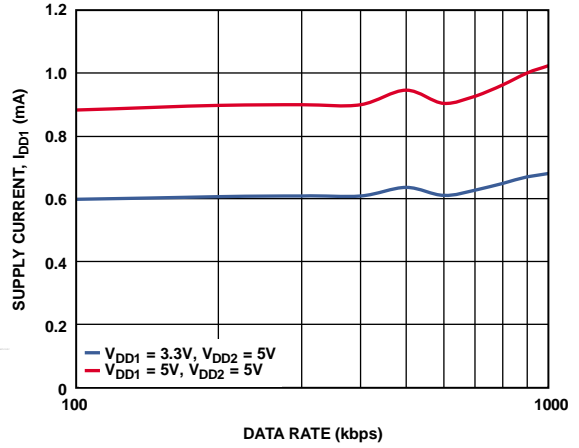
10274-019

Figure 12. Supply Current (I_{DD2}) vs. Data Rate



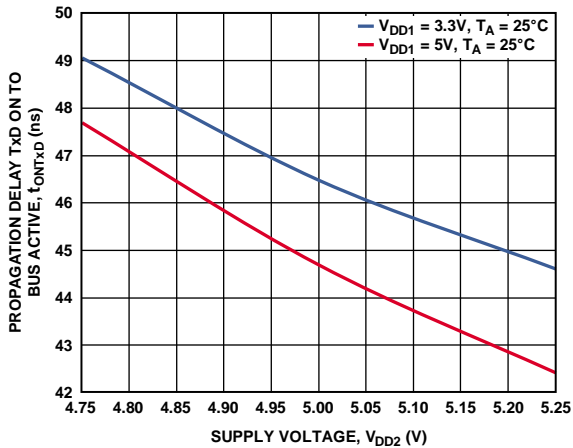
10274-017

Figure 10. Propagation Delay from TxD On to Bus Active vs. Temperature



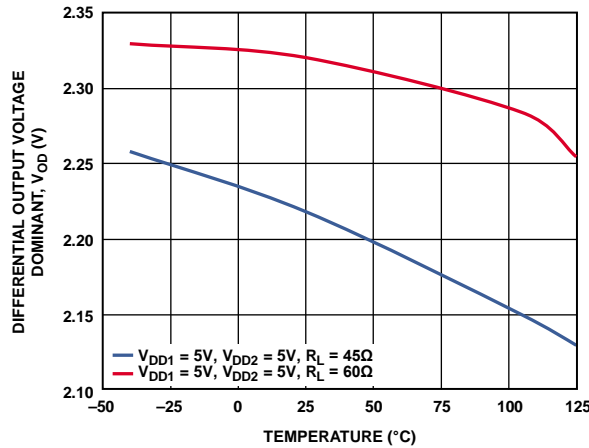
10274-020

Figure 13. Supply Current (I_{DD1}) vs. Data Rate



10274-018

Figure 11. Propagation Delay from TxD On to Bus Active vs. Supply Voltage, V_{DD2}



10274-021

Figure 14. Driver Differential Output Voltage Dominant vs. Temperature

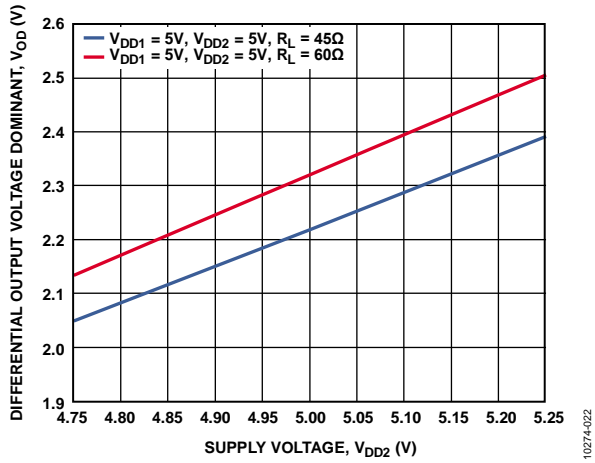


Figure 15. Driver Differential Output Voltage Dominant vs. Supply Voltage, V_{DD2}

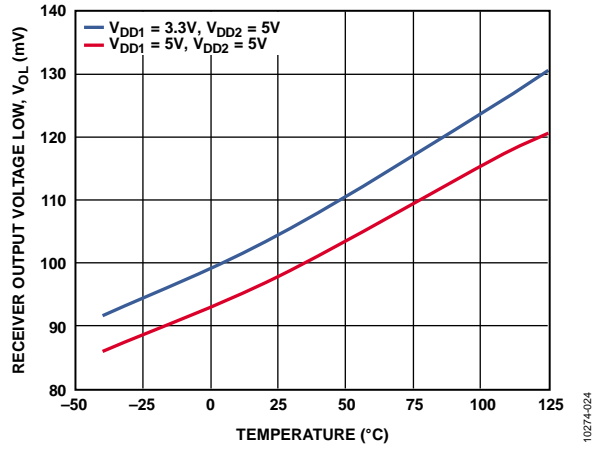


Figure 17. Receiver Output Low Voltage vs. Temperature

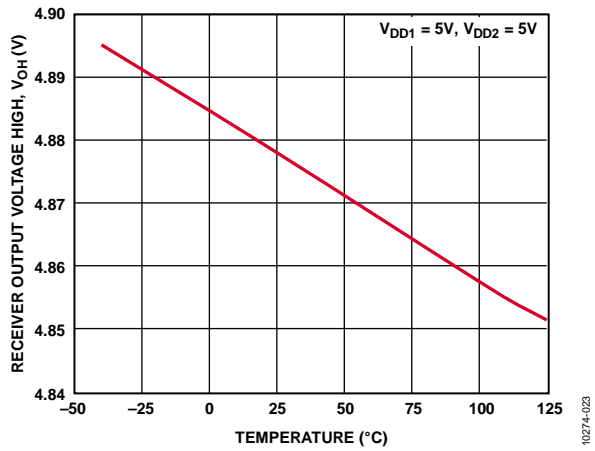


Figure 16. Receiver Output High Voltage vs. Temperature

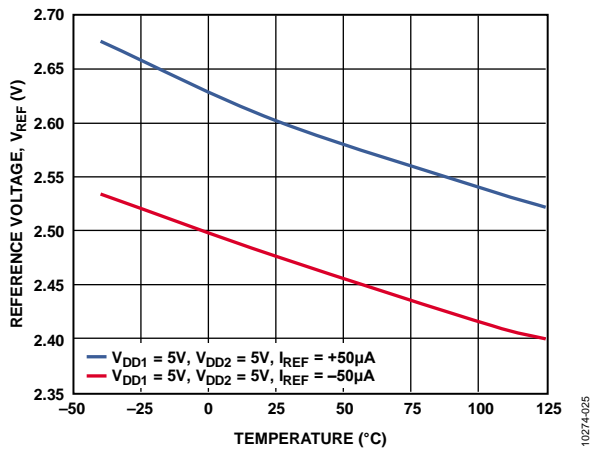


Figure 18. V_{REF} vs. Temperature

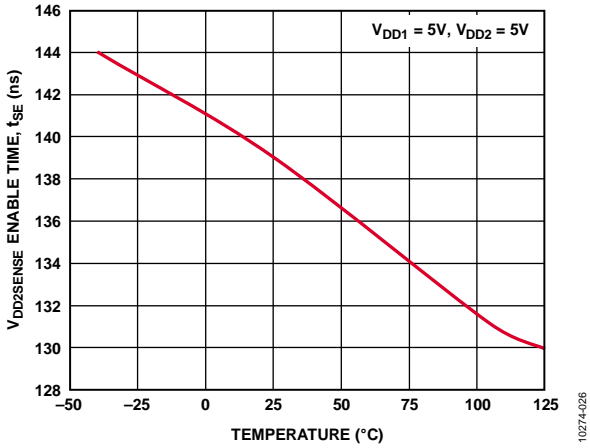


Figure 19. Enable Time, V_{DD2} High to V_{DD2SENSE} Low vs. Temperature

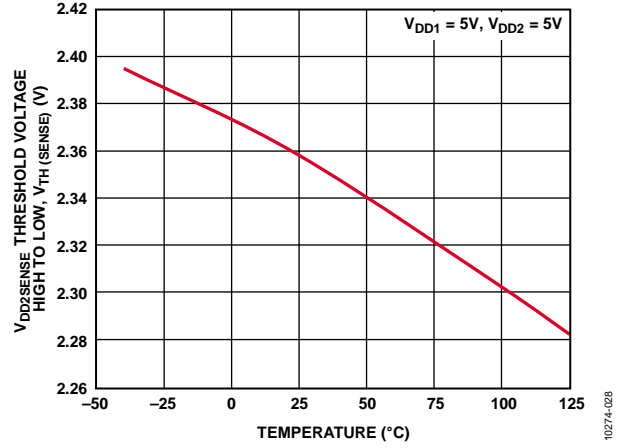


Figure 21. V_{DD2} Voltage Sense Threshold Voltage High to Low vs. Temperature

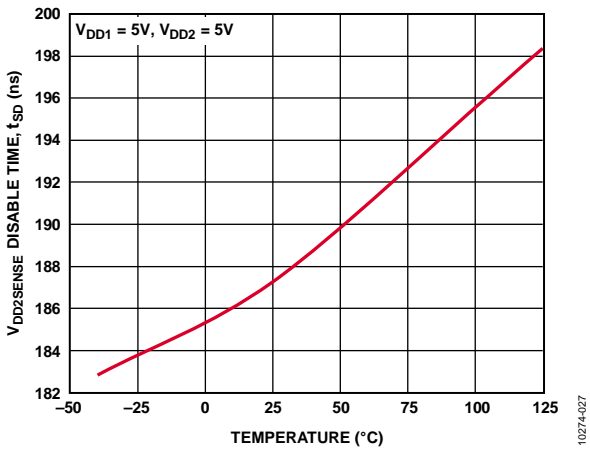


Figure 20. Disable Time, V_{DD2} Low to V_{DD2SENSE} High vs. Temperature

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

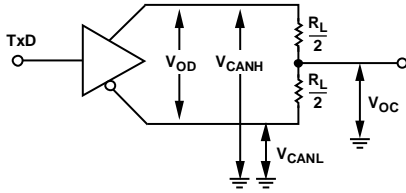


Figure 22. Driver Voltage Measurement

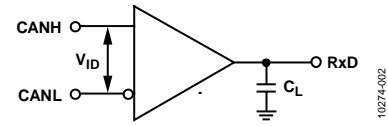


Figure 24. Receiver Voltage Measurements

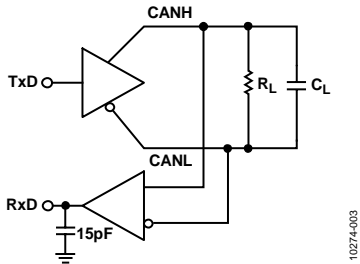


Figure 23. Switching Characteristics Measurements

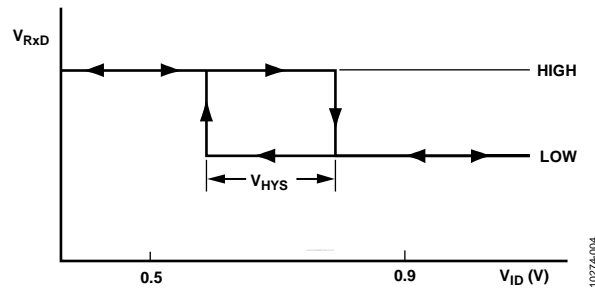


Figure 25. Receiver Input Hysteresis

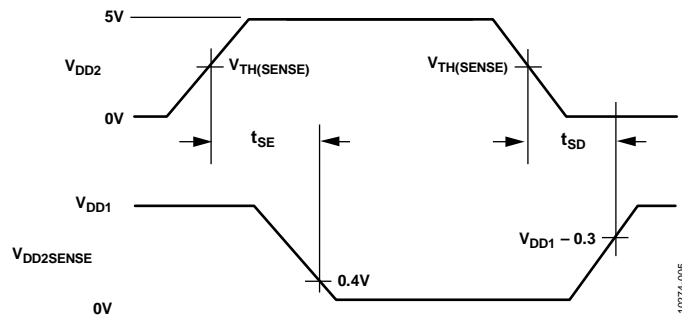


Figure 26. $V_{DD2SENSE}$ Enable/Disable Time

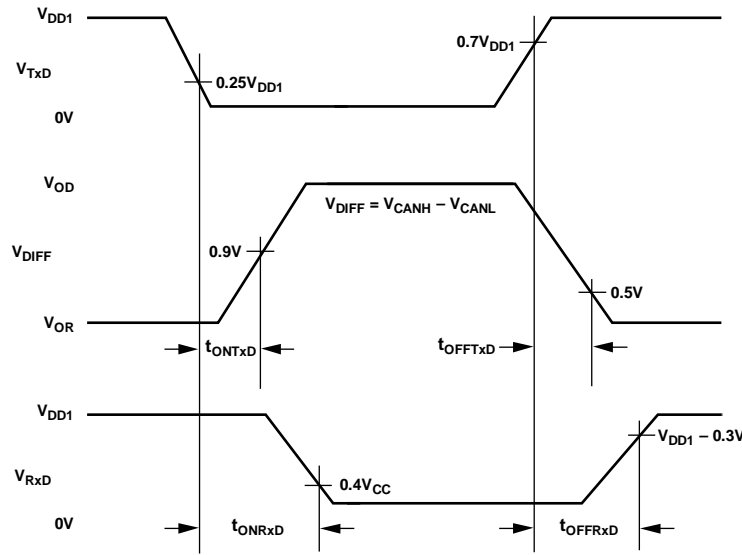


Figure 27. Driver and Receiver Propagation Delay

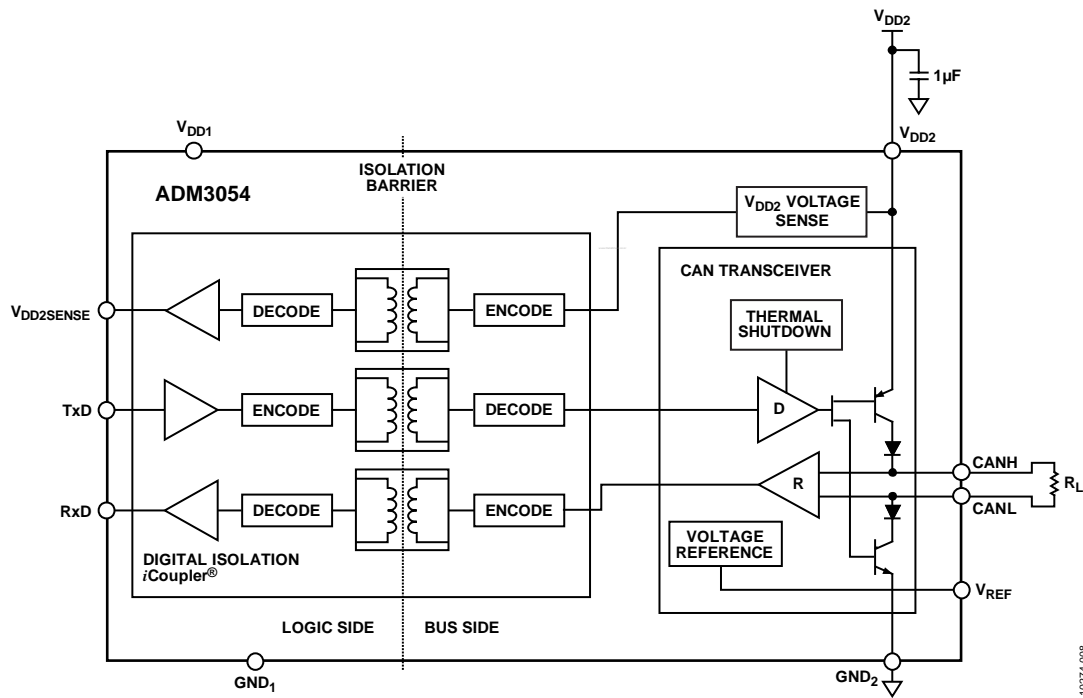


Figure 28. Supply Current Measurement Test Circuit

THEORY OF OPERATION

CAN TRANSCEIVER OPERATION

A CAN bus has two states: dominant and recessive. A dominant state is present on the bus when the differential voltage between CANH and CANL is greater than 0.9 V. A recessive state is present on the bus when the differential voltage between CANH and CANL is less than 0.5 V. During a dominant bus state, the CANH pin is high and the CANL pin is low. During a recessive bus state, both the CANH and CANL pins are in the high impedance state.

The driver drives CANH high and CANL low (dominant state) when a logic low is present on TxD. If a logic high is present on TxD, the driver outputs are placed in a high impedance state (recessive state). The driver output states are presented in Table 9.

The receiver output is low when the bus is in the dominant state and high when the bus is in the recessive state. If the differential voltage between CANH and CANL is between 0.5 V and 0.9 V, the bus state is indeterminate and the receiver output can be either high or low. The receiver output states for given inputs are listed in Table 10.

THERMAL SHUTDOWN

The ADM3054 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a junction temperature of 150°C is reached. As the device cools, the drivers reenables at a temperature of 140°C.

TRUTH TABLES

The truth tables in this section use the abbreviations listed in Table 8.

Table 8. Truth Table Abbreviations

Letter	Description
H	High level
L	Low level
I	Indeterminate
X	Don't care
Z	High impedance (off)
NC	Disconnected

Table 9. Transmitting

Supply Status		Input	Outputs			
V _{DD1}	V _{DD2}	TxD	State	CANH	CANL	V _{DD2SENSE}
On	On	L	Dominant	H	L	L
On	On	H	Recessive	Z	Z	L
On	On	Floating	Recessive	Z	Z	L
Off	On	X	Recessive	Z	Z	I
On	Off	L	I	I	I	H

Table 10. Receiving

Supply Status		Inputs		Outputs	
V _{DD1}	V _{DD2}	V _{ID} = CANH – CANL	Bus State	RxD	V _{DD2SENSE}
On	On	≥0.9 V	Dominant	L	L
On	On	≤0.5 V	Recessive	H	L
On	On	0.5 V < V _{ID} < 0.9 V	I	I	L
On	On	Inputs open	Recessive	H	L
Off	On	X	X	I	I
On	Off	X	X	H	H

ELECTRICAL ISOLATION

In the ADM3054, electrical isolation is implemented on the logic side of the interface. Therefore, the device has two main sections: a digital isolation section and a transceiver section (see Figure 29). The driver input signal, which is applied to the TxD pin and referenced to the logic ground (GND₁), is coupled across an isolation barrier to appear at the transceiver section referenced to the isolated ground (GND₂). Similarly, the receiver input, which is referenced to the isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to the logic ground.

iCoupler Technology

The digital signals transmit across the isolation barrier using iCoupler technology. This technique uses chip scale transformer

windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

Positive and negative logic transitions at the input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 μs, a periodic set of refresh pulses, indicative of the correct input state, are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the output is forced to a default state (see Table 9).

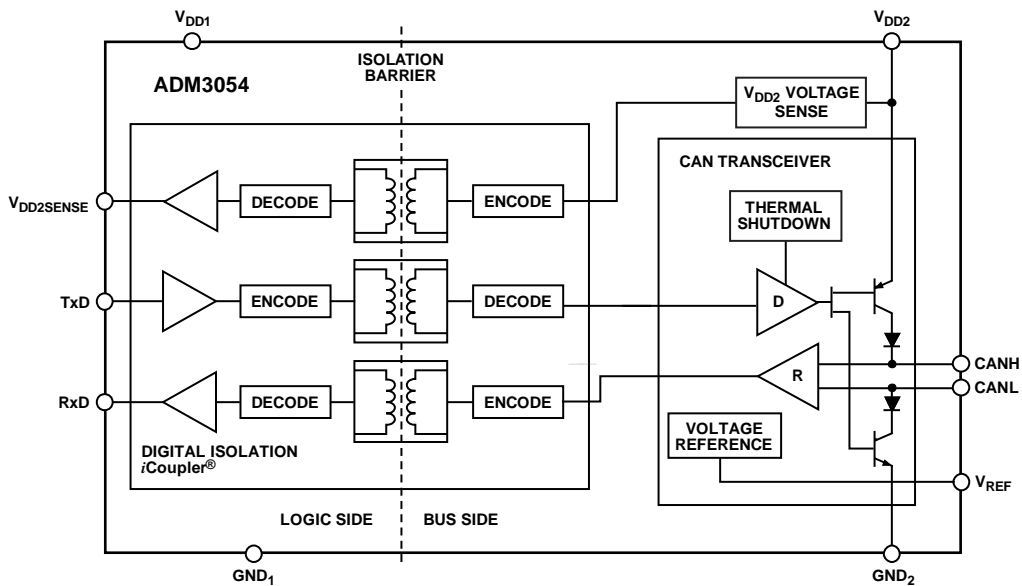


Figure 29. Digital Isolation and Transceiver Sections

10274-029

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the *iCoupler* is set by the condition in which an induced voltage in the receiving coil of the transformer is large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADM3054 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated.

The voltage induced across the receiving coil is given by

$$V = \left(\frac{-d\beta}{dt} \right) \sum \pi r_n^2 ; n = 1, 2, \dots, N$$

where:

β is the magnetic flux density (gauss).

N is the number of turns in the receiving coil.

r_n is the radius of the n^{th} turn in the receiving coil (cm).

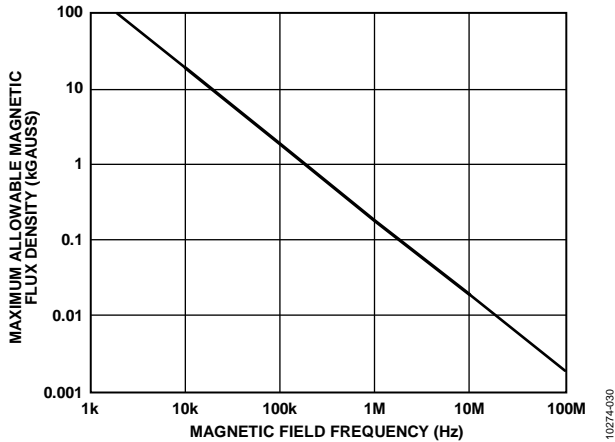


Figure 30. Maximum Allowable External Magnetic Flux Density

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field can be determined using Figure 30.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

Figure 31 shows the magnetic flux density values in terms of more familiar quantities, such as maximum allowable current flow at given distances away from the ADM3054 transformers.

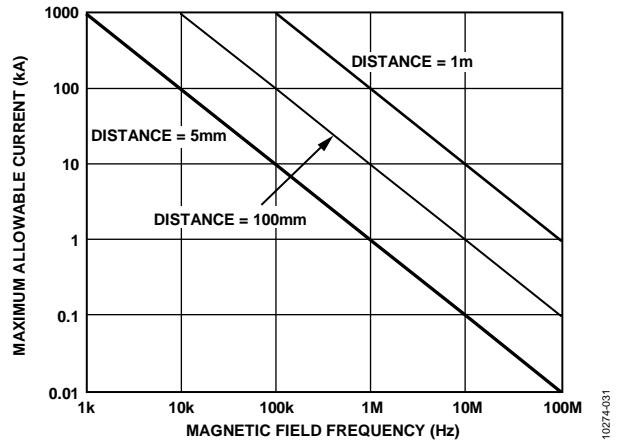
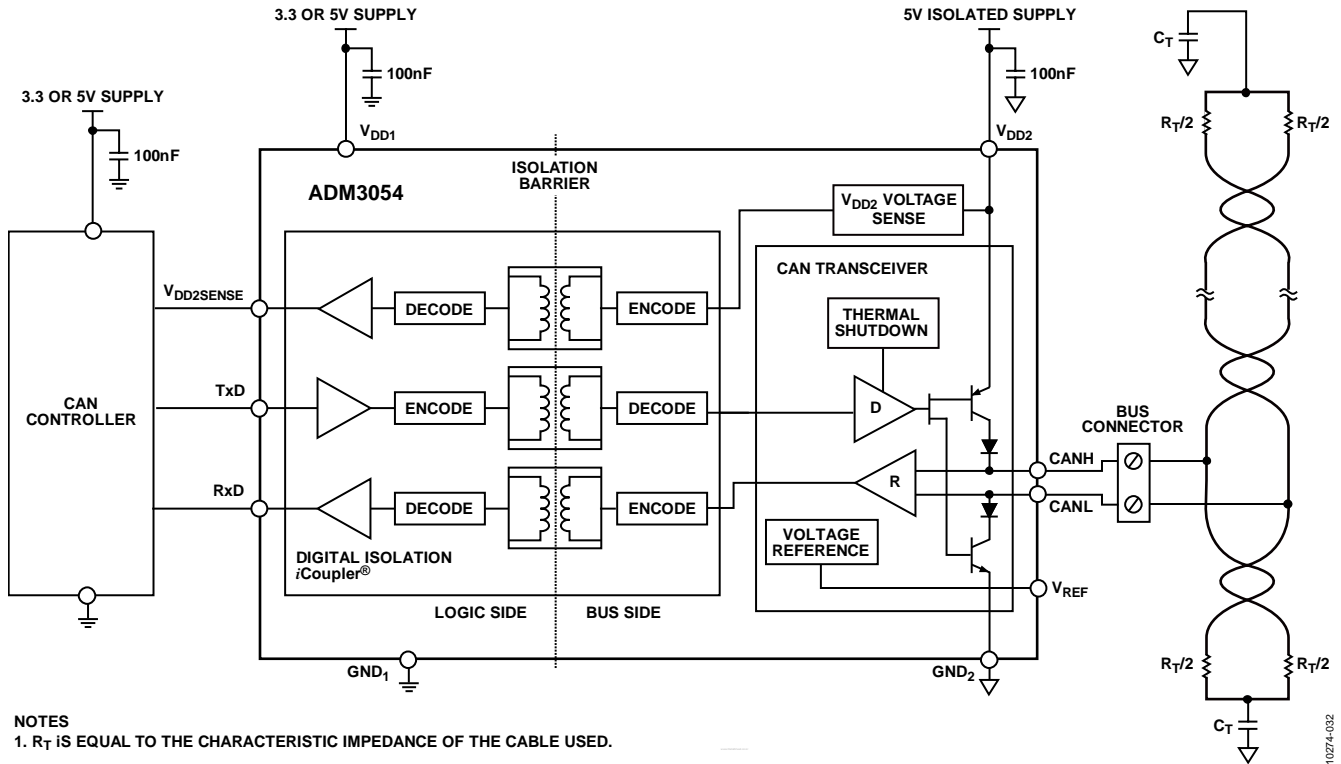


Figure 31. Maximum Allowable Current for Various Current-to-ADM3054 Spacings

With combinations of strong magnetic field and high frequency, any loops formed by printed circuit board (PCB) traces can induce error voltages large enough to trigger the thresholds of succeeding circuitry. Therefore, care is necessary in the layout of such traces to avoid this possibility.

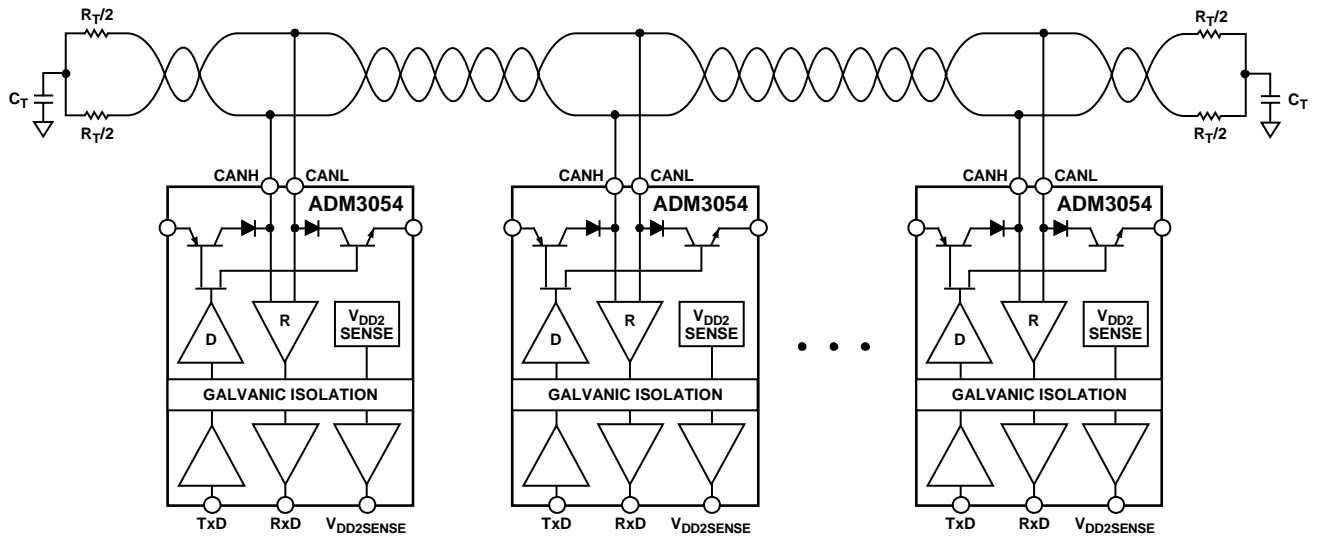
APPLICATIONS INFORMATION
TYPICAL APPLICATIONS



NOTES
1. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 32. Typical Isolated CAN Node Using the ADM3054

10274-032



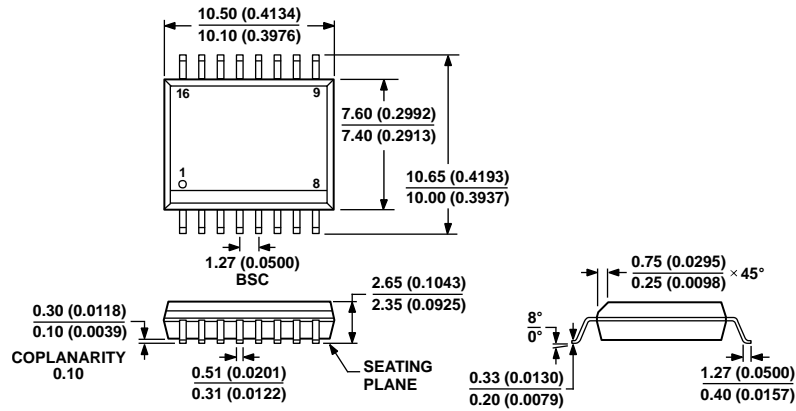
- NOTES**
1. MAXIMUM NUMBER OF NODES: 110.
 2. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 33. Typical CAN Bus Using the ADM3054

10274-003

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body
 (RW-16)

Dimensions shown in millimeters and (inches)

03-27-2007-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADM3054BRWZ	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADM3054BRWZ-RL7	-40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
EVAL-ADM3054EBZ		Evaluation Board	

¹ Z = RoHS Compliant Part.