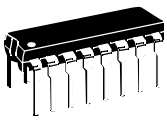
High Speed Graphic Monitor On-Screen Display - 16

CMOS

MC141545P2C



P SUFFIX
PLASTIC PACKAGE
CASE 648-08

ORDERING INFORMATION
MC141545P2C Plastic Dip

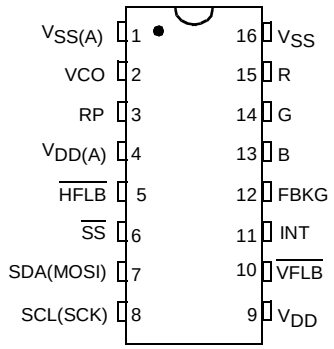
This is a high performance HCMOS device designed to interface with a micro controller unit to allow colored symbols or characters to be displayed onto CRT monitor. Because of the large number of fonts, 256 fonts including 240 standard fonts and 16 mulit-color fonts, HSGMOSD-16 is suitable to be adopted for the multi-language monitor application especially. Its on-chip PLL allows both multiscan operation and self generation of system timing. It also minimizes the MCU's burden through its built-in RAM. By storing a full screen of data and control information, this device has a capability to carry out 'screen-refresh' without any MCU supervision.

Since there is no clearance between characters, special graphics oriented characters can be generated by combining two or more character blocks. There are two kinds of resolutions that users can choose. By changing the number of dots per horizontal line to 384 (CGA) or 768 (SVGA), smaller characters with higher resolution can be easily achieved. The full OSD menu is formed of 15 rows x 30 columns which can by freely positioned on anywhere of the monitor screen by changing vertical or horizontal delay.

Special functions such as character background color, blinking, bordering or shadowing, four-level windows with programmable shadowing, row double height and double width, programmable vertical height of character and row-to-row spacing, and full-screen erasing and Fade-In/Fade-Out are also incorporated. There are 8 color selections for any individual character display with row intensity attribute and window intensity attribute to expand the color mixture on OSD menu.

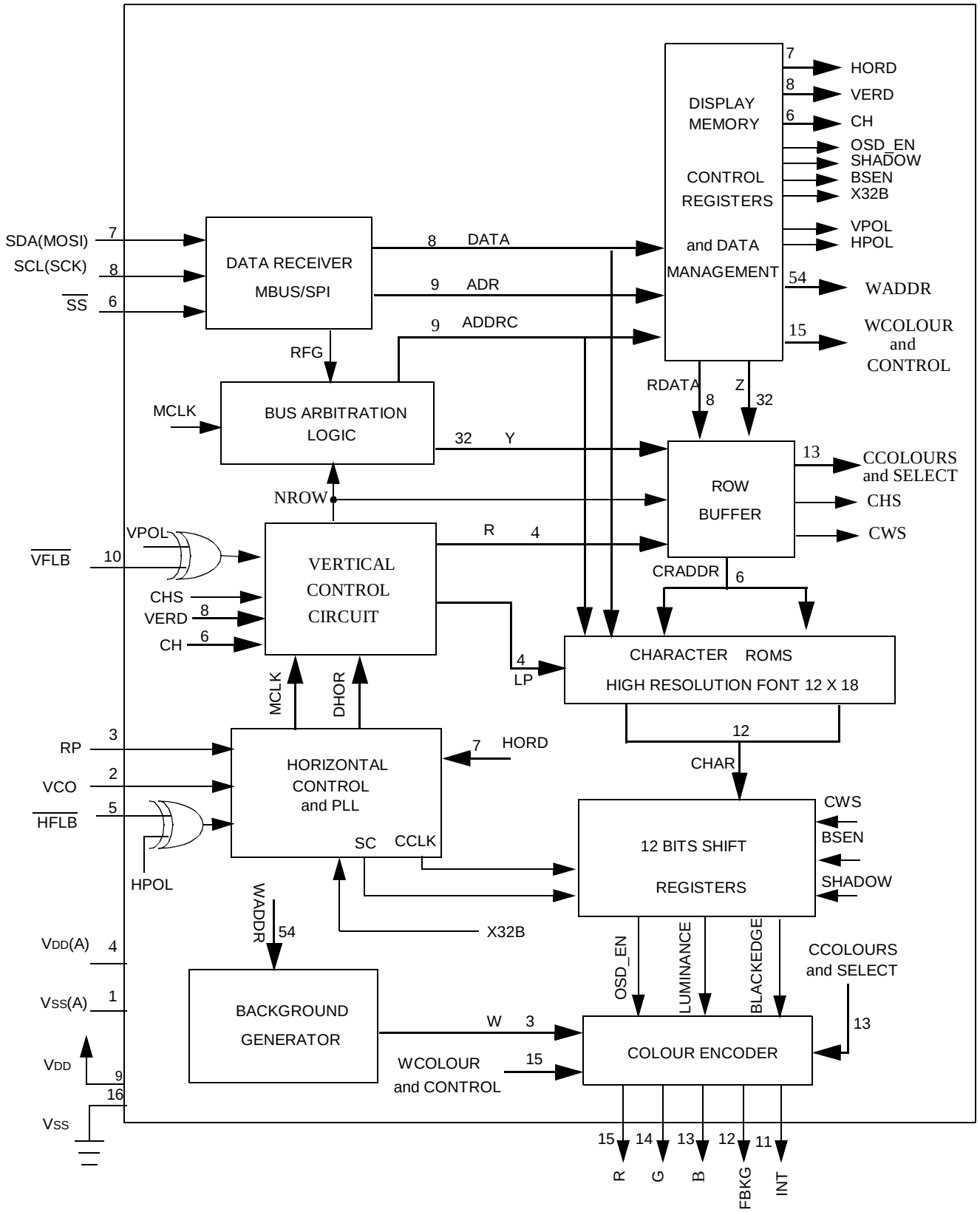
- Wide Operating Frequency Range for High End Monitor: max. 135KHz
- Totally 256 Fonts Including 240 Standard Fonts and 16 Multi-Color Fonts.
- Two Resolutions: 384 (CGA) or 768 (SVGA) Dots/Line
- Fully Programmable Character Array of 15 Rows by 30 Columns
- 8-Color Selection for Characters with Color Intensity Attribute on Each Row
- 7-Color Selection for Characters background
- True 16-Color Selection for Windows
- Fancy Fade-In/Fade-Out Effects
- Programmable Height of Character to Meet Multi-Sync Requirement
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability
- Shadowing on Windows with Programmable Shadow Width/Height
- Character Bordering or Shadowing
- Character/Symbol Blinking Function
- Programmable Vertical and Horizontal Positioning for Display Centre
- Double Character Height and Double Character Width
- Internal PLL Generates a Wide-Ranged System Clock (104 MHz)
- M_BUS (IIC) Interface with Address $7A (SPI Bus is Mask Option)

PIN ASSIGNMENT



MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS Voltage Referenced to V_{SS}

Symbol	Characteristic	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to + 7.0	V
V_{in}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
Id	Current Drain per Pin Excluding V_{DD} and V_{SS}	10	mA
Ta	Operating Temperature Range	0 to 85	°C
T_{stg}	Storage Temperature Range	– 65 to + 150	°C

NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Min	Typ	Max	Unit
VDD	Supply Voltage at Pin 9, Voltage Referenced to Pin16 VSS.	+4.75	—	+5.50	V
VDD(A)	Supply Voltage at Pin 4, Voltage Referenced to Pin16 VSS.	+4.75	—	+5.50	V
T_a	Ambient Temperature Range for Operation	0	—	+80	°C

AC ELECTRICAL CHARACTERISTICS (UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristic	Min	Typ	Max	Unit
	Output Signal (R, G, B, FBKG and INT) C_{load} = 10 pF				
t_r	Rise Time	—	—	4.5	ns
t_f	Fall Time	—	—	4.5	ns
$F_{\overline{HFLB}}$	HFLB Input Frequency	29K	—	135K	Hz

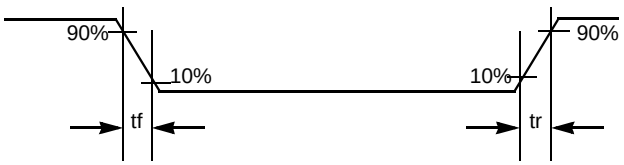


Figure 1. Switching Characteristics

DC CHARACTERISTICS (UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage I_{out} = – 5 mA	V_{DD} – 0.8	—	—	V
V_{OL}	Low Level Output Voltage I_{out} = 5 mA	—	—	V_{SS} + 0.4	V
 V_{IL} V_{IH}	Digital Input Voltage (Not Including SDA and SCL) Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in SPI Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
 V_{IL} V_{IH}	Input Voltage of Pin SDA and SCL in M_BUS Mode Logic Low Logic High	 — 0.7 V_{DD}	 — —	 0.3 V_{DD} —	 V V
I_{II}	High-Z Leakage Current (R, G, B and FBKG)	– 10	—	+ 10	μA
I_{II}	Input Current (Not Including RP, VCO, R, G, B, FBKG and INT)	– 10	—	+ 10	μA
I_{DD}	Supply Current (No Load on Any Output) at VDD/VDDA=5.0V	—	—	+ 26	mA

M_BUS AC TIMING (UNDER RECOMMENDED OPERATING CONDITIONS)

Symbol	Characteristics	Min	Typ	Max	Unit
f_{SCL}	SCL Clock Frequency(HFLB frequency >= 29KHz)	—	—	400	kHz
t_{BUF}	BUS free time between a STOP and START condition	500	—	—	ns
t_{HDSTA}	START condition hold time	500	—	—	ns
t_{LOW}	SCK low period	400	—	—	ns
t_{HIGH}	SCK high period	400	—	—	ns
t_{SUSTA}	START condition set-up time(for repeated START condition only)	100	—	—	ns
t_{HDDAT}	Data hold-time	250	—	—	ns
t_{SUDAT}	Data set-up time	100	—	—	ns
t_{SUSTO}	Set-up time for STOP condition	500	—	—	ns

NOTES: For the M_BUS can run at full speed and meet above specifiction, the $\overline{\text{HFLB}}$ signal should be applied to pin5 not less than 60ms in advance of M_BUS communication. This 60ms timing is for the stablizing of HSGMOSD internal PLL CLK.

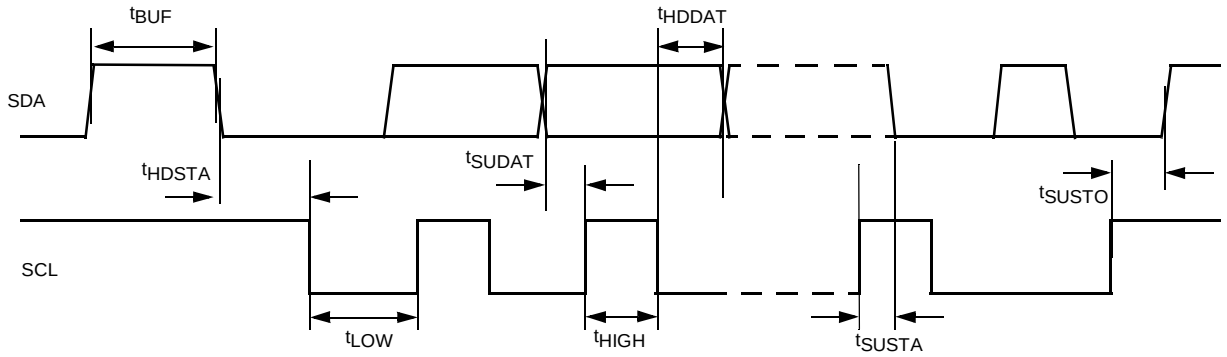


Figure 2. M_BUS TIMING

PIN DESCRIPTION

VSS(A) (Pin 1)

This pin provides the signal ground to the PLL circuitry. Analog ground for PLL is separated from digital ground for optimal performance.

VCO (Pin 2)

A dc control voltage input to regulate an internal oscillator frequency. See the Application Diagram for the application values used.

RP (Pin 3)

An external RC network is used to bias an internal VCO to resonate at the specific dot frequency. The voltage at Pin 3 should operate from 0.2V to 2.5V at any condition. See the Application Diagram for the application values used.

$V_{DD(A)}$ (Pin 4)

A positive 5 V dc supply for PLL circuitry. Analog power for PLL is separated from digital power for optimal performance.

$\overline{\text{HFLB}}$ (Pin 5)

This pin inputs a negative polarity horizontal synchronize signal pulse to phase lock into an internal system clock generated by the on-chip VCO circuit. The HFLB signal input to this pin must be present during the BUS communication. Please also refer to "BUS operation" section.

$\overline{\text{SS}}$ (Pin 6)

This input pin is part of the SPI system. An active low signal generated by the master device enables this slave device to accept data. Pull high to terminate the SPI communication. If M_BUS is employed as the serial interface, this pin should be tied to either V_{DD} or V_{SS}. This pin is in high impedence state when the chip is being power down.

SDA (MOSI) (Pin 7)

Data and control message are being transmitted to this chip from a host MCU, via one of the two serial bus systems. With either protocol, this wire is configurated as a uni-directional data line. (Detailed description of these two protocols will be discussed in the M_BUS and SPI sections). This pin is in high impedence state when the chip is being power down.

SCL (SCK) (Pin 8)

A separate synchronizing clock input from the transmitter is required for either protocol. Data is read at the rising edge of each clock signal. This pin is in high impedence state when the chip is being power down.

V_{DD} (Pin 9)

This is the power pin for the digital logic of the chip.

$\overline{\text{VFLB}}$ (Pin 10)

Similar to Pin 5, this pin inputs a negative polarity of vertical synchronize signal to synchronize the vertical control circuit.

INT (Pin 11)

This output pin is used to indicate the color intensity. If the intensity control bits are set in the row attribute registers or window control registers, this pin will output a logic high while displaying the specified windows or the characters on the associated rows. Otherwise, it will keep in low state. Please refer to Figure 14 for detail timing chart. Thus, 16-color selection is achievable by combining this intensity pin with R/G/B outputs. On the other hand, this color intensity information could be reflected on the R/G/B pins by asserting tri-state instead of logic high if 3_S bit is set to 1. Refer to the “REGISTERS” for more information.

FBKG (Pin 12)

This pin will output a logic high while displaying characters or windows when FBKGC bit in frame control register is 0, and output a logic high only while displaying characters when FBKGC bit is 1. It is defaulted to high impedance state after power on, or when there is no output. An external 10 kΩ resistor pulled low is recommended to avoid level toggling caused by hand effect when there is no output.

B,G,R (Pin 13, 14, 15)

HSGMOSD-16 color outputs in CMOS level to the host monitor. These three signals are open drain outputs if 3_STATE bit is set and the color intensity is inactive. Otherwise, they are active high push-pull outputs. See “REGISTERS” for more information. These pins are in high impedance state after power on.

V_{SS} (Pin 16)

This is the ground pin for the digital logic of the chip.

SYSTEM DESCRIPTION

MC141545P2C is a full screen memory architecture. Refresh is done by the built-in circuitry after a screenful of display data has been loaded in through the serial bus. Only changes to the display data need to be input afterward.

Serial data, which includes screen mapping address, display information, and control messages, are being transmitted via one of the two serial buses: M_BUS or SPI (mask option). These two sets of buses are multiplexed onto a single set of wires. Standard parts offer M_BUS transmission.

Data is first received and saved in the MEMORY MANAGEMENT CIRCUIT in the Block Diagram. Meanwhile, the HSGMOSD-16 is continuously retrieving the data and putting it into a ROW BUFFER for display and refreshing, row after row. During this storing and retrieving cycle, a BUS ARBITRATION LOGIC will patrol the internal traffic, to make sure that no crashes occur between the slower serial bus receiver and fast ‘screen-refresh’ circuitry. After the full screen display data is received through one of the serial communication interface, the link can be terminated if change on display is not required.

The bottom half of the Block Diagram constitutes the heart of this entire system. It performs all the HSGMOSD-16 functions such as programmable vertical length (from 16 lines to 63 lines), display clock generation (which is phase locked to the incoming horizontal sync signal at Pin 5 HFLB), bordering or shadowing, and multiple windowing.

COMMUNICATION PROTOCOLS

BUS Operation

The operating clock for M_Bus or SPI bus derives from system dot clock. Internal PLL is using to generate the dot clock base on the HFLB input frequency where the dot clock is equal to 384/768xHFLB in 384/768 modes respectively. In order to have stable operation of M_Bus or SPI bus in the OSD

and meet below specifications, $\overline{\text{HFLB}}$ must be presented and the PLL locks to $\overline{\text{HFLB}}$ properly. Refer to Application Diagram for PLL bias circuit.

M_BUS Serial Communication

This is a two-wire serial communication link that is fully compatible with the IIC bus system. It consists of SDA bidirectional data line and SCL clock input line. Data is sent from a transmitter (master), to a receiver (slave) via the SDA line, and is synchronized with a transmitter clock on the SCL line at the receiving end. The maximum data rate is limited to 400 kbps.The default chip address is $7A. Please refer to the IIC-Bus specification for detail timing requirement.

Operating Procedure

Figure 3 shows the M_BUS transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGE signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACKNOWLEDGE bit, to make up nine bits together. Appropriate row and column address information and display data can be downloaded sequentially in one of the three transmission formats described in DATA TRANSMISSION FORMATS SECTION. In the cases of no ACKNOWLEDGE or completion of data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the HSGMOSD-16 circuitry of MC141545P2C, so that the received information can then be displayed.

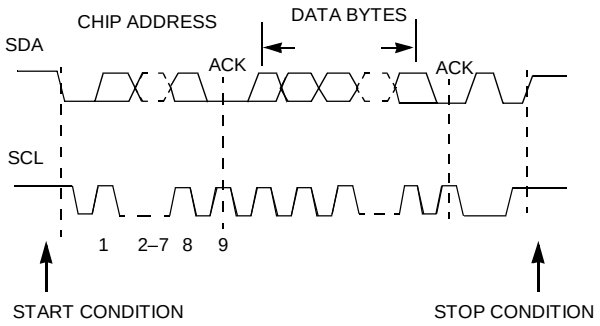


Figure 3. M_BUS Format

Serial Peripheral Interface (SPI)

Similar to M_BUS communication, SPI requires separate clock (SCK) and data (MOSI) lines. In addition, a $\overline{\text{SS}}$ SLAVE SELECT pin is controlled by the master transmitter to initiate the receiver.

Operating Procedure

To initiate SPI transmission, pull $\overline{\text{SS}}$ pin low by the master device to enable MC141545P2C to accept data. The $\overline{\text{SS}}$ input line must be a logic low prior to occurrence of SCK and remain low until and after the last (eighth) SCK cycle. After all data has been sent, the $\overline{\text{SS}}$ pin is then pulled high by master to terminate the transmission. Data bit is sent from master to OSD's internal latch during rising edge of SCK and then transmit to internal register during falling edge. Therefore, last falling edge of CLK is needed for proper transmission of last byte data. No slave address is needed for SPI. Hence, row and column address information and display data (the data transmission formats are the same as in M_BUS mode described in the previous section) can be sent immediately after the SPI is initiated.

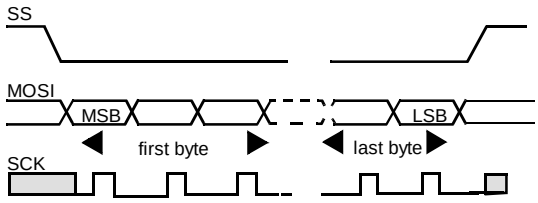


Figure 4. SPI Protocol

DATA TRANSMISSION FORMATS

After the proper identification by the receiving device, data train of arbitrary length is transmitted from the Master. As mentioned above, two register blocks, display registers, attribute/control registers, need to be programmed before the proper operation. Basically, these three areas use the similar transmission protocol. Only two bits of the row/segment byte are used to distinguish the programming blocks.

There are three transmission formats, from (a) to (c) as stated below. The data train in each sequence consists of row/seg address (R), column/line address (C), and data informations (I). In format (a), each display information data have to be preceded with the corresponding row/seg address and column/line address. This format is particular suitable for updating small amount of data between different row. However, if the current information byte has the same row/seg address as the one before, format (b) is recommended. For a full screen pattern change which requires massive information update or during power up situation, most of the row/seg and column/line address on either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. It sends the RAM starting row/seg and column/line addresses once only, and then treat all subsequent data as data information. The row/seg and column/line addresses will be automatically incremented internally for each information data from the starting location.

Based on the different programming areas, the detail transmission protocol is described below respectively.

(I) Display Register Programming

The data transmission formats are:

(a) R - > C- > I -> R - > C - > I - > . . . . . .

(b) R - > C - > I - > C - > I - > C - > I. . . . . .

(c) R - > C - > I - > I - > I - > . . - > I_{dummy} - > I_{dummy} - > I - > I. .

NOTE: - R means row byte.

- C means column byte.
- I means data byte.
- In format (c), two dummy data bytes(col 30, col 31)have to be inserted after the last data byte(col 29) at the end of each row, before the first data byte of the next row.

To differentiate the display row address from attribute area when transferring data, the most significant three bits are set to '100' to represent display row address, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

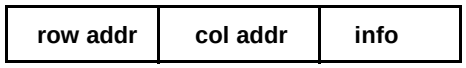
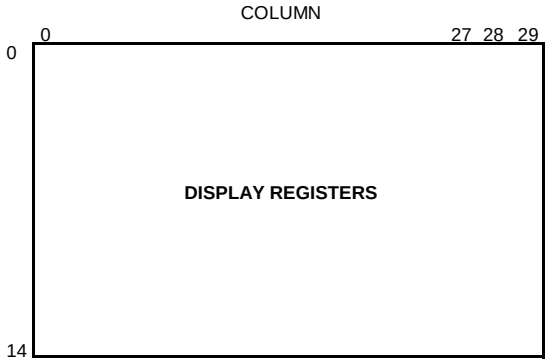


Figure 5. Data Packet for Display Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	0	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 6. Address Bit Patterns for Display Data

(II) Attribute/Control Register Programming

The data transmission formats are similar with that in display data programming:

(a) R - > C- > I -> R - > C - > I - > . . . . . .

(b) R - > C - > I - > C - > I - > C - > I. . . . . .

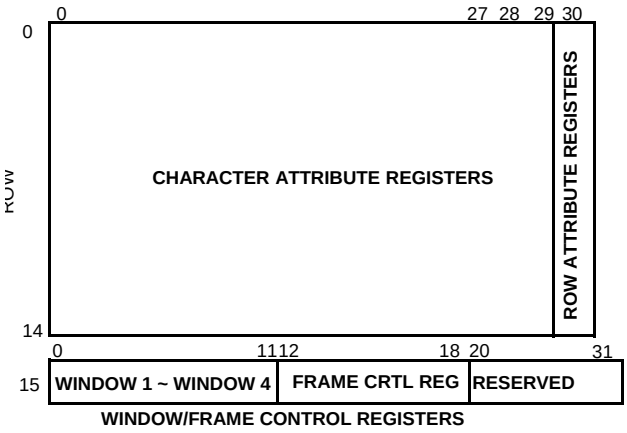
(c) R - > C - > I - > I - > I - > . .- > $I_{row\ attr.}$ - > I_{dummy} - > I - > I. .

NOTE: - R means row byte.

- C means column byte.
- I means data byte.
- In format (c), one dummy data byte(col 31) has to be inserted after the row attribute data byte (col 30) at end of each row, before the first character attribute data byte of the next row.

To differentiate the row address for attribute/control registers from display area when transferring data, the most significant three bits are set to '101' to represent the row address of the attribute/control registers, while '00X' for column address used in format (a) or (b) and '01X' for column address used in format (c). There is some limitation on using mix-formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

Figure 7. Data Packet for Attribute/Control Data



ADDRESS	BIT								FORMAT
	7	6	5	4	3	2	1	0	
ROW	1	0	1	X	D	D	D	D	a, b, c
COLUMN	0	0	X	D	D	D	D	D	a, b
COLUMN	0	1	X	D	D	D	D	D	c

X: don't care D: valid data

Figure 8. Address Bit Patterns for Attribute/Control Data

MEMORY MANAGEMENT

All the internal programmable area can be divided into two parts including (1) Display Registers (2) Attribute/Control Registers. Please refer to the following two figures for the corresponding memory map.

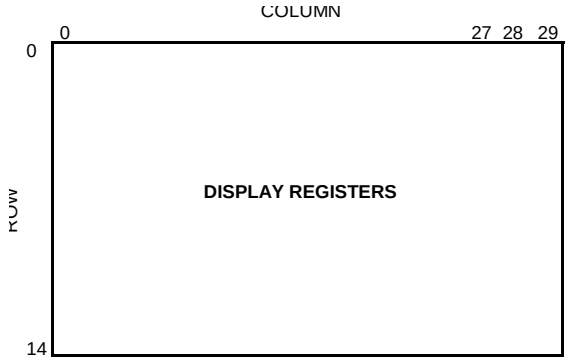


Figure 9. Memory Map of Display Registers

Internal display RAM are addressed with row and column (coln) number in sequence. As the display area is 15 rows by 30 columns, the related display registers are also 15 by 30. The space between row 0 and coln 0 to row 14 and coln 29 are called Display registers, with each contains a character/ symbol address corresponding to display location on monitor screen. And each register is 8-bit wide to identify the selected character/symbol out of 256 ROM fonts.

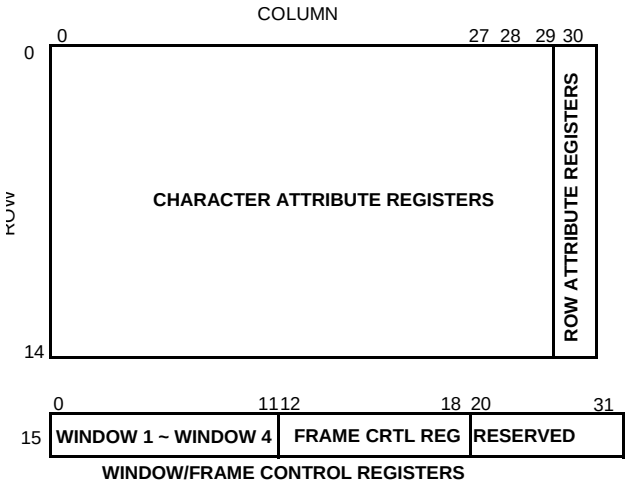


Figure 10. Memory Map of Attribute/Control Registers

Besides the font selection, there is 3-bit attribute associated with each symbol to identify its color and 3-bit to define its background. Because of 3-bit attribute, each character can select any color out of 8 independently on the same row. as well as background. Every data row associate with one attribute register, which locate at coln 30 of their respective rows, to control the characters display format of that row such as the character blinking, color intensity, character double height and character double width function. In addition, other control registers are located at row 15 such as window control and frame function control registers. Three window control registers for each of four windows together with four frame control registers occupy the first 18 columns of row 15 space. These control registers will be described on the “REGISTERS” section.

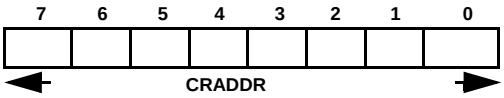
User should handle the internal display RAM address location with care especially for those rows with double length alphanumeric symbols. For example, if row n is destined to be double height on the memory map, the data displayed on screen row n and n+1 will be represented by the data contained in the memory address of row n only. The data of next row n+1 on the memory map will appear on the screen of n+2 and n+3 row space and so on. Hence, it is not necessary to throw in a row of blank data to compensate for the double row action. User needs to take care of excessive row of data in memory in order to avoid over running the limited number of row space on the screen.

There is difference for rows with double width alphanumeric symbols. Only the data contained in the even numbered columns of memory map will be shown, the odd numbered columns will be ignored and not disclosed.

REGISTERS

(I) Display Register

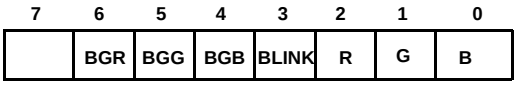
Display Register (Row 0~14, Coln 0~29)



Bit 7-0 CRADDR - This eight bits address one of the 256 characters or symbols resided in the character ROM fonts.

(II) Attribute/Window/Control/Frame Registers

Character Attribute Register (Row 0~14, Coln 0~29)



Bit 6-4 These three bits define the color of the background for the correspondent characters. If all three bits are clear, no background will be shown(transparent). Therefore, total seven background colors can be selected.

Bit 3 BLINK - The blinking effect will be active on the corresponding character if this bit is set to 1. The blinking frequency is approximately one time per second (1Hz) with fifty-fifty duty cycle at 80Hz vertical scan frequency.

Bit 2-0 These three bits are the color attribute to define the color of the associated character/symbol.

Table 1. The Character/Window Color Selection

	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Row Attribute Register (Row 0~14, Coln 30)

7	6	5	4	3	2	1	0
					R_INT	CHS	CWS

Bit 2 R_INT - Row intensity bit controls the color intensity of the displayed character/symbol on the corresponding row. Setting this bit to 1 means high intensity color and the INT pin will go high while displaying the characters of this row.

Bit 1 CHS - It determines the height of a display symbol. When this bit is set, the symbol is displayed in double height.

Bit 0 CWS - Similar to bit 1, character is displayed in double width, if this bit is set.

Window 1 Registers

Row 15 Coln 0

	7	6	5	4	3	2	1	0
ROW 15 COLN 0	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

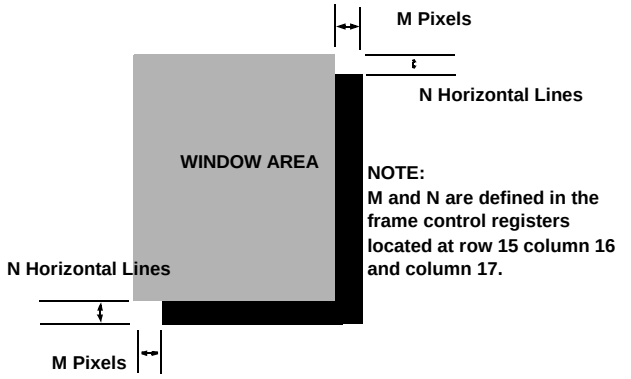
Row 15 Coln 1

	7	6	5	4	3	2	1	0
ROW 15 COLN 1	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 1 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 1. If this bit is 0, INT pin will go low while displaying window 1.The default value is 1 to indicate high intensity. .Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 1 shadowing. When the window is active, the right M pixels and lower N horizontal scan lines will output black shadowing. The width/height of window shadow, number of M/N, is defined in the frame control registers located at row 15 column 16 and 17. See the following figure and the related frame control register for detail.



Window Shadowing

Row 15 Coln 2

	7	6	5	4	3	2	1	0
ROW 15 COLN 2	COL END ADDR MSB				LSB	R	G	B

Bit 2-0 R, G and B - Controls the color of window 1. Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 2 Registers

Row 15 Coln 3

	7	6	5	4	3	2	1	0
ROW 15 COLN 3	ROW START ADDR MSB			LSB	ROW END ADDR MSB			LSB

Row 15 Coln 4

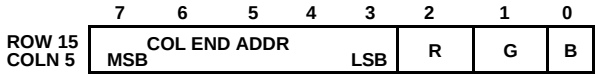
	7	6	5	4	3	2	1	0
ROW 15 COLN 4	COL START ADDR MSB				LSB	WEN	W_INT	W_SHD

Bit 2 WEN - It enables the window 2 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 2. If this bit is 0, INT pin will go low while displaying window 2.The default value is 1 to indicate high intensity. .Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 2 shadowing.

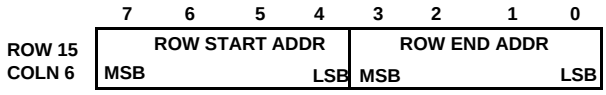
Row 15 Coln 5



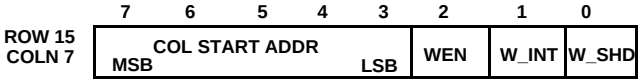
Bit 2-0 R, G and B - Controls the color of window 2.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 3 Registers

Row 15 Coln 6



Row 15 Coln 7

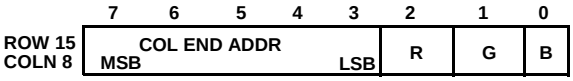


Bit 2 WEN - It enables the window 3 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 3. If this bit is 0, INT pin will go low while displaying window 3.The default value is 1 to indicate high intensity. .Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 3 shadowing.

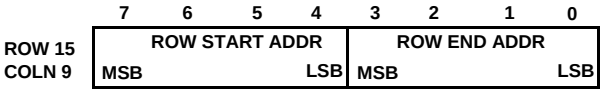
Row 15 Coln 8



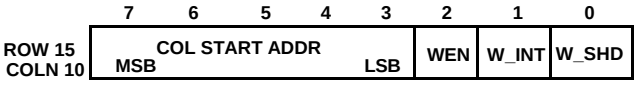
Bit 2-0 R, G and B - Controls the color of window 3.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Window 4 Registers

Row 15 Coln 9



Row 15 Coln 10

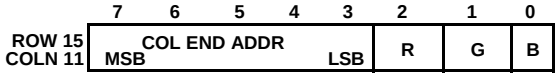


Bit 2 WEN - It enables the window 4 generation if this bit is set.

Bit 1 W_INT - This additional color related bit provides the color intensity selection for window 4. If this bit is 0, INT pin will go low while displaying window 4.The default value is 1 to indicate high intensity. Video pre-amplifier or external R/G/B switch can make use of INT pin for windows's color intensity control.

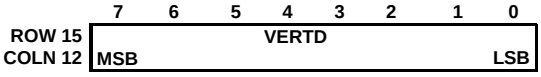
Bit 0 W_SHD - Shadowing on window. Set this bit to activate the window 4 shadowing.

Row 15 Coln 11



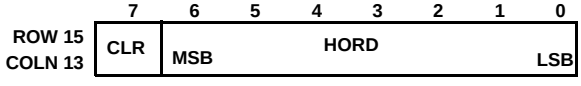
Bit 2-0 R, G and B - Controls the color of window 4.Refer to Table 1 for color selection. Window 1 registers occupy Column 0-2 of Row 15, Window 2 from Column 3-5, Window 3 from 6-8 and Window 4 from 9-11. Window 1 has the highest priority, and Window 4 the least. If window over-lapping occurs, the higher priority window will cover the lower one, and the higher priority color will take over on the overlap window area. If the start address is greater than the end address, this window will not be displayed.

Vertical Delay Control Register Row 15 Coln 12



Bit 7-0 VERTD - These 8 bits define the vertical starting position. Total 256 steps, with an increment of four horizontal lines per step for each field. Its value can't be zero anytime. The default value of it is 4.

Horizontal Delay Control Register Row 15 Coln 13



Bit 7 CLR - Setting this bit to 1 clear all display register from Row 0 to Row 14; Control register will not be erased.

Bit 6-0 HORD - Horizontal starting position for character display. 7 bits give a total of 128 steps and each increment represents five dots movement shift to the right on the monitor screen. Its value cannot be zero anytime. The default value of it is 15.

Character Height Control Register Row 15 Coln 14

	7	6	5	4	3	2	1	0
ROW 15 COLN 14	HF	0	CH5	CH4	CH3	CH2	CH1	CH0

Bit 7 HF - High Frequency Bit. If the incoming H sync signal is higher than 60 KHz, set this bit to 1 for better performance. This bit controls gain of internal VCO so that PLL can work for whole range from up to 135KHz.

Bit 6 Bit reserved. Set to 0 for normal operation.

Bit 5-0 CH5-CH0 - This six bits will determine the displayed character height. HSGMOSD adopts 12 by 18 font matrix and the middle 16 lines, line 2 to line 17, are expanded by BRM algorithm. The top line and bottom line will be duplicated dependent on the value of CH. No any line is duplicated for top and bottom if CH is less than 32. One extra duplicated line will be inserted for top and bottom if CH is larger or equal to 32 and less than 48. Two extra duplicated lines will be inserted for top and bottom if CH is larger or equal to 48. Setting a value below 16 will not have a predictable result. Display character line number is equal to C1 x (18 + C2) where C1 = 1, 2 or 3 defined by CH5-CH4 and C2 = 0-15 defined by CH3-CH0 (BRM).

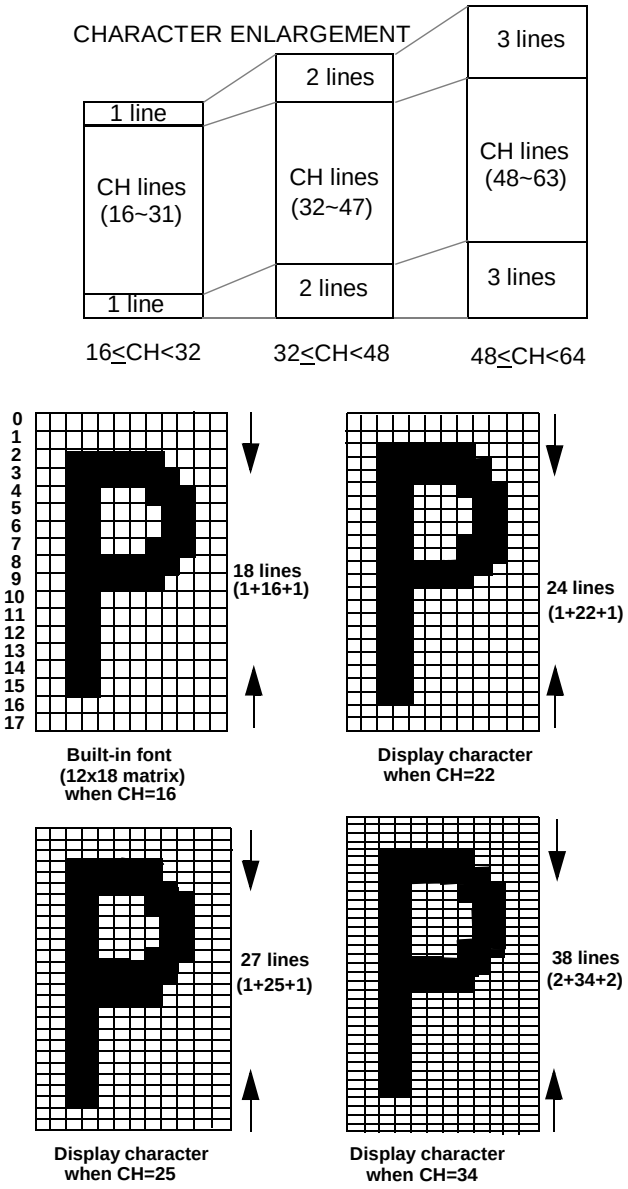


Figure 11. Variable Character Height

Figure 11 illustrates the enlargement algorithm for top and bottom lines and how this chip expand the built-in character font to the desired height.

In this approach, the actual character height in unit of the scan line can be calculated from the following simple equation:

H = CH + N

Where H is the expanded character height in unit of lines

CH is the number defined by CH5 ~ CH0

N is a variable dependent on the value of CH

N = 2 when 16≤CH<32

N = 4 when 32≤CH<48

N = 6 when 48≤CH<64

Frame Control Register Row 15 Coln 15

	7	6	5	4	3	2	1	0
ROW 15 COLN 15	OSD_EN	BSEN	SHADOW		X32B	3_S	FAN	FBKGC

Bit 7 OSD_EN - OSD circuit is activated when this bit is set.

Bit 6 BSEN - It enables the character bordering or shadowing function when this bit is set.

Bit 5 SHADOW - Character with black-edge shadowing is selected if this bit is set, otherwise bordering prevails.

Bit 3 X32B - It determines the number of dots per horizontal line. There are 384 dots per horizontal line if bit X32B is clear and this is also the default power on state. Otherwise, 768 dots per horizontal sync line when bit X32B is set to 1. Please refer to the Table 2 for details.

Table 2. Resolution Setting

X32B	0	1
Dots / Line	384	768
Resolution	CGA	SVGA

Bit 2 3_S - By setting this bit to 1, R/G/B could output high impedance state if the intensity attribute of characters or windows is set to 0. It means the corresponding R/G/B output will go high impedance instead of driving-high while displaying the low intensity characters or windows. After power on, this bit is reset and the R/G/B are push-pull outputs initially.

Bit 1 FAN - It enables the fan-in/fan-out functions when OSD is turned on from off state or vice versa. If this bit is set, it roughly takes about one second to fully display the whole menu. It also takes 1 second to disappear completely.

Bit 0 FBKGC - It determines the configuration of FBKG output pin. When it is clear. FBKG pin outputs high during displaying characters or windows. Otherwise, FBKG pin outputs high only during displaying characters.

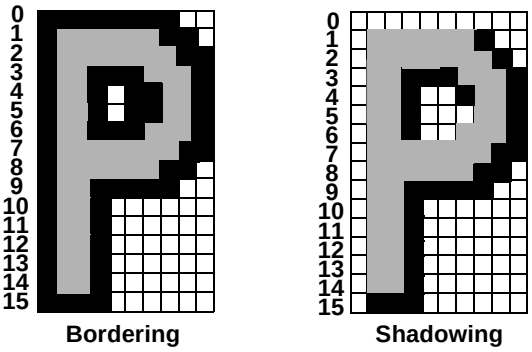
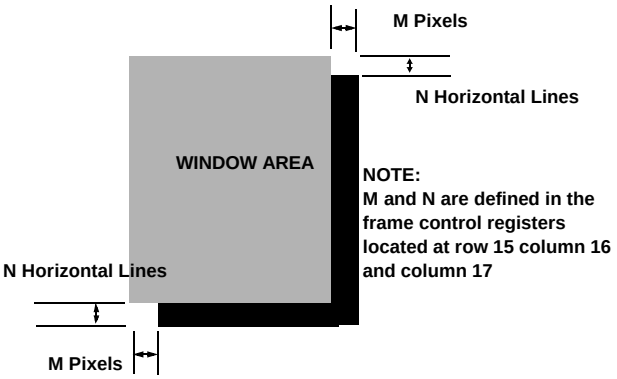


Figure 12. Character Bordering and Shadowing



Window Shadowing

Frame Control Register Row 15 Coln 16

	7	6	5	4	3	2	1	0
ROW 15 COLN 16	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

Bit 7-6 WW41, WW40 - It determines the shadow width of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where M is the actual pixel number of the shadowing.

Table 3. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width M (unit in Pixel)	2	4	6	8

Bit 5-4 WW31, WW30 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 3 when the window shadowing function is activated.

Bit 3-2 WW21, WW20 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 2 when the window shadowing function is activated.

Bit 1-0 WW11, WW10 - Similarly as WW41, WW40, these two bits determine the shadow width of the window 1 when the window shadowing function is activated

Frame Control Register Row 15 Coln 17

	7	6	5	4	3	2	1	0
ROW 15 COLN 17	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

Bit 7-6 WH41, WH40 - It determines the shadow height of the window 4 when the window shadowing function is activated. Please refer to the following table for more details where N is the actual line number of the shadowing.

Table 4. Shadow Width Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height N (unit in Line)	2	4	6	8

Bit 5-4 WH31, WH30 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 3 when the window shadowing function is activated.

Bit 3-2 WH21, WH20 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 2 when the window shadowing function is activated.

Bit 1-0 WH11, WH10 - Similarly as WH41, WH40, these two bits determine the shadow height of the window 1 when the window shadowing function is activated.

Frame Control Register Row 15 Coln 18

	7	6	5	4	3	2	1	0
ROW 15 COLN 18	RSPACE MSB				LSB	TRIC	HPOL	VPOL

Bit 7-3 RSPACE - These 5 bits define the row to row spacing in unit of horizontal scan line. It means extra N lines, defined by this 5-bit value, will be appended for each display row. Because of the nonuniform expansion of BRM used by character height control, this register is usually used to maintain the constant OSD menu height for different display modes instead of adjusting the character height. The default value of it is 0. It means there is no any extra line inserted between row and row after power on. It can be used for Portrait monitor too when icon design is rotated 90 degree.

Bit 2 TRIC - Tri-state Control. This bit is used to control the driving state of output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is reset and R, G, B and FBKG are in high impedance state while OSD being disabled. If it is set by MCU, these four output pins will drive low while OSD being in disabled state. Basically, the setting is dependent on the requirement of the external application circuit.

Bit 1 HPOL - This bit selects the polarity of the incoming horizontal sync signal (HFLB). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive H sync signal. After power on, this bit is cleared.

Bit 0 VPOL - This bit selects the polarity of the incoming vertical sync signal (VFLB). If it is negative polarity, clear this bit. Otherwise, set this bit to 1 to represent the positive V sync signal. After power on, this bit is cleared.

- **NOTE: The registers located at column 19 of row 15 are reserved for the chip testing. In normal operation, they should not be programmed anytime.**

A software called HSGMOSD-16 FONT EDITOR in IBM PC environment was written for MC141545P2C editing purposes. It generates a set of S-Record or Binary record for the desired display patterns to be masked onto the character ROM of the MC141545P2C.

In order to have better character display within windows, we suggest you to place your designed character font in the centre of the 12x18 matrix, and let its spaces be equally located in the four sides of the matrix. The character $00 is pre-defined for blank character, the character $FF is pre-defined for full-filled character.

In order to avoid submersion of displayed symbols or characters into a background of comparable colors, a feature of bordering which encircles all four sides, or shadowing which encircles only the right and bottom sides of an individual display character is provided. Figure 12 shows how a character is being jacketed differently. To make sure that a character is bordered or shadowed correctly, at least one dot blank should be reserved on each side of the character font.

Frame Format and Timing

Figure 13 illustrates the positions of all display characters on the screen relative to the leading edge of horizontal and vertical flyback signals. The shaded area indicates the area not interfered by the display characters. Notice that there are two components in the equations stated in Figure 13 for horizontal and vertical delays: fixed delays from the leading edge of HFLB and VFLB signals, regardless of the values of HORD and VERTD: (47 dots + phase detection pulse width) and one H scan line for horizontal and vertical delays, respectively; variable delays determined by the values of HORD and VERTD. Refer to Frame Control Registers COLN 9 and 10 for the definitions of VERTD and HORD. Phase detection pulse width is a function of the external charge-up resistor, which is the 1MΩ resistor in a series with 10 kΩ to VCO pin in the Application Diagram. Dot frequency is determined by the equation: H Freq. x 384 if the bit X32B is clear and H Freq. x 768 if bit X32B is set to 1. For example, dot frequency is 12.28 MHz if H freq is 32 KHz while bit X32B is 0. If X32B is 1, the dot frequency will be 24.57 MHz (double of the original one).

When double character width is selected for a row, only the even-numbered characters will be displayed, as shown in row 2. Notice that the total number of horizontal scan lines in the display frame is variable, depending on the chosen character height of each row. Care should be taken while configuring each row character height so that the last horizontal scan line in the display frame always comes out before the leading edge of VFLB of next frame to avoid wrapping display characters of the last few rows in the current frame into the next

frame. The number of display dots in a horizontal scan line is always fixed at 360, regardless of row character width and the setting of bit X32B.

Although there are 30 character display registers that can be programmed for each row, not every programmed character can be shown on the screen in 384 dots resolution. Usually, only 24 characters can be shown in this resolution at most. This is induced by the retrace time that is required to retrace the H scan line. In other resolution, 768 dots, 30 characters can be displayed on the screen totally if the horizontal delay register is set properly.

Figure 14 illustrates the timing of all output signals as a function of window and fast blanking features. Line 3 of all three characters is used to illustrate the timing signals. The shaded area depicts the window area. Both the left hand side and right hand side characters are embodied in a window with only one difference: FBKGC bit. The middle character does not have a window as its background. Timing of signal FBKG depends on the configuration of FBKGC bit. The configuration of FBKGC bits affects only FBKG signal timing. Waveform 'R, G or B', which is the actual waveform at R, G, or B pin, is the logical OR of waveform 'character R, G or B' and waveform 'window R, G or B'. 'Character R, G, or B' and 'window R, G, or B' are internal signals for illustration purpose only.

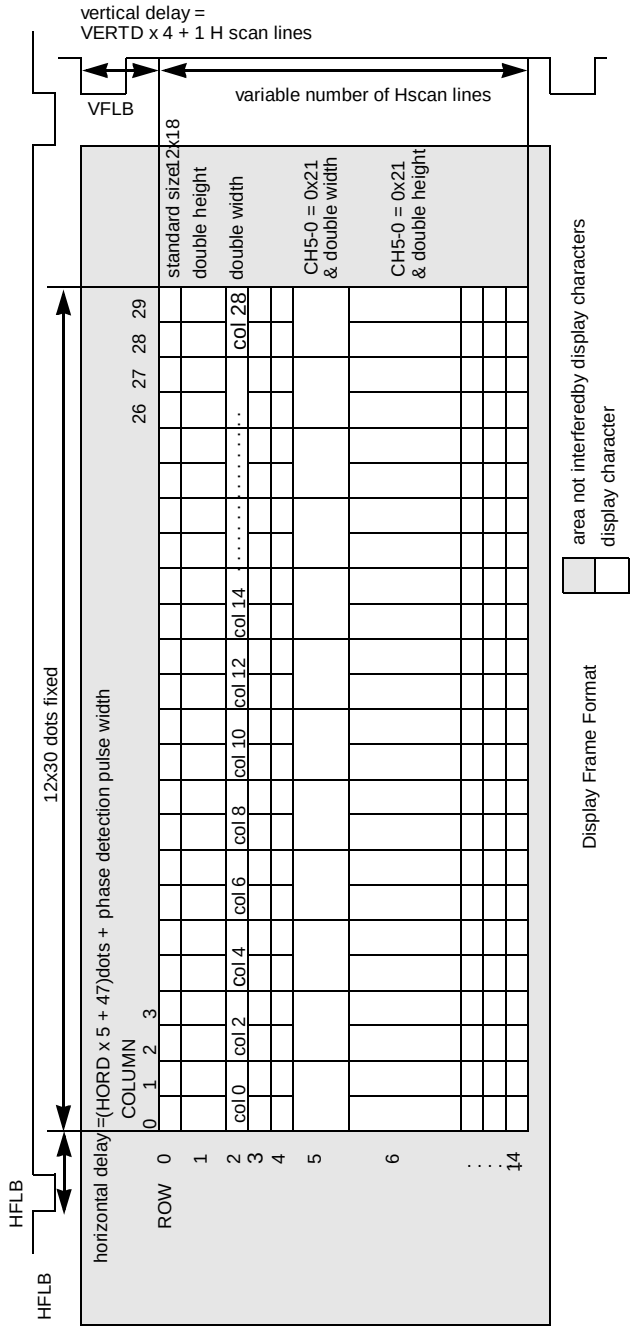


Figure 13. Display Frame Format

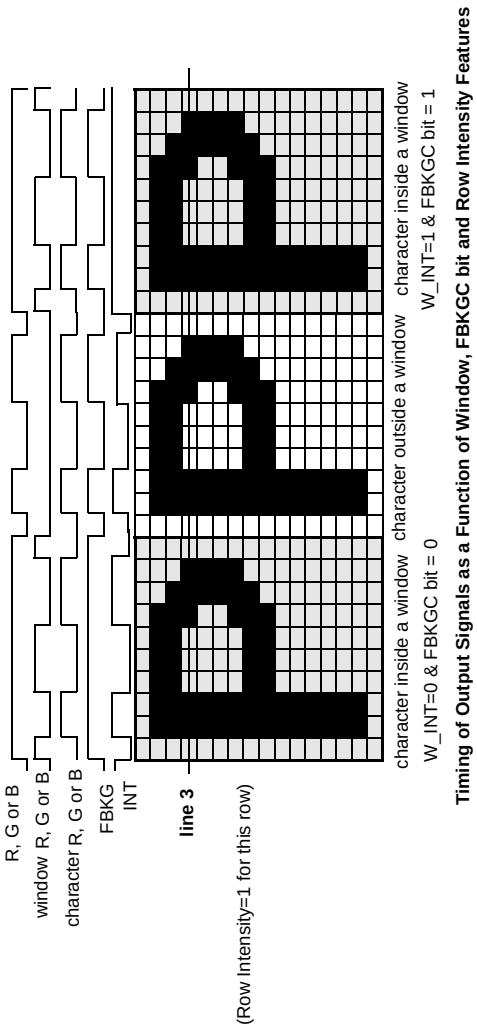


Figure 14. Timing of Output Signals

FONT

MC141545P2C contains 256 character/symbol fonts including 240 normal fonts and 16 multi-color fonts. The normal fonts are located from number $00 to $EF . The 16 multi-color fonts occupy number $F0 to $FF and their patterns can be designed using Font Editor. See the figures on the next page for the details fonts mapping.

Multi-Color Font

The color fonts comprises three different R, G, and B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to the correspondig R/G/B output. See Figure 15 for the sample displayed color font. No black color can be defined in color font: Black window underline the color font can make the dots(RGB=000) become black in color. It has to be consider during font design stage.

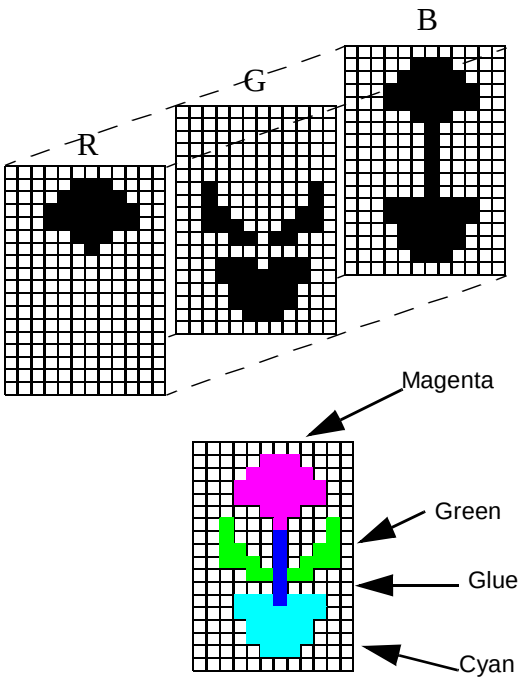


Figure 15. Example of Multi-Color Font

Table 5. The Multi-Color Font Color Selection

	R	G	B
Background Color	**0**	**0**	**0**
Blue	**0**	**0**	**1**
Green	**0**	**1**	**0**
Cyan	**0**	**1**	**1**
Red	**1**	**0**	**0**
Magenta	**1**	**0**	**1**
Yellow	**1**	**1**	**0**
White	**1**	**1**	**1**

Icon Combination

User can create On-Screen menu based on those characters and icons. Address $00 & $EF are pre-defined characters for testing.

ROM CONTENT

Figures 19 – 22 show the ROM content of MC141545P2. Mask ROM is optional for custom parts.

Table 6. Combination Map

ICON	ROM ADDRESS(HEX)
ARABIC NUMERALS	08-11
ALPHABET	12-2D
EUROPEAN	2E-48
JAPANESE	49-81
SYMBOLS	01-07, 82-C4
GEOMETRY	C5-EE
COLOR	F0-FF

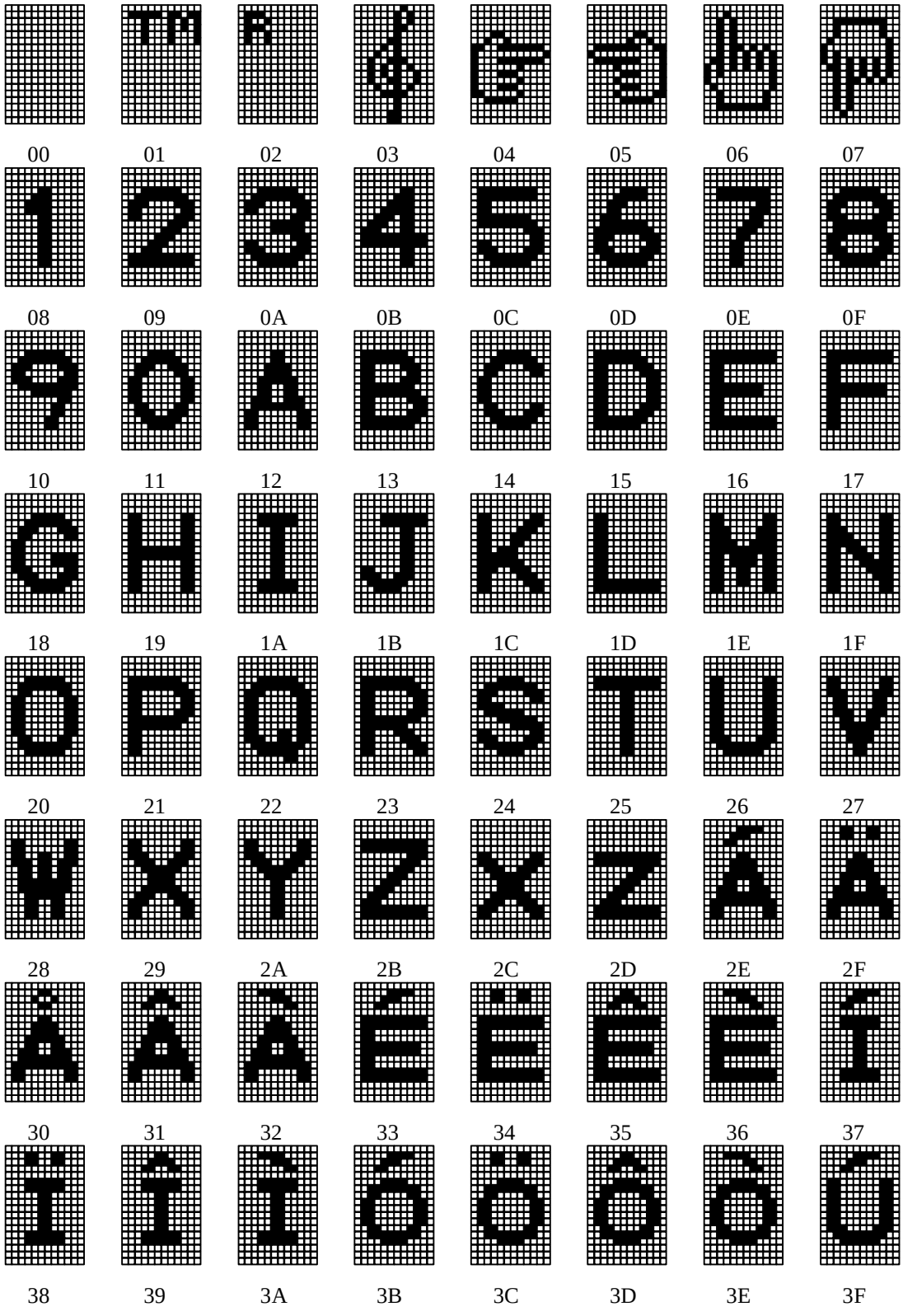


Figure 16. ROM $00 - $3F

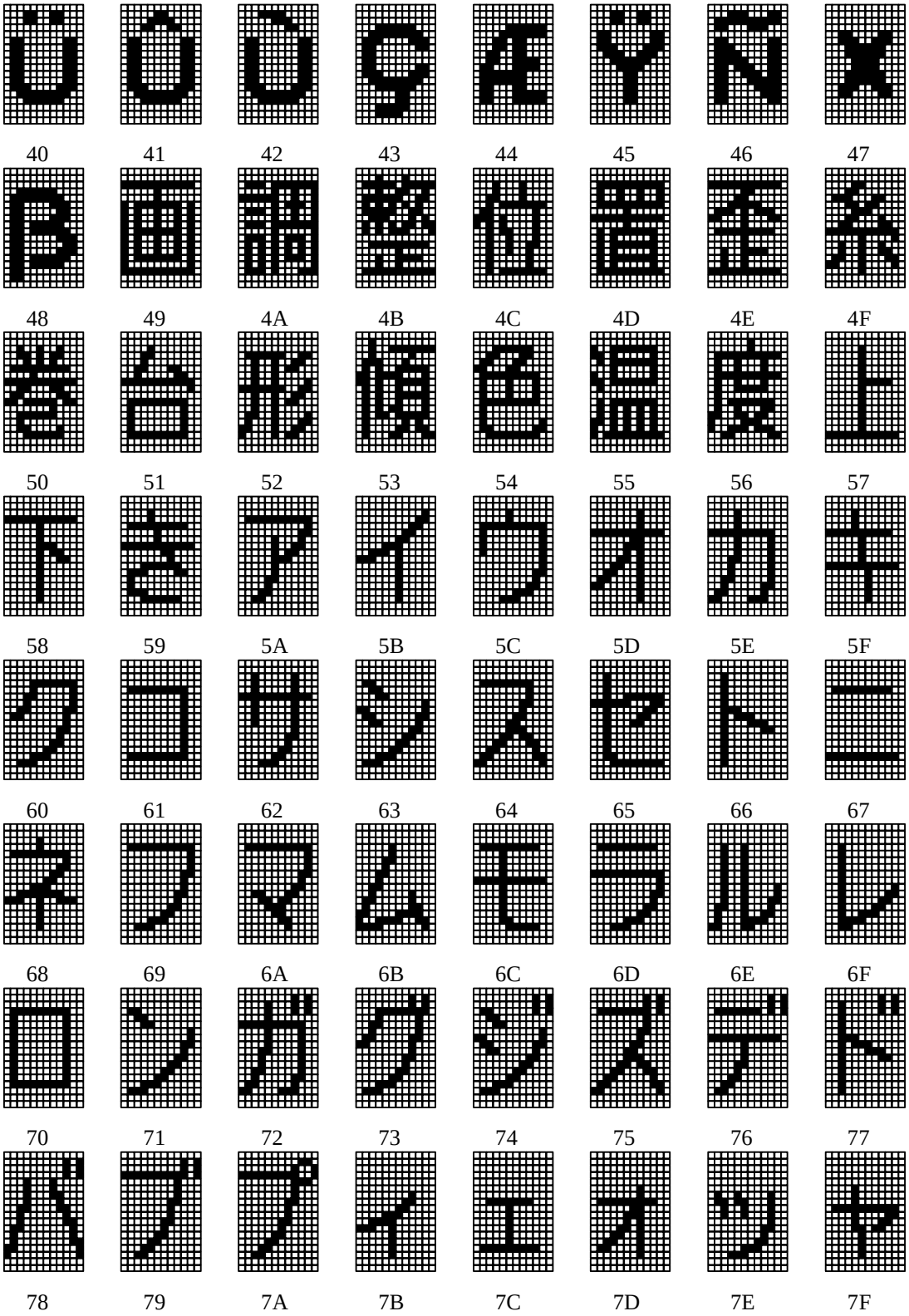


Figure 17. ROM $40 - $7F

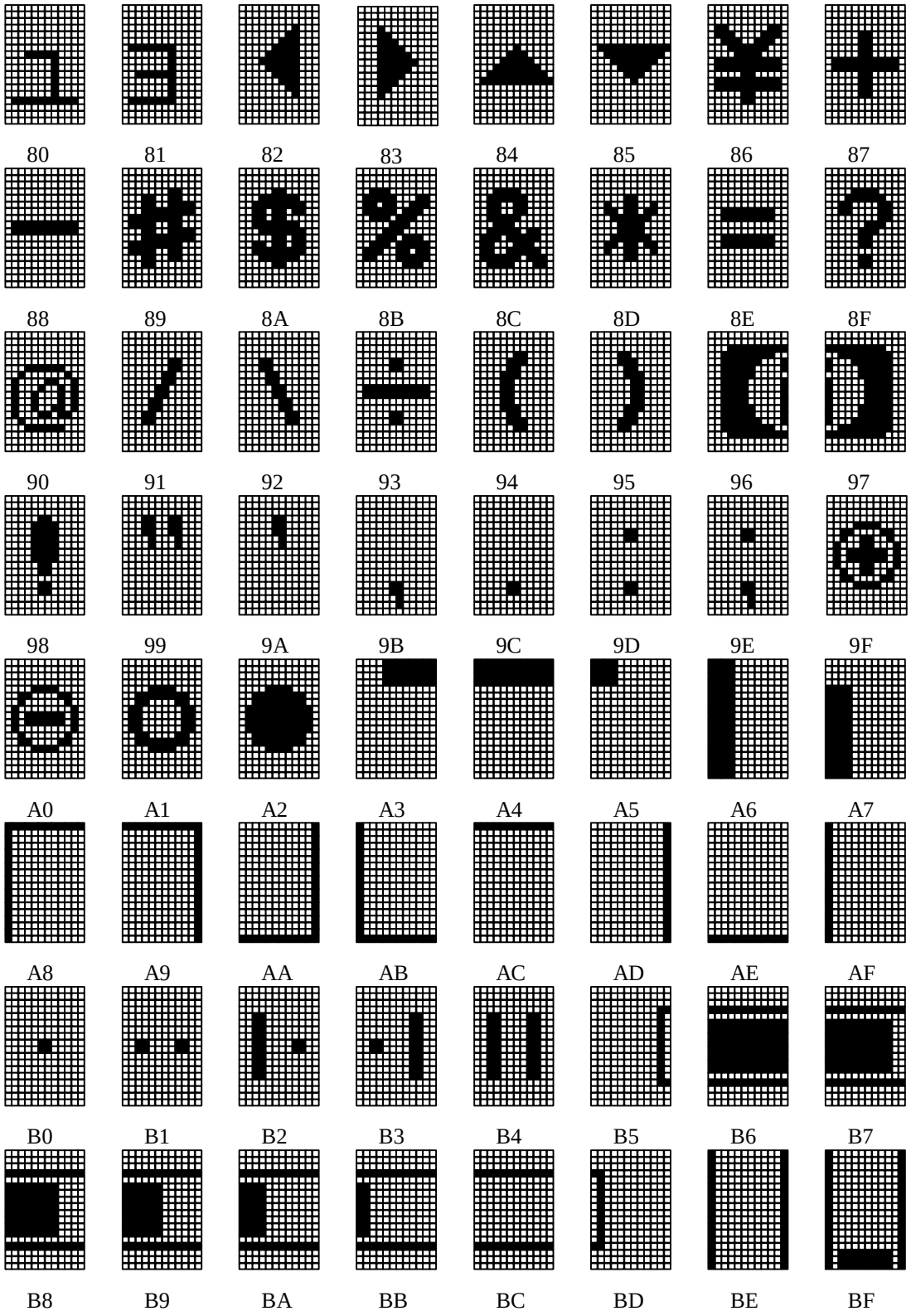


Figure 18. ROM $80-$BF

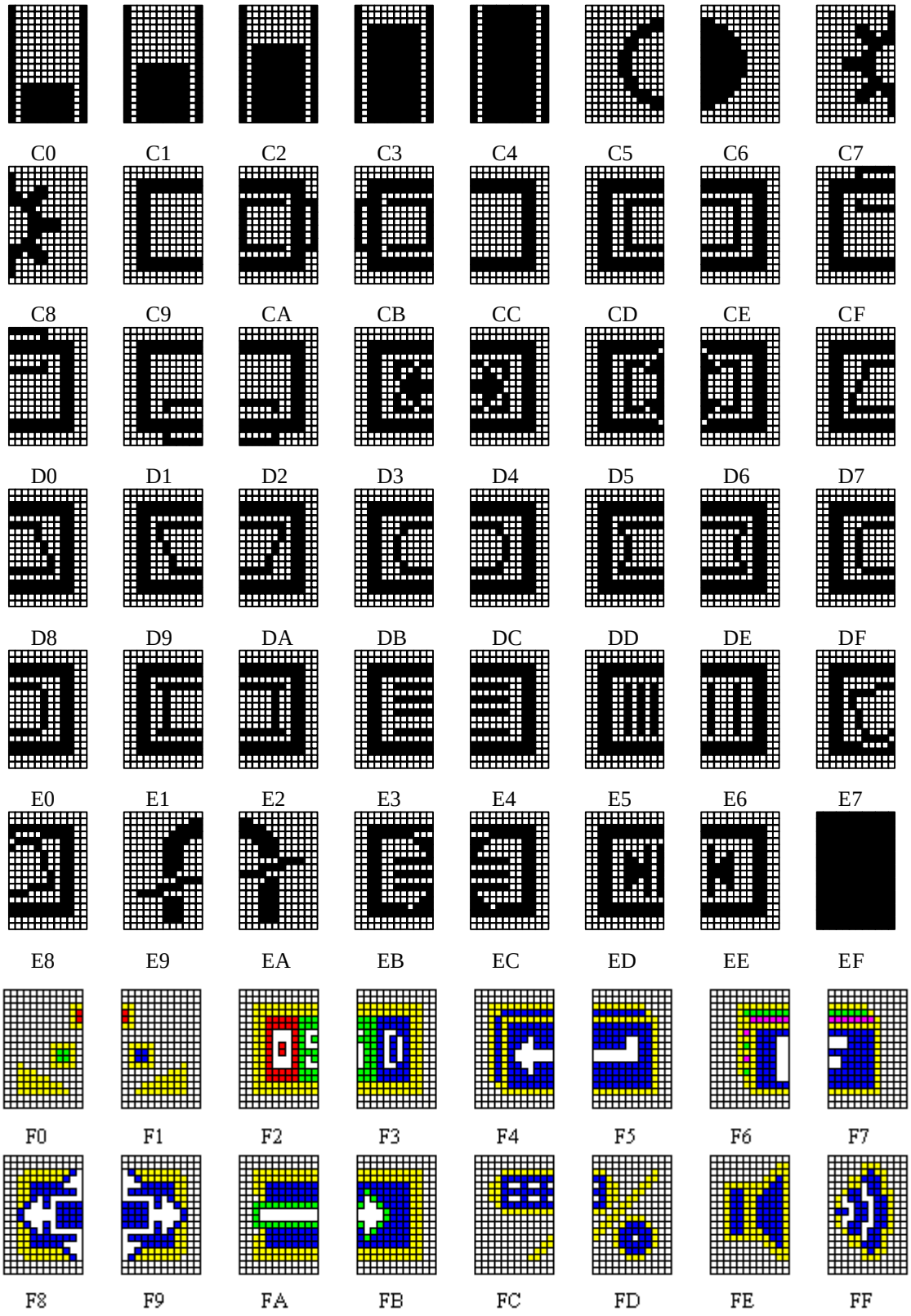


Figure 19. ROM $C0 - $FF

DESIGN CONSIDERATIONS

Distortion

Motorola's MC141545P2C has a built-in PLL for multisystems application. Pin 2 voltage is a dc basing for the internal VCO in the PLL. When the input frequency (HFLB) in Pin 5 becomes higher, the VCO voltage will increase accordingly. The built-in PLL then has a higher locked frequency output. The frequency should be equal to 384/768 x HFLB (depends on resolution). It is the dot-clock in each horizontal line.

Display distortion is caused by noise in Pin 2. Positive noise makes VCO run faster than normal. The corresponding scan line will be shorter accordingly. In contrast, negative noise causes the scan line to be longer. The net result will be distortion on the display, especially on the right hand side with window turn on.

In order to have distortion-free display, the following recommendations should be considered.

- Only analog part grounds (Pin 2 to Pin 4) can be connected to Pin 1($V_{SS(A)}$). V_{SS} and other grounds should connect to PCB common ground. Then the $V_{SS(A)}$ and V_{SS} grounds can be connected by a bead core. Please refer to the application diagram(NOTE: Vss(A) and Vss are connected internally.)
- DC supply path for Pin 4 ($V_{DD(A)}$) should be separated from other switching devices.
- LC filter should be connected between Pin 9 and Pin 4. Refer to the values used in the Application Diagram.
- Biasing and filter networks should be connected to Pin 2 and Pin 3. Refer to the recommended networks in the Application Diagram.
- Two small capacitors can be added between Pin1-Pin2 and Pin3-Pin4 to filter VCO noise if necessarry. Values should be small enough to avoid picture unlocking caused by temperature variation.
- A bead core can be added after Pin4 VDDA(the 0.33uH shown in diagram) to filter power noise if necessary.

Jittering and Unlocking

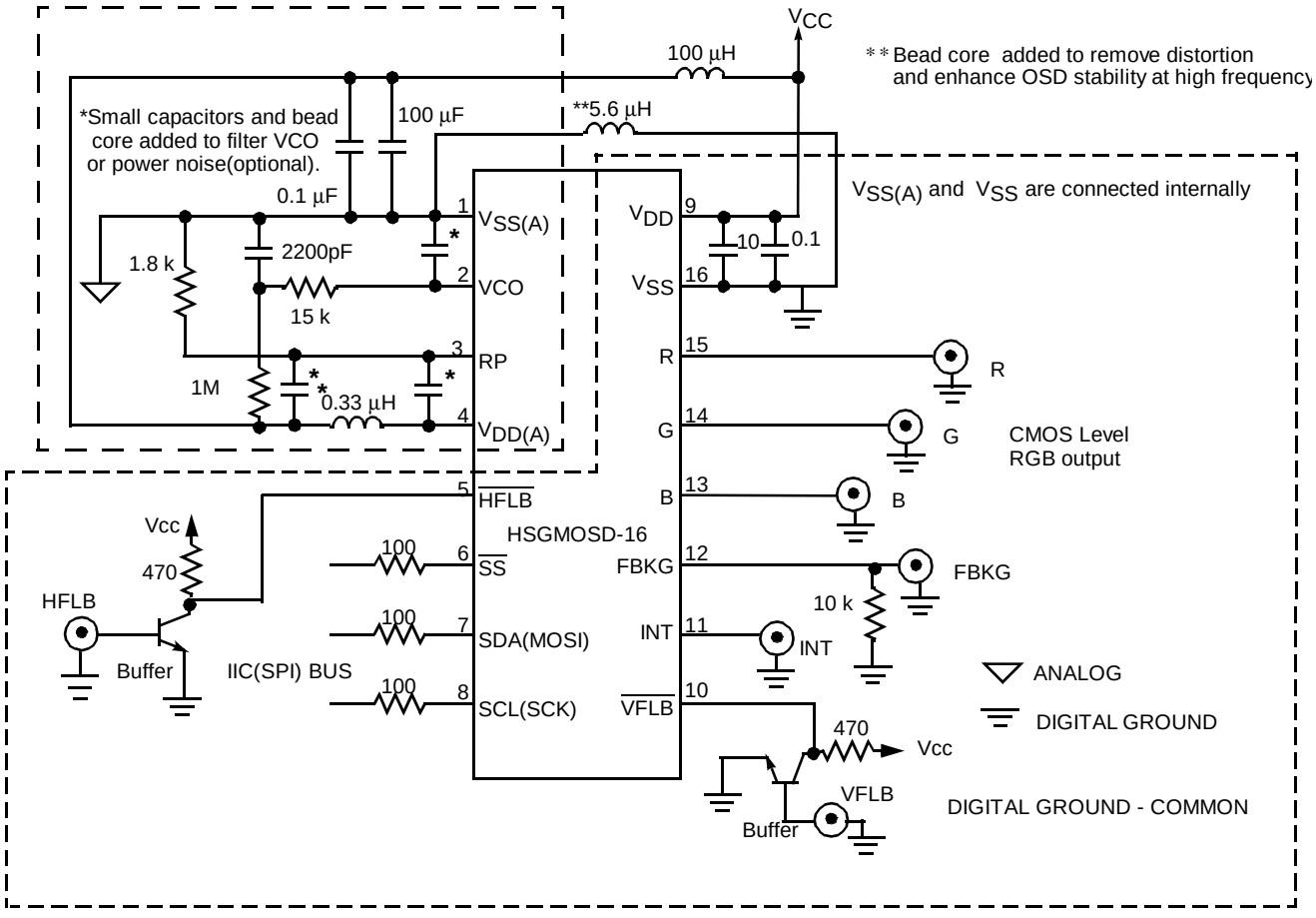
Most display jittering and unlocking is caused by HFLB in Pin 5. Care must be taken if the HFLB signal comes from the flyback transformer. A short path and shielded cable are recommended for a clean signal. Buffer is needed for both HFLB and VFLB inputs. Refer to the value used in the Application Diagram.

Note:The bead core added between $V_{SS(A)}$ and V_{SS} can also enhance the OSD stability in high frequency HFLB operation .

Display Dancing

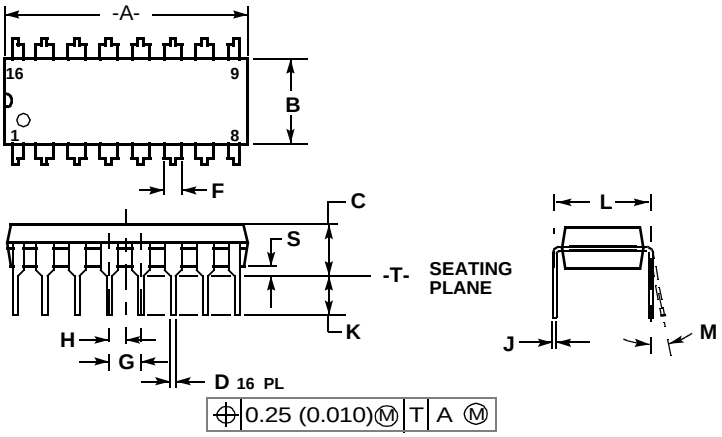
Most display dancing is caused by interference of the serial bus. It can be avoided by adding resistors in the bus in series.

APPLICATION DIAGRAM



PACKAGE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE(DUAL IN-LINE PACKAGE)



NOTES:
1.DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.CONTROLLING DIMENSION: INCH.
3.DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4.DIMENSION B DOES NOT INCLUDE MOLD

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01