Zero-Standby Power 20-Pin EPLD

Features

- 20-pin Universal EPLD
- Virtually Zero Standby Power
- Functional Replacement for Common 20-Pin Programmable Devices
  - I_{OL} = 24 mA
- High Performance CMOS EPROM Cell Technology
  - Erasable
  - Reconfigurable
  - 100% Testable
- 25 ns and 35 ns Max Propagation Delay (Commercial)
- 30 ns and 40 ns Max Propagation Delay (Industrial)
- Up to 18 Inputs and 8 Input/Output Macrocells
- Programmable Output Polarity
- Power-Up Reset on all Registers
- Register Preload Capability
- Synchronous Preset/Asynchronous Reset
- Security Fuse to Protect Duplication of Proprietary Designs
- Design Support Provided using many Popular Software Development Packages for PLDs
- Available in 300-mil-wide DIP with Quartz Window, Plastic DIP (OTP), or PLCC (OTP)
- Second Source to Signetic's PLC18V8Z/I

Description

The AT18V8Z is a universal EPLD featuring high performance and virtually zero-standby power for power-sensitive applications. It is a reliable, user-configurable substitute for discrete TTL/CMOS logic. While compatible with TTL and HCT logic, the AT18V8Z can also replace HC logic over the V_{CC} range of 4.5 to 5.5 V.

The AT18V8Z is a two-level logic element comprised of ten inputs, 74 AND gates (product terms), and eight output Macrocells.

Each output features an "Output Macrocell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the AT18V8Z is capable of emulating all common 20-pin programmable logic devices to reduce documentation, inventory, and manufacturing costs.

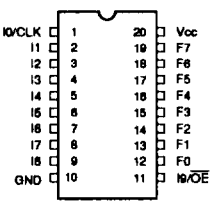
A power-up reset function and a Register Preload function have been incorporated into the AT18V8Z architecture to facilitate state machine design and testing.

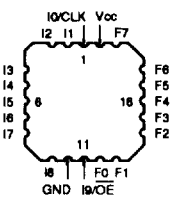
With a standby current of less than 100 µA and active power consumption of 1.5 mA/MHz, the AT18V8Z is ideally suited for power-sensitive applications in battery-operated/backed portable instruments and computers.

The AT18V8Z is also processed to industrial requirements for operation over an extended temperature range of -40°C to +85°C and supply voltage of 4.5 V to 5.5 V.

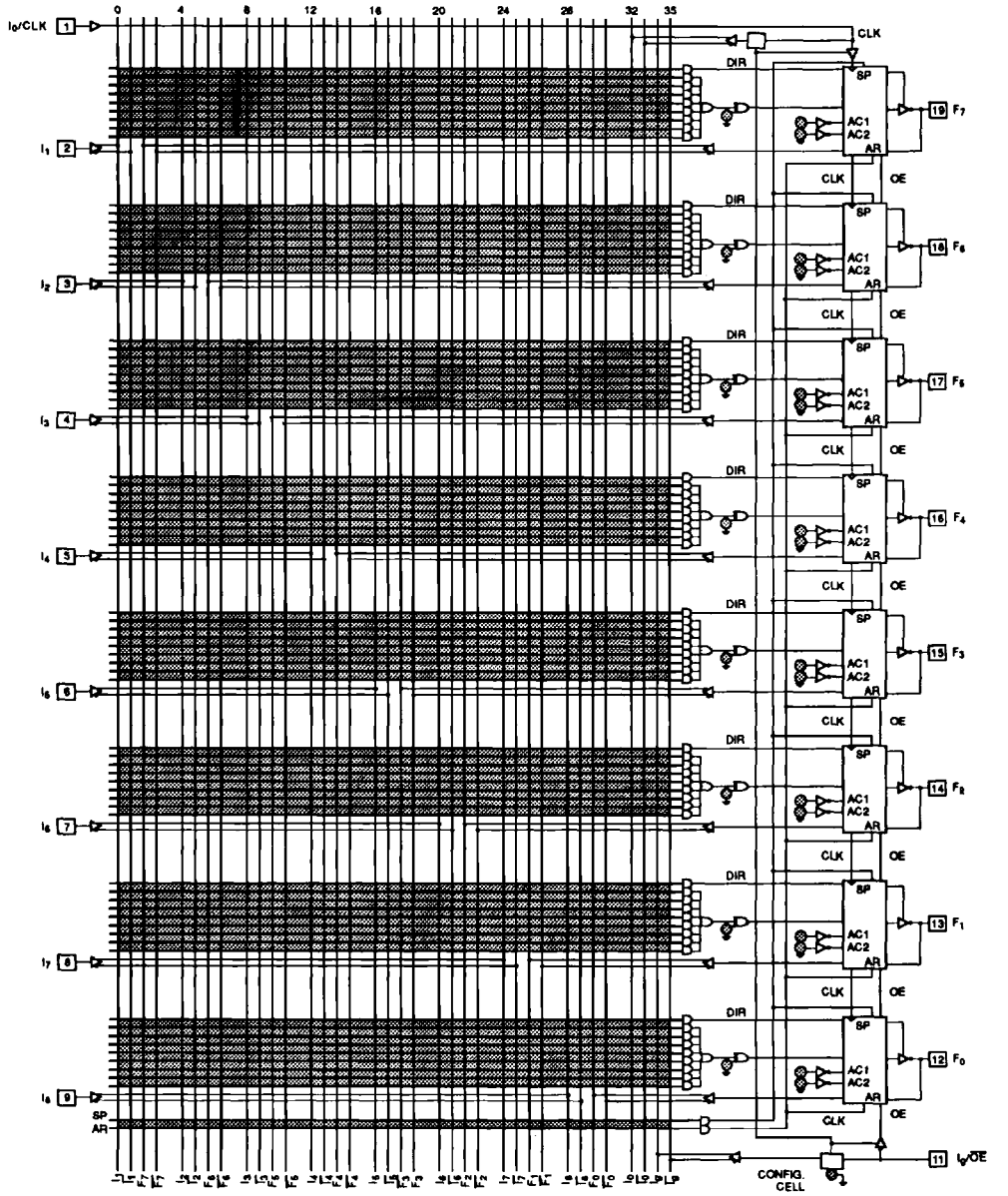
Pin Configurations

Pin Name	Function
I#/CLK	Clock and Logic Input
I#/OE	Output Enable and Logic Input
I#	Logic Inputs
F#	Bidirectional Buffers
*	No Internal Connection
V_{CC}	+5 V Supply





Logic Diagram



Notes:

In the unprogrammed or virgin state:

1. All cells are in a conductive state.
2. All AND gate locations are pulled to a logic "0" (Low).
3. Output polarity is inverting.

Denotes a programmable cell location.

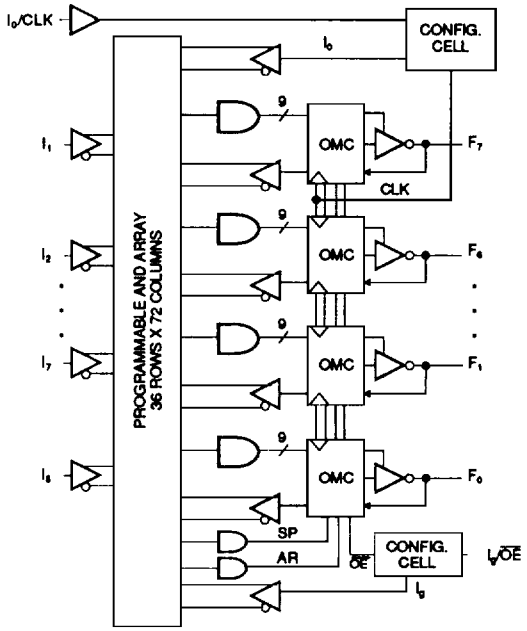
4. Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and $\overline{OE}$ functions are disabled.
5. All output macrocells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.

Absolute Maximum Ratings*

Operating Temperature (Commercial)	0°C to +75°C
Operating Temperature (Industrial)	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5 to +7 V_{DC}
Operating Supply Voltage (Commercial)	4.75 to 5.25 V_{DC}
Operating Supply Voltage (Industrial)	4.5 to 5.5 V_{DC}
Input Voltages (including N.C. Pins) with Respect to Ground	-0.5 V to V_{CC}+0.5 V_{DC}
Output Voltages with Respect to Ground	-0.5 V to V_{CC}+0.5 V_{DC}
Input Currents	-10 to +10 mA
Output Currents	+24 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functional Diagram



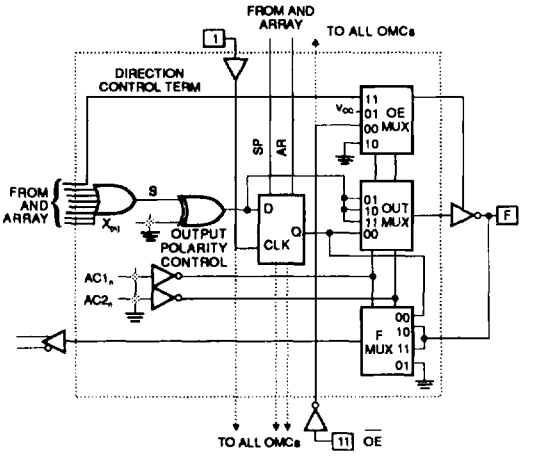
PAL Device to AT18V8Z Output Pin Configuration Cross Reference

Pin	AT18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	$I_9/\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

The Atmel state-of-the-art floating-gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Atmel to functionally test the devices prior to shipment to the customer. Additionally, this allows Atmel to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

PAL may be a registered trademark of AMD Corp.

Output Macrocell (OMC)



Note:
▒ Denotes a programmable cell location.

The Output Macrocell (OMC)

The AT18V8Z series devices have eight individually programmable Output Macrocells. The 72 AND inputs (or product terms) from the programmable AND array are connected to the eight OMCs in groups of nine. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macrocell). Similarly, each OMC has a programmable output polarity control bit (X_n). By configuring the pair of architecture control bits according to the configuration cell table, four different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

Design Security

The AT18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device.

Configuration Cell

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

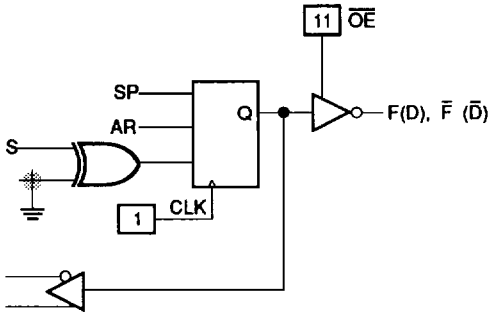
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

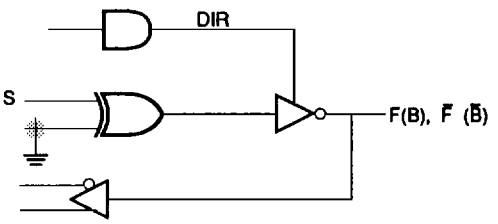
Function	Control Cell Configurations			Comments
	$AC1_n$	$AC2_n$	Config. Cell	
Registered Mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ control for all registered OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

Note:
1. This is the virgin state as shipped by the factory.

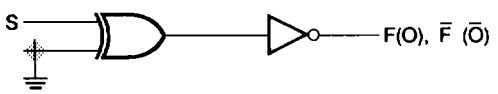
Architecture Control: AC1 and AC2



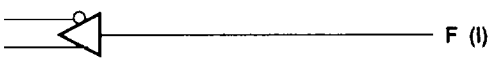
OMC Configuration	Code
Registered (D-type)	D



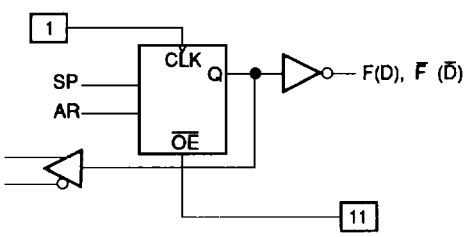
OMC Configuration	Code
Bidirectional I/O[1] (Combinatorial)	B



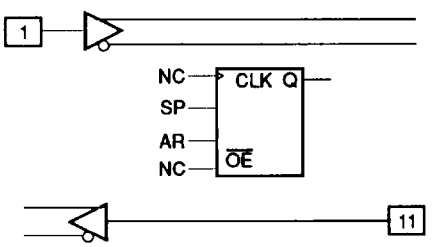
OMC Configuration	Code
Fixed Output	O



OMC Configuration	Code
Fixed Input	I



OMC Configuration	Code
Pin 1 = $\overline{CLK}$ Pin 11 = $\overline{OE}$	L



OMC Configuration	Code
Pin 1 = Input Pin 11 = Input	H[6]

Notes:
A factory shipped unprogrammed device is configured such that:

1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macrocells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

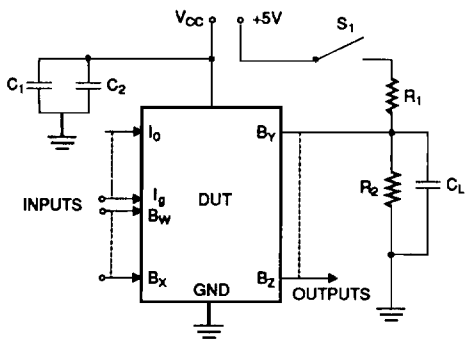
D.C. Characteristics

T_{AC} = 0°C to +75°C, V_{CC} = 4.75 V to 5.25 V; T_{AI} = -40°C to 85°C, V_{CC} = 4.5 V to 5.25 V; R_2 = 390 Ω

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{CC} = Min	-0.3		0.8	V
V_{IH}	Input High Voltage	V_{CC} = Max	2.0		V_{CC}+0.3	V
V_{OL} (2)	Output Low Voltage	V_{CC} = Min, I_{OL} = 24 mA			0.500	V
V_{OH} (2)	Output High Voltage	V_{CC} = Min, I_{OH} = -3.2 mA	2.4			V
		V_{CC} = Min, I_{OH} = -20 µA	V_{CC}-0.1 V			V
I_{IL}	Input Low Current	V_{IN} = GND			-10	µA
I_{IH} (7)	Input High Current	V_{IN} = V_{CC}			10	µA
$I_{O(OFF)}$	Hi-Z State Output Current	V_{OUT} = V_{CC}			10	µA
		V_{OUT} = GND			-10	µA
I_{OS} (3)	Short Circuit Output Current	V_{OUT} = GND			-130	mA
I_{CC}	V_{CC} Standby Supply Current	V_{CC} = Max, V_{IN} = 0 or V_{CC} (8)			100	µA
$I_{CC/f}$ (4)	V_{CC} Active Supply Current	V_{CC} = Max (CMOS Inputs) (5,6)			1.5	mA/MHz
C_I	Input Capacitance	V_{CC} = 5 V, V_{IN} = 2.0 V		12		pF
C_B	I/O Capacitance	V_B = 2.0 V		15		pF

Notes:
1. All typical values are at V_{CC} = 5 V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TLL input levels: V_{IL} = 0.45 V, V_{IH} = 2.4 V. Measured with all outputs switching.
5. ΔI_{CC}/TLL input = 2 mA.
6. ΔI_{CC} vs. frequency (registered configuration) = 2 mA/MHz.
7. I_{IL} for Pin 1 (I_O/CLK) is ± 10 µA with V_{IN} = 0.4 V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

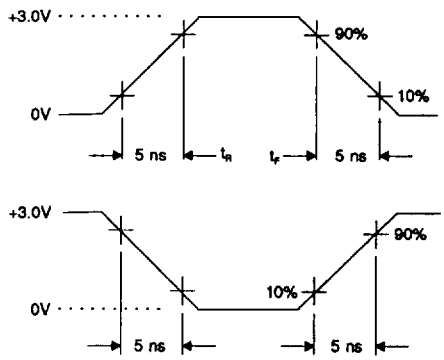
A.C. Test Conditions



Notes:
C_1 and C2 are to bypass V_{CC} to GND.
C_L = 50 pF
R_1 = 200 Ω
R_2 = 390 Ω

Voltage Waveforms

Input Pulses



Note: All circuit delays are measured at the +1.5 V level of inputs and outputs, unless otherwise specified.

A.C. Read Characteristics

T_{AC} = 0°C to +75°C, V_{CC} = 4.75 V to 5.25 V; T_{AI} = -40°C to 85°C, V_{CC} = 4.5 V to 5.25 V; R_2 = 390 Ω

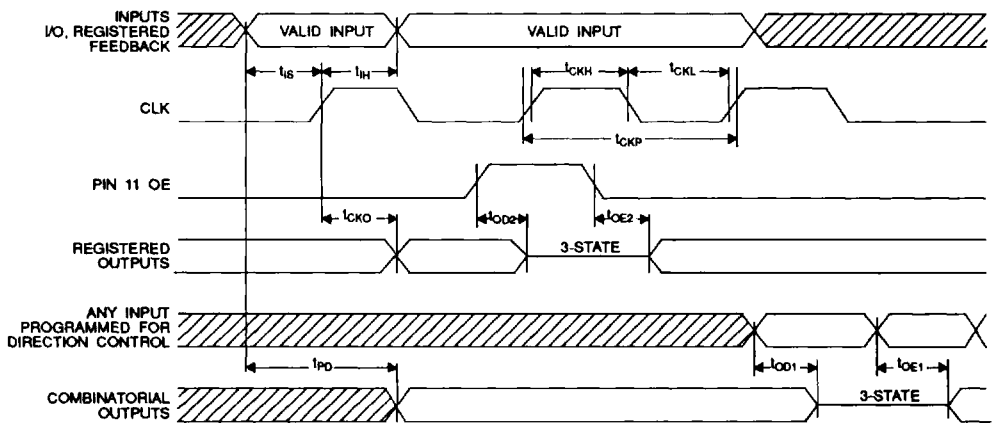
				AT18V8Z								
				-25		-30		-35 (Comm.)		-35 (Ind.)		
Symbol	Parameter	From	To	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{CKP}	Clock Period (Minimum t_{IS} + t_{CKO})	CLK+	CLK+	33		40		47		57		ns
t_{CKH}	Clock Width High	CLK+	CLK-	15		20		20		25		ns
t_{CKL}	Clock Width Low	CLK-	CLK+	15		20		20		25		ns
t_{ARW}	Asynchronous Reset Pulse Width	I±, F±	I±, F±	25		30		35		40		ns
t_{IH}	Input or Feedback Data Hold Time	CLK+	Input±	0		0		0		0		ns
t_{IS}	Input of Feedback Data Setup Time	I±, F±	CLK+	18		2		25		30		ns
t_{PD}	Delay from Input to Active Output	I±, F±	F±		25		30		35		40	ns
t_{CKO}	Clock High to Output Valid Access Time	CLK+	F±		15		18		22		27	ns
t_{OE1}	Product Term Enable to Outputs Off	I±, F±	F±		25		30		35		40	ns
t_{OD1}	Pin 11 Output Disable to Outputs Off	I±, F±	F±		25		30		35		40	ns
t_{OD2}	Pin 11 Output Disable High to Outputs Off	OE-	F±		20		25		25		30	ns
t_{OE2}	Pin 11 Output Enable to Active Output	OE+	F±		20		25		25		30	ns
t_{ARD}	Asynchronous Reset Delay	I±, F±	F+		30		35		35		40	ns
t_{ARR}	Asynchronous Reset Recovery Time	I±, F±	CLK+	20		25		25		30		ns
t_{SPR}	Synchronous Preset Recovery Time	I±, F±	CLK+	20		25		25		30		ns
t_{PPR}	Power-Up Reset	V_{CC}+	F+		25		30		35		40	ns
f_{MAX}	Maximum Frequency	$1/(t_{IS} + t_{CKO})$			30		25		21		18	ns

Power Up Reset

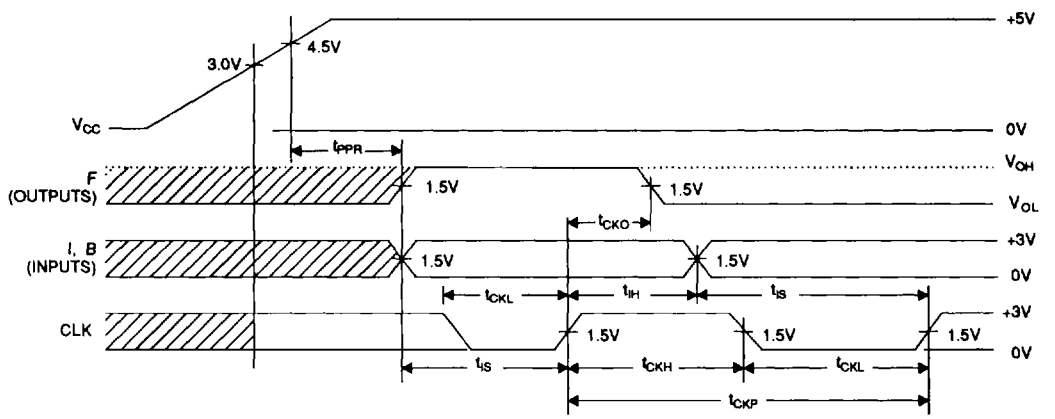
In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the AT18V8Z. All internal registers will reset to Active-Low (logical "0") after a specified period of time (t_{PPR}).

Therefore, any OMC that has been configured as a registered output will always produce an Active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the Active-High output condition during a system power-up condition.

Switching Waveforms Timing Diagram

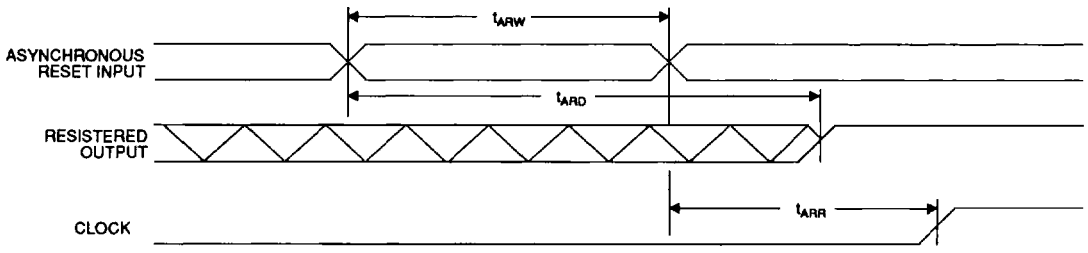


Power Up Reset Timing Diagram

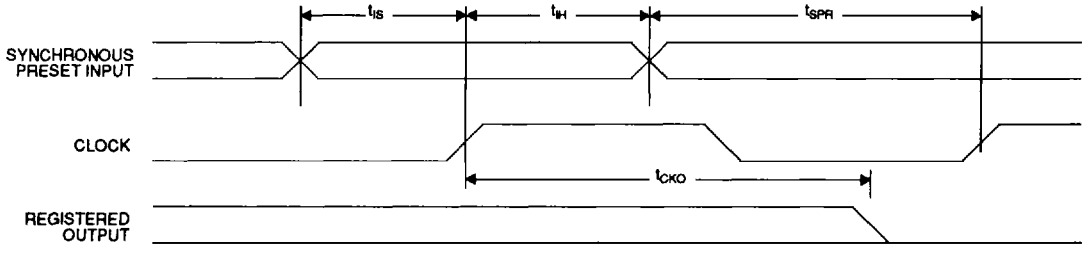


Note:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Asynchronous Reset Timing Diagram



Synchronous Preset Timing Diagram



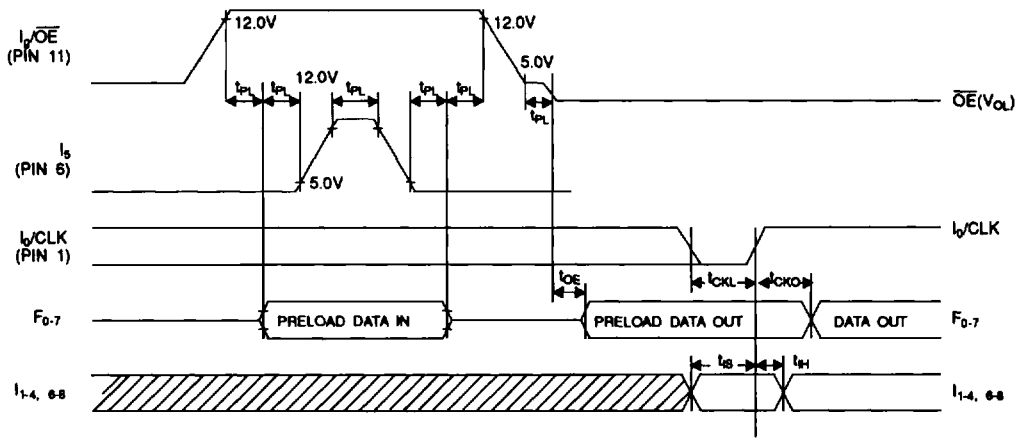
Register Preload Function (Diagnostic Mode Only)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the AT18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_8/\overline{OE}$ and I_5). (See diagram for timing and sequence).

To read the data out, Pins 11 and 6 must be returned to normal TLL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. $t_{PL} \approx 10$ µsec.

Register Preload (Diagnostic Mode)



Logic Programming

The AT18V8Z series is fully supported by industry standard (JEDEC compatible) PLD CAD tools. ABEL™ and CUPL™ design packages also support the AT18V8Z architecture.

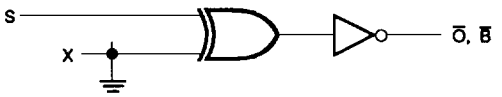
All packages allow Boolean and state equation entry formats. ABEL and CUPL also accept, as input, schematic capture format.

AT18V8Z logic designs can also be generated using the program table entry format, which is detailed on the following pages.

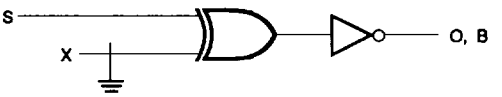
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

Output Polarity (O, B)

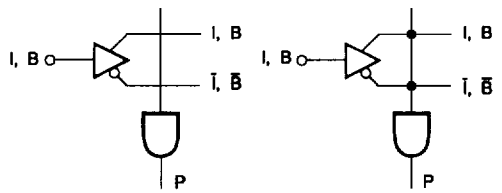


Active Level	Code
Inverting[1]	L



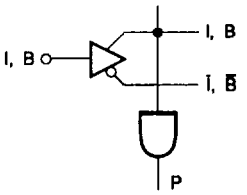
Active Level	Code
Non-inverting	H

"AND" Array (I, B)

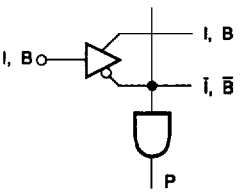


State	Code
Don't Care	–

State	Code
Inactive[1]	O



State	Code
I, B	H



State	Code
$\overline{I}$, $\overline{B}$	L

Note:
1. A factory-shipped unprogrammed device is configured such that all cells are in a conductive state.

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Erasure Characteristics (For Quartz Window Packages Only)

The erasure characteristics of the AT18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical AT18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the AT18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the AT18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000 µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258 Wsec/cm^2. Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

Programing

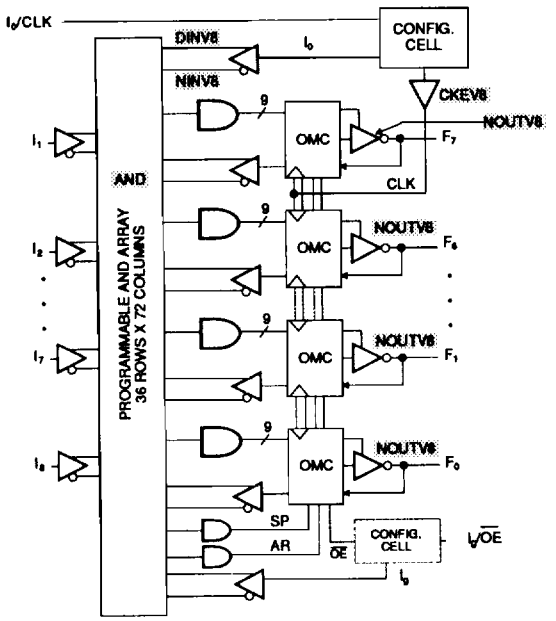
The AT18V8Z is programmable on conventional programmers for 20-pin PAL devices.

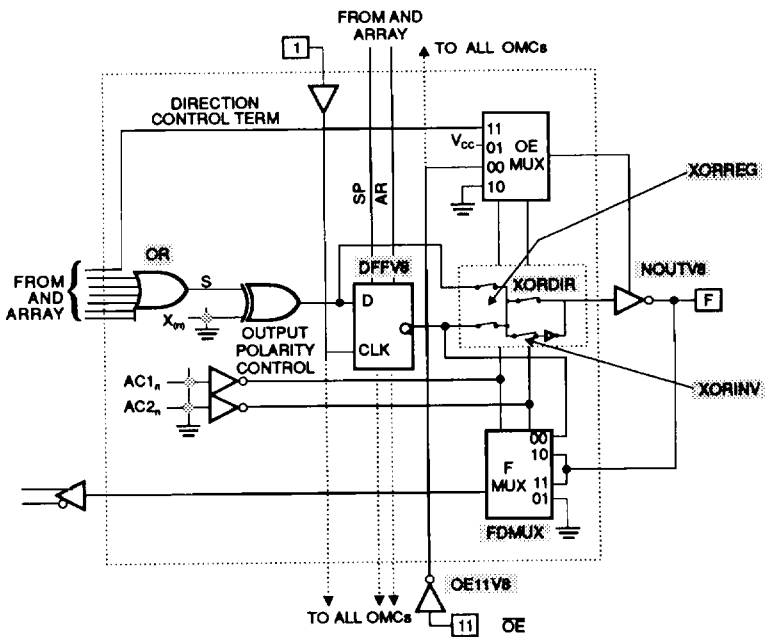
Refer to the following charts for qualified manufacturers of programmers and software tools:

Programmer Manufacturer	Programmer Model	Family/Pinout Codes
Data I/O Corporation 10525 Willows Road, N.E. P.O. Box 97046 Redmond, Washington 98073-9746 (800) 247-5700	System 29B, LogicPak™ 303A-011A; V09 (DIL) 303A-011B; VO4 (PLCC) UNISITE 40/48 V2.6 (DIL) Chipsite (PLCC)-V2.8 MODEL 60 360A001 (DIL) 360A006 (PLCC)	86/4F
Stag Microsystems, Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, California 95054 (408) 988-1118	ZL30/30A Programmer Rev. 30A34 (DIL) 30A001 Adaptor (PLCC) PPZ Programmer TBA	12/205

Software Manufacturer	Development System
Signetics Company 811 East Arques Avenue P.O. Box 3409 Sunnyvale, California 94088-3409 (408) 991-2000	SNAP Rev. 1.6 and later SLICE Rev. 1.0 and later AMAZE Software Rev. 1.8 and later
Data I/O Corporation 10525 Willows Road, N.E. P.O. Box 97046 Redmond, Washington 98073-9746 (800) 247-5700	ABEL™ Software
Logical Devices, Inc. 1201 Northwest 65th Place Fort Lauderdale, Florida 33309 (800) 331-7766	CUPL™ Software

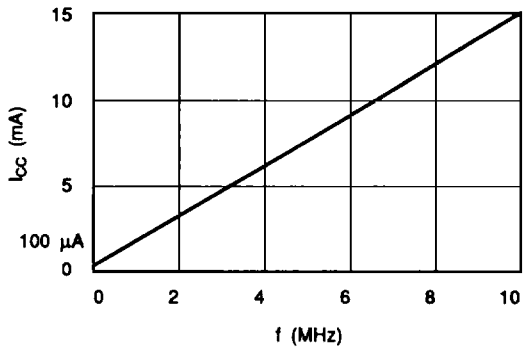
Snap Resource Summary Designations



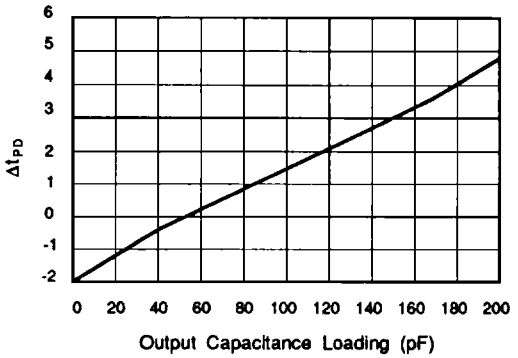


Note:
▒ Denotes a programmable cell location.

I_{CC} vs. FREQUENCY (WORST CASE)



Δt_{PD} vs. OUTPUT CAPACITANCE LOADING (TYPICAL)



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
25	18	15	AT18V8Z-25DC AT18V8Z-25JC AT18V8Z-25PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
30	22	18	AT18V8Z-30DI AT18V8Z-30JI AT18V8Z-30PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)
35	25	22	AT18V8Z-35DC AT18V8Z-35JC AT18V8Z-35PC	20DW3 20J 20P3	Commercial (0°C to 70°C)
40	30	27	AT18V8Z-40DI AT18V8Z-40JI AT18V8Z-40PI	20DW3 20J 20P3	Industrial (-40°C to 85°C)

Package Type	
20DW3	20 Lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
20J	20 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
20P3	20 Lead, 0.300" Wide Plastic Dual Inline Package OTP (PDIP)